A Programmable CMOS Feedback IC for Reconfigurable MEMS-Referenced Oscillators

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***Abstract*—MEMS resonators integrated with CMOS feedback networks have a potentially wide field of applications as oscillator circuits in communications and sensor systems. However, considerable advancements to this nascent technology are required to realize such a vision. We present a configurable CMOS chip which facilitates the development of MEMS-referenced oscillators, especially for timing and sensing applications in harsh environments. The chip has been designed in the OnSemi 3M2P 0.5 μm process. It supports MEMS resonators with various frequencies (10–120 kHz), resonant modes, and impedance levels, thus allowing interfacing to a wide range of devices. This paper describes analysis, design, and simulation results.**

I. Introduction

MEMS-based programmable frequency references are becoming popular replacements for quartz-based oscillators [1], [2], [3], especially in applications like space-constrained mobile devices and wireless sensor networks. This is due to their small form factors (system or node size $\sim$mm^2) and low power consumption (driven by the availability of ultra-high-Q resonators), low cost, and wide operating temperature range. These designs generally use a CMOS fractional-N frequency synthesizer to multiply the output frequency of a MEMS oscillator. The latter is formed by adding positive feedback (via a "sustaining" circuit) to one mode of a high-Q MEMS resonator [4]. In addition, MEMS resonators have multiple resonant modes [5], which are useful for precision sensing of mass values and spatial distributions [6], [7], and also for actuation [6]. However, mode selectivity has so far been realized by using either electronic or optomechanical sustaining networks built using desktop instruments [5], [6], which limits their applicability and makes widespread deployment difficult. In this paper we describe an IC that contains a highly-programmable sustaining circuit, thus allowing the same chip to be used to implement oscillators based on a variety of MEMS resonators, or different modes of the same resonator. We first analyze an electrical model of the MEMS device [8], and then describe an integrated CMOS feedback circuit with tunable frequency response, gain, and phase shift (see Fig. 1). Oscillators in the 10–120 kHz range can be realized by setting these parameters via 5-bit current DACs programmed from a standard serial peripheral interface (SPI) port.

II. MEMS Resonator Model

Electrical equivalent circuit models for MEMS resonators can be derived using well-known methods [8]. We assume the common form shown in Fig. 1, in which the resulting

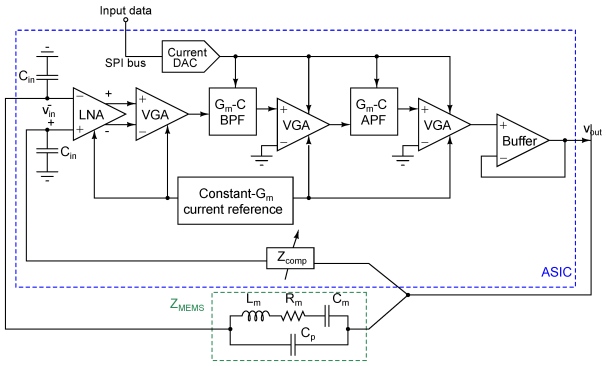

Fig. 1. Block diagram of the programmmable CMOS feedback IC. The output driver block acts as a low-impedance voltage source.

impedance Z_{MEMS} contains three motional elements in series, namely the motional resistance (R_m), inductance (L_m), and capacitance (C_m); and a parallel capacitor C_p that models the electrical capacitance between the resonator's shuttle and actuator. The resonant frequency and quality factor are

$$\omega_0 = (L_m C_m)^{-1/2} = 2\pi f_0 \ , \ Q = (\omega_0 L_m)/R_m. \quad (1)$$

The resonator is used as a two-port, which results in a frequency-dependent attenuation of $f(s) = Z_{in}/(Z_{in} + Z_{MEMS})$ across the device where $Z_{in} = 1/(sC_{in})$ is the input impedance of the chip. The on-chip sustaining network must have enough gain $|a(s)|$ to overcome this attenuation, which can be minimized by wire-bonding the resonator to the chip within the same package. In this case the dominant contributor to C_{in} becomes the capacitance of the bond-pad to the chip substrate. Moreover, the parallel capacitance C_p introduces a nearly frequency-independent "background" term $f_p = C_p/(C_{in} + C_p)$ within $f(s)$. This term can be large enough to overwhelm the desirable high-Q frequency response $f_m(\omega)$ offered by the motional branch. Specifically, the ratio of these terms near ω_0 is given by

$$\frac{f_m(\omega_0)}{f_p} = -j\left(\frac{C_{in}}{C_{in}+C_p}\right)\left(\frac{C_m}{C_p}\right)Q \approx -j\left(\frac{C_m}{C_p}\right)Q, \quad (2)$$

where the approximation is valid when $C_{in} \gg C_p$, which is usually the case. It is common for C_m to be much smaller than C_p, which results in low motional-to-background ratios even

with high-Q. In this case $f(s)$ has poor amplitude selectivity, and the phase of the sustaining network must be precisely adjusted to make the loop oscillate at ω_0. We avoid this issue by using a differential low-noise amplifier (LNA) and tunable on-chip compensation impedance $Z_{comp} = 1/(sC_p)$ (realized as a switched capacitor array) to cancel f_p. Assuming perfect cancellation, the on-resonance attenuation is

$$f(\omega_0) = -jQ\frac{C_m C_{in}}{(C_p + C_{in})^2}. \quad (3)$$

In practice cancellation will not be perfect, resulting in a residual f_p term that is $\pi/2$ out of phase with f_m. Both the phase and amplitude of $a(s)$ (the forward path) must be adjusted to compensate for the resulting change in $f(s)$.

Another important design requirement is to minimize the phase noise contributed by the sustaining circuit. The thermal noise voltage PSD of the MEMS resonator near ω_0 is $\overline{v_{M,n}^2} = 4k_BTR_m$, where k_B is Boltzmann's constant and T is the absolute temperature. Typical value for R_m are hundreds of $k\Omega$ or more [8], resulting in $\overline{v_{M,n}^2} > 40$ nV/Hz$^{1/2}$ at 300 K. However, resonator noise is filtered by Z_{MEMS} before it reaches the LNA. Since the output driver guarantees that the output of the feedback network is low impedance, the resulting PSD across the LNA input terminals is

$$\overline{v_{M,ni}^2(\omega)} \approx 4k_BTR_m\left(\frac{C_m}{C_{tot}}\right)^2\left|\frac{1}{1-\omega^2\tau^2 + j\omega\tau/Q}\right|^2, \quad (4)$$

where $C_{tot} = C_p + C_{in}$, $\tau = 1/\omega_0$, and the approximation is valid when $C_{tot} \gg C_m$, which is usually the case. Thus the resonator's noise is modulated by a resonant low-pass filter with a low-frequency gain of $(C_m/C_{tot})^2 \ll 1$, and the same resonant frequency and Q as the motional branch. The peak value of $\overline{v_{M,ni}^2}$ occurs at resonance, and is given by

$$\overline{v_{M,ni}^2(\omega_0)} = \frac{4kTR_m}{(\omega_0 R_m C_{tot})^2}. \quad (5)$$

In order not to degrade the close-in phase noise of the oscillator, i.e., its long-term stability, the input-referred noise of the entire feedback network $a(s)$, which is dominated by that of the LNA, should be negligible compared to $\overline{v_{M,ni}^2(\omega_0)}$.

III. Circuit Design

The chip contains an LNA, three variable gain amplifier (VGA) stages, a $G_m - C$ band-pass filter (BPF), and a $G_m - C$ phase shifter (all-pass filter), as shown in Fig. 1. The VGA, BPF, and APF stages use wide-linear-range operational transconductance amplifiers (WLR-OTAs) [9] to improve signal handling capability and dynamic range (DR). The circuit has been designed in the OnSemi 0.5 μm CMOS process. The tunable gain range is 80 dB, and the phase shift range is 0–π. The bandwidth of the LNA is > 1 MHz, while its $1/f$ corner frequency is $\ll 10$ kHz. These values were designed for MEMS resonators in the 10-120 kHz range. However, the design can be easily modified to operate up to several MHz.

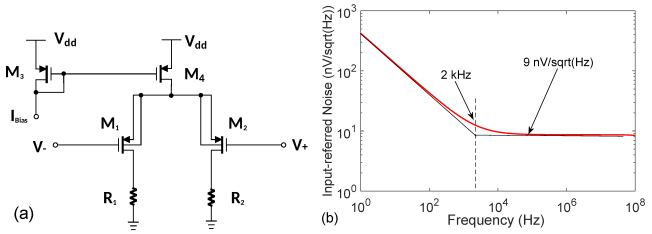

Fig. 2. (a) Schematic of the low-noise amplifier (LNA). (b) Simulated input-referred voltage noise PSD of the LNA.

A. Low-Noise Amplifier (LNA)

A simple resistively-loaded differential-pair topology was used for the LNA (see Fig. 2(a)). High-impedance pseudo-resistor elements (not shown) were used to set the DC common mode level at the input terminals. The input PMOS pair $M_{1,2}$ had large layout area to minimize $1/f$ noise. The input-referred thermal noise PSD of this topology is

$$\overline{v_{ni}^2} = \frac{8k_BT}{g_{m1,2}}\left(\gamma + \frac{1}{A_0}\right), \quad (6)$$

where $g_{m1,2}$ and $\gamma \approx 2/3$ are the transconductance are excess noise parameter of M_1 and M_2, and $A_0 \equiv g_{m1,2}R_{1,2}$ is the DC voltage gain. The first term arises from the transistors, and the second from the resistors. The latter is usually negligible for a well-designed circuit since $A_0 \gg 1$. Ignoring $1/f$ upconversion and other time-varying effects, minimal degradation of close-in phase noise requires

$$\overline{v_{ni}^2} \ll \overline{v_{M,ni}^2(\omega_0)} \;\Rightarrow\; g_{m1,2} \gg 2\gamma\omega_0^2 R_m C_{tot}^2. \quad (7)$$

Since $g_m \propto I_{Bias}$ (in subthreshold) or $\propto I_{bias}^{1/2}$ (above threshold), it is evident that LNA power requirements are a strongly increasing function of the resonant frequency. We set $R_1 = R_2 = 125$ kΩ and realized them using high-resistivity polysilicon to save area and minimize parasitic capacitance. The value of I_{Bias} was set to ensure a low $1/f$ corner frequency of 2 kHz and a thermal noise PSD of $\overline{v_{ni}^2} = 9$ nV/Hz$^{1/2}$, as shown in Fig. 2(b).

B. Wide-Linear-Range (WLR) Amplifier

A WLR-OTA was used as the basic signal-processing element in most of the stages in the feedback network. This circuit (see Fig. 3(a)) is a modified version of the 13-transistor design proposed by Sarpeshkar et. al. [9] and has significantly larger input linear range V_L than typical OTA designs. Increasing V_L is beneficial since thermal-noise-limited $DR \propto V_L$. Our design uses source degeneration and bump linearization to increase V_L, but uses gates (instead of wells) as the input terminals. This change increases input common-mode range; it also simplifies device layout and improves matching, since the input pair can be laid out within the same well. However, it precludes the use of gate degeneration and limits V_L to $\approx 3\phi_T(1 + 1/\kappa)/\kappa \approx 270$ mV in subthreshold (compared to 1.7 V in [9]). Here $\phi_T = 26$ mV is the thermal voltage and

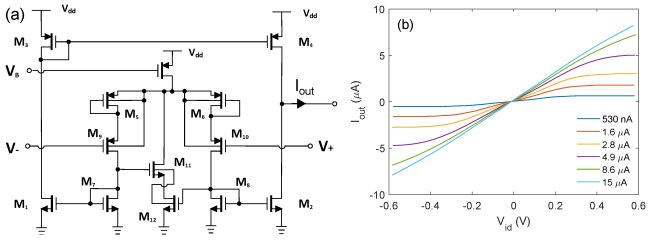

Fig. 3. (a) Schematic of the wide-linear-range (WLR) amplifier. (b) DC simulation of the WLR amplifier.

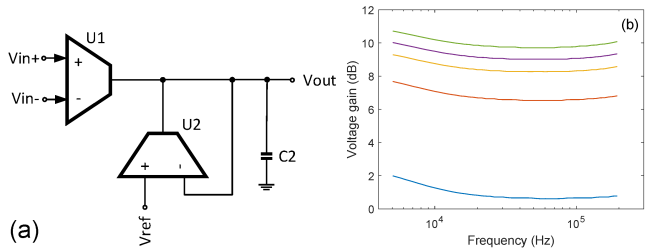

Fig. 4. (a) Schematic of the variable-gain amplifier (VGA). (b) Simulated gain for different bias current ratios.

$\kappa \approx 0.7$ is the subthreshold slope constant. The bulk terminals of the input transistors and the source degeneration diodes are all tied together to minimize the number of different wells, at the expense of increased threshold voltage of the input pair.

Fig. 3(b) shows the simulated I-V curves of the WLR-OTA for various bias currents. The linear range in subthreshold (bias currents < 1 μA) was ~ 300 mV, which is in good agreement with theory. For larger currents the input pair is biased above threshold, which causes V_L to increase.

C. Variable-Gain Amplifier (VGA)

The overall gain $|a(s)|$ is set by three VGAs. Each VGA uses two WLR OTAs (see Fig. 4(a)). The gain is equal to the ratio of the two OTA transconductances (see Fig. 4(b)), and reduces to the ratio of their bias currents, i.e., $G = I_{bias,1}/I_{bias,2}$, if both OTAs operate in subthreshold. The differential input voltage of OTA U2 is given by $(V_{out} - V_{ref})$ and limits the input-referred linear range of this circuit to V_L/G. A small capacitor at the output terminal reduces bandwidth and improves phase margin by ensuring that high-frequency poles generated by internal capacitances of U2 occur beyond crossover. The VGA operates in the 10-100 kHz range while these poles occur in the 1-10 MHz range, so selecting an appropriate bandwidth that does not impact overall performance is not difficult. The amplifier can be operated with differential inputs (as shown), or in single-ended mode where one terminal of U1 is kept at a stable reference voltage.

D. Band-Pass Filter (BPF)

The next stage is a programmable band-pass filter (BPF) to select a particular resonant mode and remove unwanted out-of-band distortion that is commonly introduced by the electro-mechanical transducers used to couple to MEMS devices.

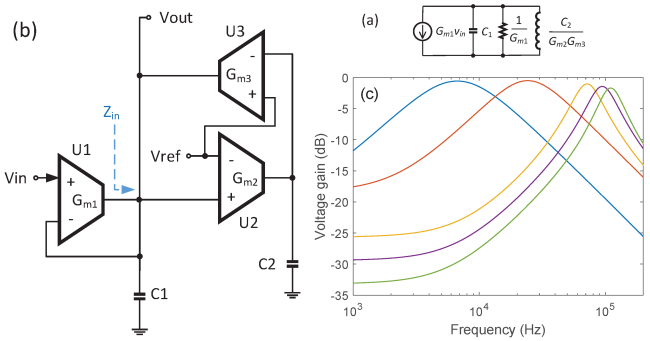

Fig. 5. (a) Equivalent passive RLC prototype of the BPF. (b) Implementation using three WLR OTAs. (c) Simulation for different center frequencies and quality factors.

A fourth-order BPF consisting of two identical second-order sections in cascade is used to improve frequency selectivity. Each section uses three WLR OTAs to implement the passive RLC prototype shown in Fig. 5(a) [10]. On-chip inductors would be impractically large in this frequency range; instead, two OTAs implement a gyrator that inverts the impedance of a capacitor C_2 to create an active inductor of value $L_1 = C_2/(G_{m2}G_{m3})$ (see Fig. 5(b)). The effective filter transfer function is given by $H_{BP}(s) = (s\tau/Q)/\left(s^2\tau^2 + s\tau/Q + 1\right)$, where $\tau = 1/\sqrt{L_1 C_1}$ and $Q = \sqrt{C_1/L_1}/G_{m1}$. Adjusting the bias currents I_{B2} and I_{B3} of OTAs U2 and U3 sets the center frequency $\omega_c = 1/\tau$ (see Fig. 5(c)). For simplicity, we set $I_{B2} = I_{B3}$ and $C_1 = C_2$. The bias current of U1 is then used to set the Q of the filter (values of 3-6 are typical).

The input-referred linear range of the circuit can be found by calculating the transfer function from the input to the differential input voltage $v_d = (v_+ - v_-)$ of each OTA. For U1, we get a band-stop response with a maximum gain of 1 and a null near ω_c:

$$\frac{v_{d1}}{v_{in}} = 1 - H_{BP}(s), \quad \max\left|\frac{v_{d1}}{v_{in}}\right| = 1. \tag{8}$$

For U2 we get $v_{d2}/v_{in} = H_{BP}(s)$, which has a maximum gain of 1. For U3 we get a low-pass response with a maximum gain of $Q\,(G_{m1}/G_{m3})$:

$$\frac{v_{d3}}{v_{in}} = H_{BP}(s)\,\frac{G_{m2}}{sC_2}, \quad \max\left|\frac{v_{d3}}{v_{in}}\right| = Q\left(\frac{G_{m1}}{G_{m3}}\right). \tag{9}$$

The overall linear range of $V_L \times \min\{1, (G_{m3}/G_{m1})/Q\}$ is limited by OTA U3 for large values of Q. This limit can be increased by using well-inputs and other degeneration techniques to further increase the linear range of U3.

E. All-Pass Filter (APF)

A programmable all-pass filter (APF) implements variable phase shift within the feedback network to ensure that the oscillation condition can always be satisfied. An all-pass topology was chosen because a programmable delay-line at this frequency would have consumed much more area in order

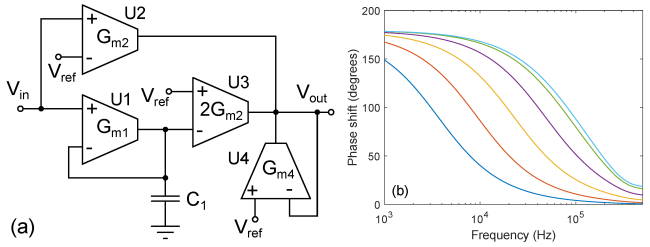

Fig. 6. (a) Schematic of the all-pass filter (APF) or phase shifter. (b) Simulated APF phase shift for various bias currents.

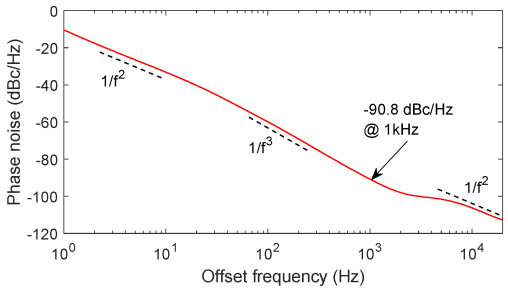

Fig. 7. Simulated phase noise of the closed-loop oscillator. The nominal oscillation frequency was $\omega_0 = 2\pi \times 24.184$ kHz.

to achieve the same level of tunability [11]. The circuit is shown in Fig. 6(a) and has a transfer function of

$$H_{AP}(s) = \frac{G_{m2}}{G_{m4}}\left(\frac{\tau s - 1}{\tau s + 1}\right), \ \tau \equiv \frac{C_1}{G_{m1}}. \qquad (10)$$

The magnitude of $H_{AP}(s)$ is G_{m2}/G_{m4} at all frequencies, while the phase shift is $\theta(\omega) = -2\tan^{-1}(\omega\tau)$. The phase shift decreases monotonically from 0 to π with frequency, and is equal to $\pi/2$ when $\omega\tau = 1$. This point can be varied by adjusting the bias current of U1, as shown in Fig. 6(b). Finally, it is easy to show that the effective input-referred linear range of this circuit is $V_L \times \min\{1, (G_{m4}/G_{m2})\}$.

IV. Simulation Results

The entire design consumes ~30 μA from a 3.3 V supply. Its functionality was verified by performing transient simulations with an equivalent circuit model of a SiC MEMS resonator with electrostatic comb drive, a background subtraction capacitor, and a bond-pad capacitance of 150 fF. Element values within the MEMS model were derived from two-port electrical measurements of the first resonant mode in vacuum. The best-fitting values for a DC bias voltage of 20 V and drive amplitude of 0 dBm were $R_m = 10$ GΩ, $L_m = 40$ MH, $C_m = 1.1$ aF, and $C_p = 28.5$ fF, corresponding to $\omega_0 = 2\pi \times 24.0$ kHz and $Q = 603$. The resulting motional-to-background ratio is only 0.023 (-32.7 dB), which highlights the importance of background subtraction using Z_{comp}. Additionally, the resonant frequencies of the second and third modes were found to be 37.8 kHz and 46.5 kHz with $Q = 260$ and 220, respectively.

The gain, center frequency, and phase shift of the feedback network were adjusted to generate stable near-sinusoidal oscillations around ω_0. The input voltage amplitude to the chip was ~1 mV, and the VGA gains were set such that the output amplitude was ~300 mV. Fig. 7 shows the resulting phase noise of the oscillator. Three distinct regions are visible: offsets $< \omega_0/Q = 40$ Hz have a $1/f^2$ spectrum dominated by thermal noise from the resonator (as desired), offsets between 50 Hz and 2 kHz have a $1/f^3$ spectrum dominated by upconverted $1/f$ noise from the LNA, while offsets > 5 kHz have a $1/f^2$ spectrum dominated by the LNA's thermal noise.

V. Conclusion

A configurable CMOS chip for MEMS-referenced resonators has been designed in the OnSemi 0.5 μm process. It can be interfaced with a variety of MEMS resonators with frequencies in the 10–120 kHz range. This paper has described the design and presented simulation results; chip layout is currently underway. Future work will include an automatic level control (ALC) loop and operation at higher frequencies.

Acknowledgment

The authors would like to thank Jonathan McCandless, Hao Tang, Jaesung Lee, Mohammad Saiful Islam, Liuming Zhao, and Chen Liang for assistance with MEMS resonator measurements and modeling. This work was partially funded by a National Science Foundation Grant (ECCS-1509721).

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