Low-Power Multiplexer Designs Using Three-Independent-Gate Field Effect Transistors

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***Abstract*—Three-Independent-Gate Field Effect Transistors (TIGFETs) are capable of different modes of operation thanks to their additional gate terminals. By electrically controlling their side gates, TIGFETs can act either as a *p*-type or an *n*-type transistor and can also implement multi-threshold logic. This versatility can be used to create compact logic gates intended for high-performance or low-leakage applications. In today's *Integrated Circuits* (ICs), multiplexers are used in a broad range of applications such as encoding-decoding, routing signals or *Look-Up Tables* (LUTs). In particular, conventional *Complementary Metal-Oxide-Semiconductor* (CMOS)-based multiplexers with a large number of inputs require several stages, leading to significant area and energy. Due to their three-gate terminals, TIGFETs can implement the equivalent multiplexers using less transistors, arranged in a compact way, reducing the area and energy. In this paper, we present novel two-level and tree-like multiplexer structures intended for low-power applications based on *Silicon Nanowire* TIGFETs (TIG SiNWFETs) and compare it with conventional CMOS FinFET *Low-STandby Power* (LSTP) structures. Using the 22nm technology node, electrical simulations show that our SiNWFET-based multiplexer can improve the energy by operation by $2.5\times$ and *Energy-Area Product* by up to $2.6\times$ compared to the best CMOS FinFET structures.**

I. Introduction

For many years, the semiconductor industry has continued to scale down the *Metal-Oxide Semiconductor Field Effect Transistors* (MOSFETs) in order to increase the number of transistors per area unit, thus enhancing the performances of *Integrated Circuits* (ICs). Novel transistor topologies have emerged in the past few years as an alternative to planar transistors, such as FinFETs [1]. They allow better electrostatic control, decreased leakage and greatly reduced short-channel effects, improving electrical performances. However, FinFETs still suffer from physical limitations, such as short-channel and quantum effects [2] and can not be scaled indefinitely. Therefore, alternative routes are investigated to enhance the device functionalities with the goal to sustain the need for more powerful ICs.

To this end, for the past few years, several research focused on increasing transistor's capabilities and many devices have been proposed in the recent years [3], [4], [5]. *Multiple-Independent-Gate FETs* (MIGFETs) are promising candidates since they provide more functionalities than conventional *Complementary Metal-Oxide-Semiconductor* (CMOS) by using several gate terminals to independently control the channel region [2], [6]. MIGFETs have been successfully demonstrated in a wide range of applications such as radio frequency [7], optics [8] and digital circuits design [4], [9].

Notably, *Three-Independent-Gate* (TIGFETs) [11] can be dynamically configured as an *n*-type or a *p*-type transistor, during runtime. Moreover, they also allow a dynamic control of the threshold voltage [10], allowing them to be used either for low-leakage or high-performance applications. Thus, TIGFETs have shown promises in arithmetic operators, memory design and multi-V_T design [12].

In today's *Application Specific Integrated Circuits* (ASICs), multiplexers are used in for several applications such a routing structures in *Networks-on-Chip* (NoCs) [13] or for non-trivial logic implementation [14]. In *Field Programmable Gate Arrays* (FPGAs), multiplexers are an essential component since they are used to build routing multiplexers and *Look-Up Tables* (LUTs) [15]. Therefore, in ASICs and FPGAs, datapath signals often go through several layers of multiplexers. As a result, multiplexers have a great impact on delay, power and area [16], [17] and it is crucial to improve them to enhance ICs capabilities.

In this paper, we present novel architectures for multiplexers designs based on TIGFETs and compare it with conventional CMOS structures. Due to their three independent gates, TIGFETs have richer switching capabilities for one given transistor. When two transistors in series are needed in conventional tristate CMOS inverters, TIGFETs only require one transistor, compacting the structure and achieving area as well as energy reduction. We showcase the benefits of the proposed architectures at the 22nm technology node by comparing *Silicon NanoWire TIGFETs* (TIG SiNWFETs) with CMOS FinFET *Low-STandby Power* (LSTP) structures. We target the 22nm technology node because of the large dominance of this node in beyond-CMOS evaluations, allowing the reader to put this work into perspective with respect to other technologies. Nevertheless, similar conclusions can be achieved at other nodes. The proposed TIGFET-based multiplexers reduce energy by $2.5\times$ and *Energy-Area Product* by up to $2.6\times$ compared to the best CMOS architectures.

The rest of this paper is organized as follows: In Section II, we provide the technical background about TIGFETs technology and CMOS multiplexer designs. Section III presents two-level and tree-like multiplexer designs based on TIGFETs. Section IV shows experimental results. Section V concludes

this paper.

II. Technical Background

In this section, we first present the necessary background on TIGFETs multi-threshold technology and review some generalities about conventional CMOS multiplexer circuit design.

A. Operation of TIGFET

TIGFET devices have three independent gate contacts, as shown in Fig. 1: the *Control Gate* (CG) which controls the potential barrier in the channel and the *Polarity Gate at Source* (PGS) and the *Polarity Gate at Drain* (PGD) which modulate the Schottky barriers at source and drain. Those three electrodes allow TIGFETs to operate in several modes, as presented in [18].

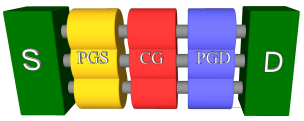

Fig. 1: TIG SiNWFET structure using three vertically-stacked nanowires. The three gates are surrounding the silicon nanowires in a gate-all-around fashion.

In this work, we are interested in the polarity and dual-V_T properties of TIGFETs. The different device configurations under interest are illustrated in Fig. 2. The symbol of a TIGFET is shown in Fig. 2 (a) with its five terminals. When CG is used as a regular gate, the device is configured as a low-V_T *n*-type if PGD and PGS are biased to V_{DD} (Fig. 2 (b)) or as a low-V_T *p*-type if PGD and PGS are biased to G_{ND} (Fig. 2 (c)). If PGS (or PGD) are used to switch the device configuration, the TIGFET is is configured as a high-V_T *n*-type if the two other terminals are biased to V_{DD} (Fig. 2 (d)) or as a high-V_T *p*-type if they are biased to G_{ND} (Fig. 2 (e)).

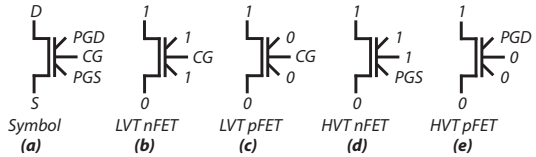

Fig. 2: TIGFET symbol (a) and equivalent logic behaviors (b-e) depending on the gate usage.

TIGFET devices have been implemented with several channel technologies such as FinFET [19], SiNWFET [10] or 2D [20] structures. In this paper, we will consider the TIG SiNWFET presented in [10] whose structure is depicted in Fig. 1. The vertically stacked structure of the TIGFET allows to use several nanowires to determine the driving strength of the device, without affecting its area, at a cost of increased capacitances. This structure provides better electrostatic control over the channel and better scalability properties than FinFETs [21] while being fully compatible with CMOS. In the considered TIGFET structure, the nanowires have a diameter d of 15nm while the length of the gates are both 24nm long. The dielectric layer is HfO_2 with a thickness of 5.1nm and an *Equivalent Oxide Thickness* (EOT) of 0.8nm. These materials were selected to ensure full compatibility with standard CMOS processes. The dual-V_T I-V curves of a single nanowire TIGFET, simulated with TCAD Sentaurus [22], are shown in Fig. 3. The solid lines are the low-V_T configurations and the dashed lines are the high-V_T configuration. The extracted on-curent is about $33.5\mu A$. Note that the on-current is the same for the *n*-type and *p*-type configurations, which is not achievable in CMOS. By using an effective width of πd, the on-current density is $J_{on} = 708.7\mu A/\mu m$. The low-$V_T$ and high-V_T have a threshold difference of $0.3V$. Similarly, the off-current density of the *p*-type is $J_{off} = 31.8pA/\mu m$ for the low-V_T configuration and $J_{off} = 0.53pA/\mu m$ for the high-V_T configuration, leading to a leakage ratio of 60 between the low-V_T and high-V_T *p*-type configurations. Note that while we use a V_{DD} of $1.2V$, which is higher than the nominal voltage of the 22nm technology node ($0.9V$), TIGFET can still achieve significant energy savings, as it will be demonstrated in Section IV.

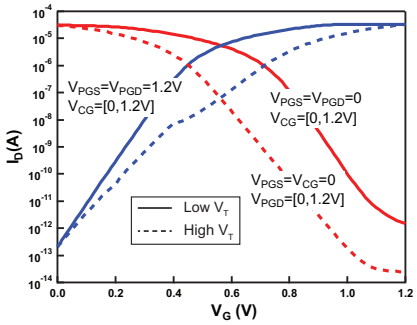

Fig. 3: Simulated I-V curve of a TIG SiNWFET for $V_{DS} = 1.2V$ in logarithmic scale [10].

B. CMOS Multiplexer Designs

Multiplexers are widely used in digital circuits and are typically implemented with static logic (using tristate inverters), pass-transistors or transmission gates [23], as illustrated in Fig. 4 (a-d). In this paper, we consider multiplexers based on transmission-gate over pass-transistors since they perform better in terms of *Area-Delay-Power Product* [24]. When N is small, i.e., $N \leq 4$, static multiplexers are chosen since they have larger noise immunity and lower energy than a transmission-gate counterpart. When $N \geq 4$, multiplexers are traditionally implemented using transmission gates, as it is the case in commercial FPGAs [25]. Depending on the critical parameters, CMOS multiplexers can be built with different architectures in order to optimize delay, area, power, or number of control signals. Transmission-gate multiplexers can be realized in the same way as pass-transistor multiplexer, as introduced in [26], using a one-level, two-level, or tree-like multiplexing structures. The schematics of two-level and tree-like N inputs multiplexers based on static logic and transmission-gate are depicted in Fig. 4 (e) and (f) respectively.

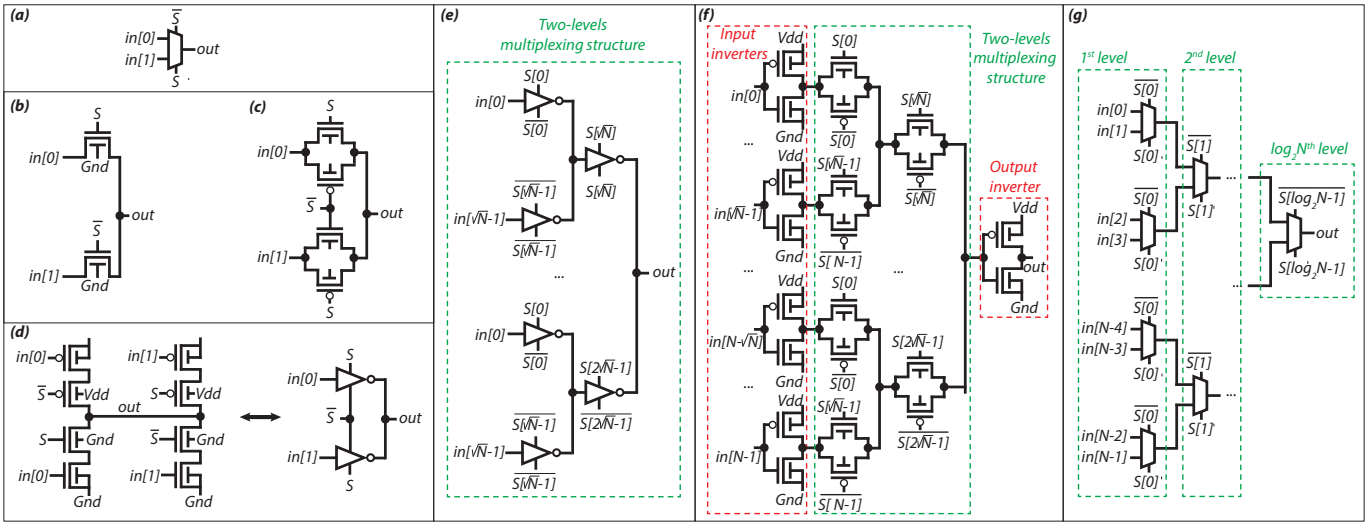

Fig. 4: CMOS multiplexers: (a) 2:1 symbol; (b) 2:1 pass-transistor implementation; (c) 2:1 transmission-gate implementation; (d) 2:1 static implementation; (e) N-input two-level static design; (f) N-input two-level transmission gate design; (f) N-input tree-like

Note that for the transmission-gate multiplexer, input and output inverters are required to restore the signal. In the two-level multiplexer, the first level is grouped in clusters of $\sqrt{N}$ inputs. The second level is therefore composed of $\sqrt{N}$ tristate inverters or transmission-gate. In the tree-like structure, each inputs are grouped together by cluster of 2, and this structure is cascade at each stage. Therefore, $\log_2 N$ levels are required. As explained in [26], the one-level multiplexer has increased performance and lower area when the number of inputs N is small ($N \leq 8$). The parasitic capacitance before the output inverter increasing linearly with N, a large N leads to high delay and energy consumption. Therefore, when N is large ($N \geq 8$), a two-level multiplexer structure performs better in terms of *Area-Delay-Power Product* and in terms of number of control signals. Lastly, tree-like multiplexers perform worse in terms of area, power and delay but are often chosen when the number of input is high ($N \geq 32$), keeping the number of control signals reasonable. In our paper, we will focus on multiplexers with a number of inputs N ranging from 2 to 64.

III. TIGFET-Based Multiplexer

In this section, we introduce the novel TIGFET multiplexer structures. First, we discuss the methodology to decrease the number of transistors compared to CMOS structures. Thereafter, we present one-level, two-level and tree-like static multiplexer structures based on TIGFET devices.

By independently controlling their three gate terminals, TIGFETs can have different operation modes, as explained in the previous section. By biasing one input and controlling the two others, a TIGFET can act as two series transistors, as illustrated in Fig. 5. In Fig. 5 (a), a TIGFET can act as two *n*-type in series by combining the low-V_T and high-V_T *n*-type configurations. In the same way, in Fig. 5 (b), a TIGFET can act as two *p*-type in series by combining the low-V_T and high-V_T *p*-type configurations. More details on this feature of TIGFETs can be found in [10]. Therefore, by using TIGFET, more compact logic gates can be built.

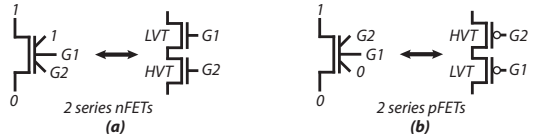

Fig. 5: Bias configuration of a TIGFET for 2 inputs.

As depicted in Fig. 6 (a), a traditional tristate CMOS inverter requires 4 transistors. In order to explain how to implement tristate TIGFET inverters with less transistors, we present in Fig. 6 (b) a naive tristate inverter using TIGFETs, configured as low-V_T *n*-type and *p*-type transistors. To obtain such structure, we simply replaced each CMOS transistor by a TIGFET. Based on this structure, it is possible to derive a more compact tristate TIGFET inverter, using less transistors, as shown in Fig. 6 (c). Indeed, TIGFETs allow us to build tristate inverters with only two devices. As a result, the datapath signal goes through less diffusion capacitances, leading to better energy as it will be demonstrated in the experimental section.

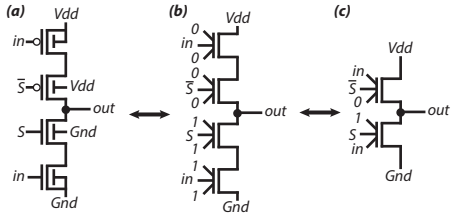

Fig. 6: (a) Tristate CMOS inverter; (b) Naive tristate TIGFET inverter; (c) Proposed tristate TIGFET inverter.

As explained in the background section, CMOS multi-

TABLE I: Area (in μm^2) comparison of N-input CMOS and TIGFET multiplexers

	One-level Static					Two-level				Tree-like			
	CMOS	Naive TIGFET		Compact TIGFET		Static CMOS	Tgate CMOS	Compact TIGFET		Static CMOS	Tgate CMOS	Compact TIGFET	
N	Area	Area	Gain$^{(1)}$	Area	Gain$^{(1)}$	Area	Area$^{(2)}$	Area	Gain$^{(3)}$	Area	Area$^{(2)}$	Area	Gain$^{(3)}$
2	0.65	0.996	-52%	0.664	-15%	0.545	0.654	0.498	9% / 31%	0.545	0.654	0.498	9% / 31%
4	1.308	1.992	-52%	1.328	-15%	1.526	1.417	1.328	15% / 7%	1.526	1.417	1.328	15% / 67%
8	3.379	5.146	-52%	3.818	-12%	3.052	2.834	2.822	8% / 0.4%	3.379	3.052	2.822	20% / 81%
16	6.213	9.462	-52%	6.806	-9%	5.232	4.905	4.648	12% / 5%	6.976	5.995	5.644	24% / 62%
32	11.881	18.094	-52%	12.782	-7%	9.592	9.047	8.300	15% / 9%	14.061	11.990	11.122	26% / 78%
64	24.525	37.35	-52%	26.726	-9%	17.44	16.677	14.608	19% / 14%	28.122	23.653	21.921	28% / 79%

(1) Compared to CMOS. (2) Input, output and restoring inverters are taken into consideration for the area computation. (3) Compared to Static CMOS / Transmission-gate CMOS.

plexers can be implemented with static logic using tristate inverters. By using tristate TIGFET inverters, several multiplexer structures, i.e., one-level, two-level or tree-like structure can be built. Our TIGFET-based multiplexer structures are very close to the traditional CMOS counterparts. Indeed, a one-level TIGFET multiplexer is built with several tristate TIGFET inverters in parallel. For a two-level multiplexer, the structure is the same as for the CMOS (Fig. 4 (e)) except that tristate TIGFET inverters are used. The tree-like TIGFET multiplexer is built by cascading several 2-input static TIGFET multiplexers, whose schematic is depicted in Fig. 4 (d). Fig. 7 shows the schematics of the proposed one-level and two-level 4-input static TIGFET multiplexers. Similarly to the CMOS counterpart, the delay and energy of the one-level structure are expected to scale linearly with N since the output parasitic capacitance is directly proportional to N. For the two-level and tree-like structures, energy improvements are expected since the parasitic capacitances are less dependent on N thanks to the reduced number of transistors per stack. This also leads to a smaller area, as shown in Table I.

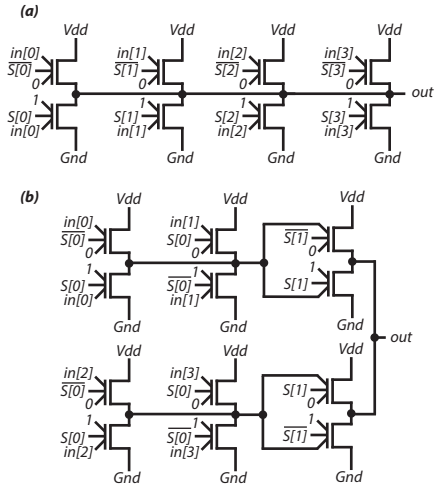

Fig. 7: 4-input static TIGFET multiplexer: (a) one-level; (b) two-level.

IV. Experimental Results

In this section, we demonstrate the benefits of our novel TIGFET multiplexer structures. We first introduce our experimental methodology and then evaluate the performances of TIGFET and CMOS for several multiplexer design styles.

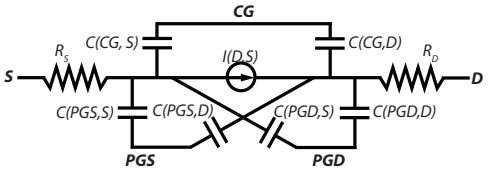

Fig. 8: Equivalent RC circuit of a SiNWFET

A. Experimental Methodology

For circuit level simulations, a VerilogA table model from [10] has been used for the TIGFET. The model equivalent circuit is depicted in Fig. 8. The source drain current values have been extracted from Sentaurus TCAD simulations as discussed in section II. Capacitance values have been extracted from TCAD simulations as an average value under all possible bias configurations to model intrinsic capacitances of the device. Interconnect capacitances were not considered in this evaluation for both TIGFETs and FinFETs. Nevertheless, since the constraints on routing (number of inputs and control signals) is similar between these two designs, considering interconnect will simply shift the results but not change their relative comparisons. For more details about physical design with TIGFETs, we refer the reader to [27]. Resistance R_S and R_D have been estimated according to the TIGFET geometry. The supply voltage used for the TIG SiNWFETs is 1.2V. We consider one nanowire per stack. The *Predictive Technology Model* (PTM) 20nm-FinFET *Low-STandby-Power* (LSTP) [28] is used in the circuits of the CMOS multiplexers. Inverters and pass-transistors are minimum sized. They have a nominal supply voltage $V_{DD} = 0.9V$. Delay and energy per transition results are extracted from HSPICE simulations [29].

Area estimation uses the same methodology than in [10], based on the number of transistors of each multiplexer design and according to the 22-nm FinFET design rules [30].

B. One-level Static Multiplexers Comparison

Fig. 9 (a), (b) compare the delay and energy of one-level multiplexers, using standard CMOS design, naive CMOS-inspired TIGFET design and the proposed compact TIGFET design, for a different number of inputs N. The naive one-level static TIGFET design suffers from much larger delay

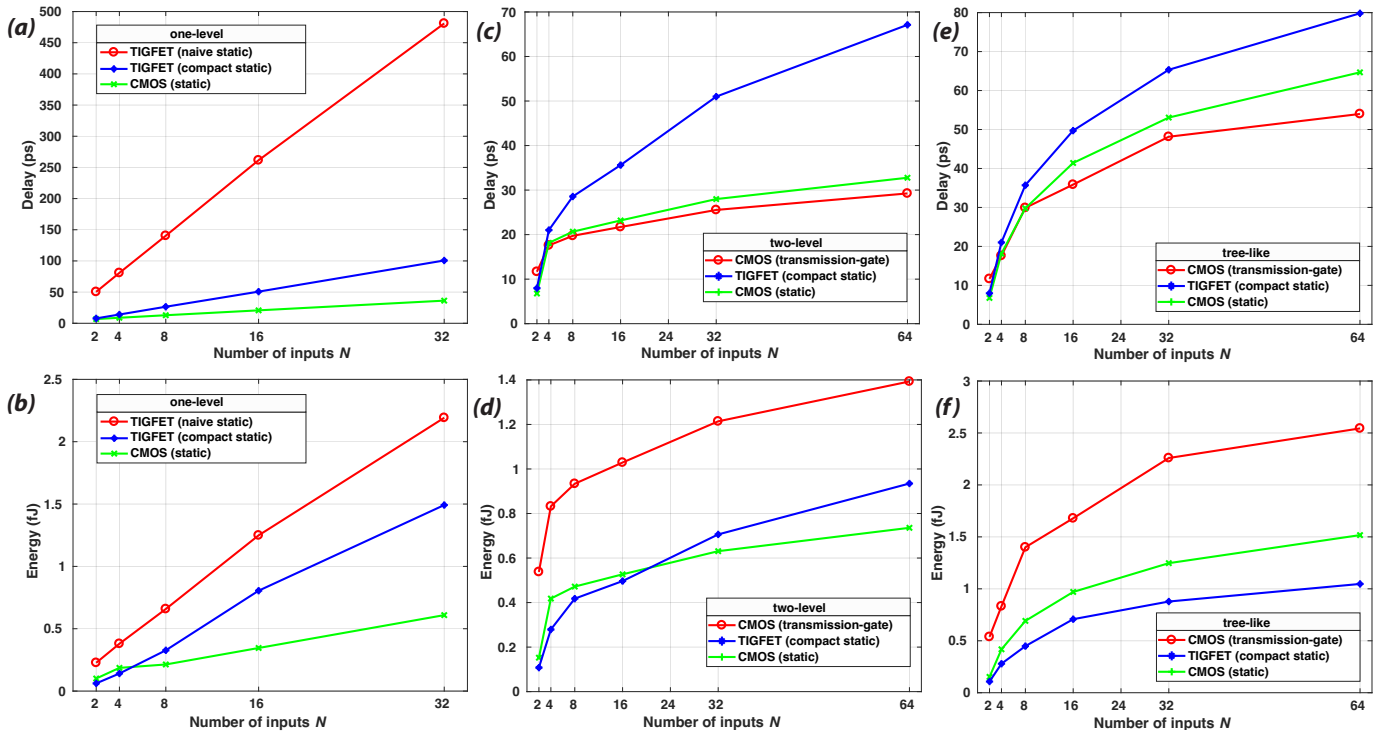

Fig. 9: Delay and energy comparison between CMOS and TIGFET-based multiplexers: (a), (b): one-level static multiplexers (CMOS, naive TIGFET and proposed TIGFET), (c), (d): two-level multiplexers (transmission-gate CMOS, static CMOS and static TIGFET), (e), (f): tree-like multiplexers (transmission-gate CMOS, static CMOS and static TIGFET).

compared to the one-level static CMOS design due to the lower current density of a TIGFET compared to a CMOS transistor. Conversely, the compact one-level static TIGFET multiplexer has an improved scalability compared to the naive structure, bridging the gap with the one-level static CMOS multiplexer. The energy savings between the two TIGFET designs comes from the lower diffusion capacitance of a single TIGFET compared to two stacked TIGFET. The compact TIGFET multiplexer even outperforms a static CMOS design in term of energy for a small number fo inputs. For $N = 2$ ($N = 4$), it reduces energy by 63% (31%) as compared to the one-level static CMOS multiplexer. By cascading such kind of multiplexers to build larger ones, energy savings can be achieved, as it will be shown in the next subsection. For the rest of this paper, we refer to the compact static TIGFET design simply as static TIGFET design.

C. Two-level Multiplexer Designs Comparison

Fig. 9 (c), (d) studies the delay and energy of two-level multiplexers, for different number of inputs N. The considered designs are based on transmission-gate CMOS, static CMOS and static TIGFET designs. Note that, while the TIGFET design consumes more energy than the static CMOS design, for $N \geq 32$, it requires half as many transistors, leading to a lower area (15% lower) and slightly better *Energy-Area Product* (EAP) (6% better) for $N = 64$. In addition, in spite of a lower performance, TIGFET design is more energy efficient than transmission-gate CMOS design, which are traditionally used when the number of inputs N is large, as explained in Section II, no matter the number of inputs N. For instance, compact two-level TIGFET can bring up to 50% energy saving when $N = 64$, compared to two-level transmission gate multiplexer design.

D. Tree-like Multiplexer Designs Comparison

Fig. 9 (e), (f) present the delay and energy of tree-like multiplexers using static CMOS, transmission-gate CMOS and static TIGFET designs. Tree-like static TIGFET multiplexer can bring up to 2.5× energy savings compared to the tree-like transmission-gate CMOS multiplexer and up to 1.5× compared to tree-like static CMOS multiplexers, at a cost of lower performances. For the tree-like structure as well, the TIGFET design consumes less area than the static CMOS and transmission-gate CMOS (up to 8% and 28% respectively), as shown in Table I, leading to a better EAP of 1.86× and 2.6× respectively.

E. Baseline Comparison Between CMOS and TIGFET Multiplexers

As explained in section II, different multiplexer structures are used, in order to trade-off area, delay and power, motivating us to consider the right baseline design style for a given N. For a small number of inputs ($N \leq 4$), one-level static CMOS multiplexers are used as baseline since they perform better in delay and energy. When ($4 \leq N \leq 16$), two-level transmission-gate CMOS multiplexers are used as baseline

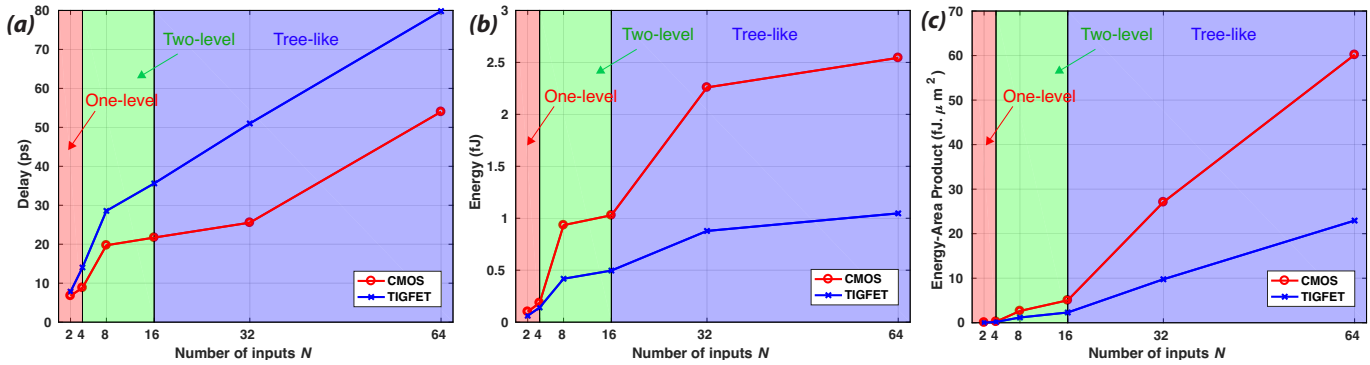

Fig. 10: Comparison between CMOS and TIGFET multiplexers: (a) Delay; (b) Energy; (c) Area-Delay-Power product.

since they achieve the best performance with a reasonable number of control signal. Finally, when ($N \geq 16$), tree-like transmission-gate multiplexers are traditionally chosen since two-level structures would require too many control signals, leading to an unacceptable overhead from the control circuits. As shown in Fig. 10, even if CMOS structures outperform TIGFET structures in terms of delay due to a better current density, TIGFET multiplexers bring significant energy savings (up to $2.5\times$) and achieve a better EAP (up to $2.6\times$) compared to CMOS multiplexers. In addition, due the low-leakage of TIGFET devices, TIGFET multiplexers can achieve low standby power compare to its CMOS counterparts. For $N = 64$, leakage of compact tree-like TIGFET multiplexer was about 217 pA while leakage of tree-like transmission-gate CMOS multiplexer was about 964 pA, leading to a $4.4\times$ lower leakage further showcasing the benefits of the TIGFET technology.

V. Conclusion

In this paper, we proposed novel multiplexer architectures, intended for low-power applications exploiting TIGFET devices. Electrical simulations showed that, at the 22nm technology node, our TIGFET multiplexer can improve the energy efficiency by up to $2.5\times$ and the *Energy-Area Product* by up to $2.6\times$ compared to the best CMOS multiplexers, working at their respective nominal voltage.

Acknowledgments

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