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Polarity-controllable 2-dimensional transistors: experimental demonstration and scaling opportunities

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***Abstract*— This paper reports on the experimental demonstration of polarity-controllable devices fabricated on 2D-WSe_2, achieving high *on/off* ratio and low leakage floor. Following these results, we use ballistic self-consistent quantum simulations to study the scaling trends and benchmark the performances of polarity-controllable devices realized with undoped mono- and bi-layer 2D materials. We show that polarity-controllable devices can scale down to 5nm gate lengths, while showing performances comparable to the ones of 2-dimensional, unipolar, physically-doped transistor. Thanks to their peculiar switching properties polarity-controllable devices enable the design of compact logic gates, leading to higher computational densities with respect to standard CMOS.**

I. Introduction

Conventional CMOS logic circuits are based on doped, *n* or *p*, unipolar devices. With physical gate lengths as small as 14nm in modern devices, doping processes have become increasingly complicated to control [1]. Very abrupt doping profiles are needed, and due to random fluctuations of the number of dopants in the channel, device variability has been increasing, *i.e.* fluctuations in the dopant number causes shifts in the threshold voltage value [1]. A device concept that does not require any doping would thus be highly desirable for new generation electronic devices, and 2-dimensional semiconducting *Transition Metal Di-chalcogenide* (TMDCs) materials provide an excellent platform for its exploration. 2D-TMDCs have recently drawn considerable attention as viable candidates for flexible and beyond-CMOS electronics [2-6] thanks to their physical and electrical properties. The key enabler for the concept of polarity-controllable devices is the exploitation and control of the inherently ambipolar behavior, also known as ambipolarity, of *Schottky-barrier Field Effect Transistors* (SB-FETs). Both electrons and holes can be injected in the intrinsic device channel depending on the voltage applied to the gate. Ambipolarity is usually considered a drawback in standard CMOS devices and is suppressed thanks to the doping process that creates strictly unipolar devices. In polarity-controllable devices instead, the polarity is not set during the fabrication process, but it can be dynamically changed thanks to an additional gate, named program gate (PG). The PG modulates the SB at source and drain, and therefore enables to select the carrier type to be injected into the device at runtime. In principle, no dopant implantation is required in the fabrication process of the device, thus there is no need for the separate development of n and p-type device, to the benefit of fabrication simplicity and device regularity. Here, we report on WSe_2 polarity-controllable devices with *on/off* currents ratio $>10^6$ for both electrons and holes conduction [7], and we study scaling trends with quantum transport simulations for ultra-scaled polarity-controllable devices [8]. We concluded that 2D-TMDCs with an energy bandgap of ~0.8eV could provide a successful scaling path for this technology. For the simulated MX_2 material, we showed $I_{on} > 10^3$ μA/μm and $I_{on}/I_{off} > 10^5$ down to L_G=5nm for both *p*- and *n*-type polarities.

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II. Experimental Results

We used mechanically exfoliated multilayer WSe_2 (7.5 nm thick), that was transferred and aligned on a substrate where buried metal lines were used as PG while the silicon substrate was used as CG (Fig. 1a). The metal contacts (Ti/Pd) were evaporated and provided a band-alignement suitable for the injection of both charge carriers (near mid-gap contacts). The ambipolar behavior of the device can be seen in Fig. 1b, where the PG and CG gates where kept at the same potential during the voltage sweep.

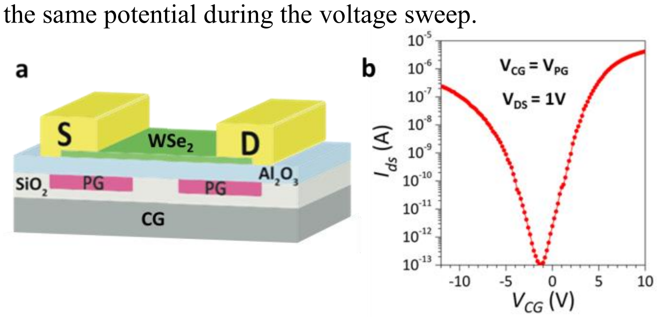

Figure 1. (a) 3D schematic of the fabricated devices. (b) Ambipolar transfer characteristics measured with no bias voltage applied to the PG.

When using the two gates independently, the transistor polarity could be dynamically changed by the PG, while the CG controlled the *on/off* status of the device (Fig. 2). The experimental transfer characteristics measured showed a *p*-type behavior for V_{PG}<-6V, Fig. 2a, while *n*-type conduction properties are shown for V_{PG} >4V, Fig. 2b, on the same device. I_{on}/I_{off} ratios of 10^7 and 10^6 were achieved for *n*-type and *p*-type operation respectively [7].

III. Quantum Simulations of Scaled Devices

To explore the potentials and limitations of these devices, have simulated further scaled devices based on the schematic presented in Fig.3, where HfO_2 (κ=25, EOT=0.47nm) was used as gate dielectric in a *Double-Independent-Gate* (DIG) structure.

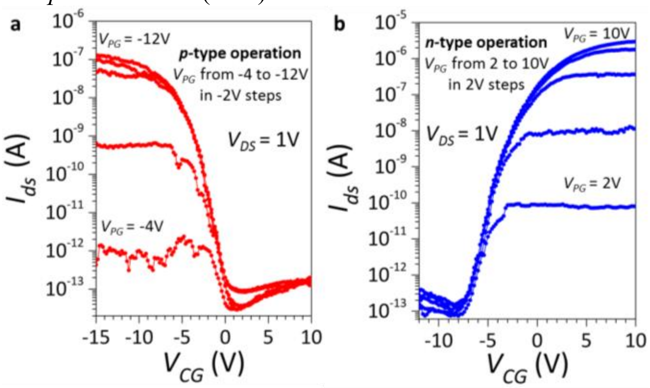

Figure 2. (a) Transfer characteristics of the device obtained for negative bias of the PG, showing p-type beahvior and complete subpression of n-current. (b) Transfer characteristics of the device obtained for positive bias of the PG, showing n-type beahvior and complete subpression of p-current.

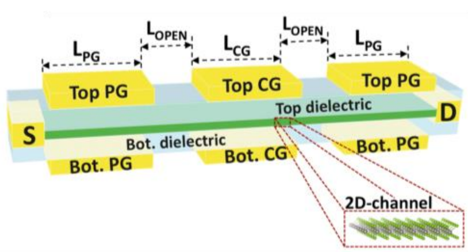

Figure 3. 3D schematic of the simulated polarity-controllable double-gated devices.

No doping was introduced at source and drain contacts and we assumed mid-gap Schottky barrier contacts, to achieve a symmetric behavior of the n- and p- branch. We performed self-consistent ballistic simulations, iteratively solving Poisson and Schrödinger equation (within the NEGF formalism), with an open-source quantum transport code [9]. We used a 2-band tight-binding Hamiltonian to model the conduction and valence band of the 2D-material. The model was extended from monolayer to bilayer 2D materials by adding an interlayer hopping parameter in the effective-mass Hamiltonian, to account for coupling between the two layers [10]. Bilayer (2L) WSe_2 was studied as a channel material. 2L-WSe_2 is reported to show a bandgap of ~1.1 eV [11], which is considerably reduced with respect to the ~1.5eV [12] bandgap of monolayer (1L) WSe_2. The smaller bandgap translates in a lowering of the Schottky barriers at the contacts (ϕ_{SB} = 0.55eV), which enables a more efficient carrier injection. Combined with the extra mobile charge provided by the additional layer, we expect 2L-WSe_2 to show better performances than 1L-WSe_2 for polarity-controllable devices. We studied the device switching properties by fixing the bias on the PG, thus fixing its polarity, and sweeping the CG applied voltage. The ON-currents extracted from the simulated transfer characteristics are ~300 µA/µm, and there is an excellent control on the device *off* state with I_{off} well below 10^{-3} µA/µm, providing $I_{on}/I_{off} > 10^6$ down to L_G=4nm. However, the I_{on} of the device is still too low with respect to what is foreseen for unipolar doped 2D-transistors (I_{on}~2mA/µm) [13]. To increase the performances of the device, and provide a successful scaling path, we need to use a 2D channel material with a lower energy bandgap, thus lowering the height of the Schottky barriers at source and drain. Theoretical calculations [14-16] have shown that several materials, such as ZrS_2, HfS_2, $HfSe_2$, etc., have a lower semiconducting band-gap (0.7-0.9eV) and could prove to be well suited for application in SB-DIG FETs. Based on these theoretical analyses, we modelled a 2D-material (with E_G=0.8eV) and studied its potential application as a semiconducting channel in polarity-controllable FETs. Fig. 4 shows the transfer characteristics for *n*- and *p*-type behavior at different L_G. Thanks to the lower Schottky barrier height at source and drain (ϕ_{SB} = 0.4 eV) the I_{on} is increased to ~1.5 mA/ µm, while I_{off} is well below 10^{-2} µA/µm down to L_G = 5 nm. The I_{on}/I_{off} ratios are above 10^5 down to L_G = 5nm for both *n*- and *p*-type behavior, showing a successfull scaling path that matches the objectives stated in ITRS [17].

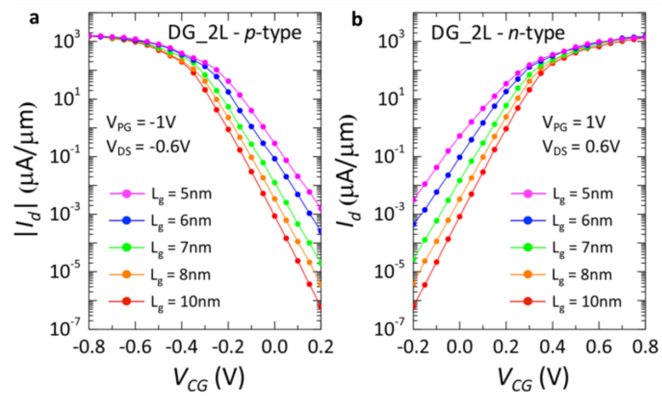

Figure 4. (a) Simulated transfer characteristics of p-type and (b) n-type FET. The gate length is varied from 10 nm down to 4 nm

References

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