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Optimized pulsed write schemes improve linearity and write speed for low-power organic neuromorphic devices

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Abstract

Neuromorphic devices are becoming increasingly appealing as efficient emulators of neural networks used to model real world problems. However, no hardware to date has demonstrated the necessary high accuracy and energy efficiency gain over CMOS in both (1) training via backpropagation and (2) in read via vector matrix multiplication. Such shortcomings are due to device non-idealities, particularly asymmetric conductance tuning in response to uniform voltage pulse inputs. Here, by formulating a general circuit model for capacitive ion-exchange neuromorphic devices, we show that asymmetric nonlinearity in organic electrochemical neuromorphic devices (ENODes) can be suppressed by an appropriately chosen write scheme. Simulations based upon our model suggest that a nonlinear write-selector could reduce the switching voltage and energy, enabling analog tuning via a continuous set of resistance states (100 states) with extremely low switching energy (~170 fJ $\cdot$ μm^{-2}). This work clarifies the pathway to neural algorithm accelerators capable of parallelism during both read and write operations.

Keywords: neuromorphic computing, resistive memory, organic electronics, neural network, symmetric cycling, PEDOT:PSS, electrochemical organic neuromorphic device

Supplementary material for this article is available online

(Some figures may appear in colour only in the online journal)

Introduction

Neural networks are increasingly utilized for traditionally difficult computational tasks such as image classification [1, 2], speech recognition [3, 4], and language translation [5, 6]. However, neural algorithm performance has quickly become limited by computationally demanding networks, such as in deep learning, that can require as many as 10^8 synaptic weights to represent the connection strength between neurons in a network. One strategy is to develop dedicated hardware, such as GPU clusters, that are optimized to efficiently execute core neural algorithms [7–9]. However, any digital architecture will be inherently limited by the energy costs to transmit data between CPU and memory. This has led to interest in neuromorphic computing architectures that outperform traditional CPU and GPU hardware when implementing neural network algorithms and could provide improvements in computation speed and energy (factors of 10^2–10^5) [10]. One example is resistive memory devices with multi-level resistance states that emulate synaptic weights in a crossbar array, forming a

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dot product engine (DPE) [11, 12]. DPEs are capable of performing analog vector matrix multiplication (VMM), one of the most computationally intensive steps in neural algorithms, in a single compute cycle, thus greatly reducing the latency and energy of computation. Furthermore, an ideal DPE can accelerate both read and write by implementing massive parallelism, where simultaneous pulses to all of the rows and columns of the array can either read out or program conductance states in a single operation [13].

Recently, DPEs have been demonstrated to achieve accuracies of 89.9% when recognizing handwritten digits using filament forming memristors [14]. To achieve this classification accuracy, however, requires feedback programming schemes where each device in the array is iteratively read and programmed to get the desired weight, eliminating the write parallelism necessary for highly efficient analog programming [13]. To achieve acceleration for both read and write operations, a 'blind update' scheme (not requiring an additional read) is preferred, where symmetric voltage write-pulses of constant magnitude are applied to the array to achieve a linear change in conductance of the memristive element [15]. Therefore, a new memristive device that has a symmetric and linear response to uniform programming pulses should be implemented to avoid complex programming schemes and benefit from parallel programming in a crossbar array.

Recently, an electrochemical neuromorphic organic device (ENODe), a three-terminal memristive device that uses ionic currents to control the oxidation state of a semiconducting polymer channel, has been demonstrated [16–18]. The advantage of the ENODe architecture is the high-density of ionic doping sites in the conductive polymer which enables virtually-continuous analog conductance tuning [19]. An ENODe consists of an electrochemically active gate electrode used to drive ion exchange between an electrolyte and a doped semiconducting polymer channel (figure 1(a)). The gate voltage controls the electronic carrier concentration, thus modulating the channel conductance (G_{ENODe}). The low energetic barrier for ion migration between the electrolyte and the channel results in low minimum programming energies (e.g. 390 pJ·mm^{-2}) [19]. Although the three-terminal architecture presents a challenge for device integration (see supplementary figure 1 for more details (stacks.iop.org/JPhysD/51/224002/mmedia)), the low switching energy and high number of resistance states make ENODes a promising candidate for low-power neuromorphic computing.

Here, we analyze the performance of ENODes when they are programmed using square voltage pulses as the programming input. We describe a staightforward ionic circuit model to describe the ENODe charge state as a function of input pulses to the gate. The circuit model is used to extract equivalent circuit parameters for aqueous-electrolyte-based ENODes, and is expected to be applicable to all-solid-state ENODes and other, e.g. inorganic, non-volatile electrochemical neuromorphic devices [20]. We demonstrate that asymmetric nonlinearities can be reduced by implementing appropriate programming conditions in order to utilize parallel programming schemes, while maintaining low power consumption during write operations. The presented model focuses on individual devices, not accounting for circuit parasitics that may arise in an integrated crossbar array which could be incorporated into our model in the future. We conclude by using our proposed model to outline the critical materials parameters when designing next generation ENODe materials.

Methods

ENODe preparation

Device fabrication consists of cleaning 2 cm × 2 cm polished indium–tin oxide (ITO) coated glass slides (Xin Yang Technology LTD) with soap, acetone, methanol, and ethanol. Next, PEDOT:PSS (Hereaus, Clevios PH 1000) aqueous solution is prepared by adding 6 v/v % Ethylene Glycol (EG, Sigma Aldrich) to increase the PEDOT:PSS conductivity, 0.1 v/v % Dodecyl Benzene Sulfonic Acid (DBSA, Sigma Aldrich) as a surfactant, and 1 v/v % (3-glycidyloxypropyl) trimethoxysilane (GOPS, Sigma Aldrich) as a crosslinking agent to improve mechanical stability. PEDOT:PSS solution is spun on the ITO slide at 1000 RPM for 2 min and baked at 120 °C for 20 min. To prepare the ENODe channels, PEDOT:PSS films were placed in a sealed glass chamber and vapor-doped by heating polyethyleneimine (PEI, Sigma Aldrich) on a hotplate (Thermo Scientific) at 250 °C for 5 min. A PEI/PEDOT:PSS film and PEDOT:PSS film (L = 11 mm, W = 14 mm, A = 154 mm^2) are placed adjacent to each other with a PDMS well (3M) defining the channel and gate of the device, respectively, and are connected with an aqueous electrolyte (100 mM NaCl).

Pulsed measurements

Pulsed measurements were carried out with a Keithley 2612B source-measure unit with custom LabView code. Devices were programmed through a limit resistor (R_{limit}) with a symmetric write-pulse amplitude (V_{pulse}) using square pulses with a programmable pulse duration (t_{pulse}), pulse delay (t_{delay}), and number of positive and negative pulses (n).

MATLAB code and model fitting procedure

All Keithley parameters are fixed to those used in experiment. ENODe parameters (capacitance C_{ENODe}, charge-transfer resistance R_{ct}, and electrolyte resistance R_{el}, see figure 1(b)) were obtained by iteratively fitting the model to the experimental data by least-squares using custom MATLAB code. The fit is global, i.e. the entire pulse cycling sequence (multiple up/down cycles, e.g. see figure 1(c)) are fitted simultaneously to determine C_{ENODe}, R_{ct}, and R_{el} for a single ENODe. The model was verified by varying V_{pulse}, t_{pulse}, and R_{limit} in experiment, and fitting the model to the experimental data, resulting in similar ENODe parameters. For our simulations, we use the average of C_{ENODe}, R_{ct}, and R_{el} device parameters for the various tested conditions.

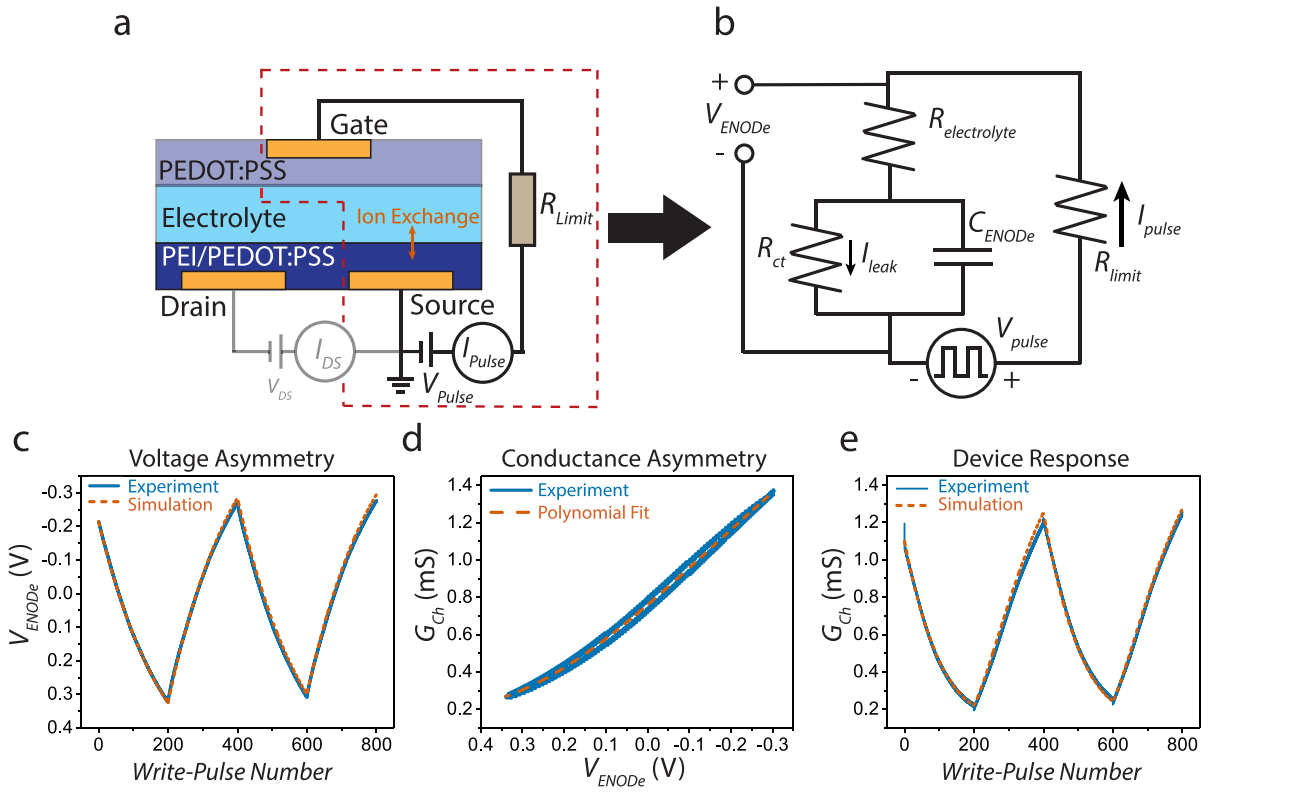

Figure 1. ENODe circuit model: (a) schematic of the ENODe measurement setup and (b) equivalent circuit model. (c) First, the circuit elements C_{ENODe}, R_{el}, and R_{ct} are obtained by fitting the experimentally determined voltage across the ENODe V_{ENODe} under pulsed conditions, then (d) the relationship between V_{ENODe} and conductance G_{ENODe} is fit using a 3rd order polynomial. (e) The simulated V is then input into the polynomial describing G_{ENODe} versus V_{ENODe} to reproduce the conductance response of the ENODe channel to input pulses.

Results and discussion

Equivalent circuit model

Figure 1(a) shows a schematic of an ENODe with a limit resistor ($R_{limit} = 1$ MΩ) to prevent discharge between programming pulses. Figure 1(b) shows the corresponding circuit model used in the simulations, where R_{el} represents the electrolyte resistance, C_{ENODe} represents the mutual capacitance between the gate and channel, and R_{ct} represents the equivalent resistance describing faradaic current from undesired redox reactions at the channel/electrolyte interface. Figure 1(c) shows that our model can successfully reproduce experimental device cycling data spanning hundreds of potentiation/depotentiation (up/down) write pulses. The dataset in figure 1(c) corresponds to a measurement using a series of 100 square pulses with pulse amplitude $V_{pulse} = 2$ V, pulse duration $t_{pulse} = 1$ s, and delay between pulses $t_{delay} = 1$s. We verified our model by varying the experimental conditions V_{pulse}, t_{pulse}, and/or R_{limit}, and in all cases we could successfully fit the experimental data.

In the circuit simulation, the voltage across the ENODe (V_{ENODe}), i.e. the voltage between the gate and source, is computed by integrating the current flowing into/out of C_{ENODe} during continued pulsing. To fit simulations to measured data, we measure the gate current (I_{GS}) during off pulses ($V_{app} = 0$ V) and compute V_{ENODe} using Ohm's Law:

$$V_{ENODe} = I_{GS} * R_{limit}. \quad (1)$$

The result is plotted in figure 1(c). The simulation is iteratively fit to experiment by a least-squares method to accurately obtain the fit parameters (C_{ENODe}, R_{el}, and R_{ct}) describing the ENODe equivalent circuit. We perform this procedure for varied experimental parameters (V_{pulse}, t_{pulse}, R_{limit}) and take their average to obtain $C_{ENODe} = 4.06 \pm 0.24$ μF·mm^{-2}, $R_{el} = 228 \pm 62$ Ω, and $R_{ct} = 274 \pm 87$ MΩ·mm^2 for a PEDOT/PEI:PSS ENODe. We will later discuss how these channel properties affect ENODe write speeds and switching energy.

The modeling illustrates two sources of asymmetric nonlinearity (ν) when cycling ENODes with a uniform write pulse input: (1) voltage asymmetry (figure 1(c)) and (2) channel conductance asymmetry (figure 1(d)). Voltage asymmetry is the result of the voltage division between the limit resistor and the parallel RC component of the ENODe; as C_{ENODe} is charged, the voltage across R_{limit}, and therefore the programming current (I_{pulse}), decreases. This decrease leads to reduced charging of C_{ENODe} with successive programming pulses, giving rise to the tapered shape of the V_{ENODe} versus pulse number as shown in figure 1(c). The conductance asymmetry is an ENODe materials property: as holes in the organic channel are removed, further de-doping of the channel becomes increasingly difficult, possibly related to the shape of the material's density of states [21] or changes in the charge

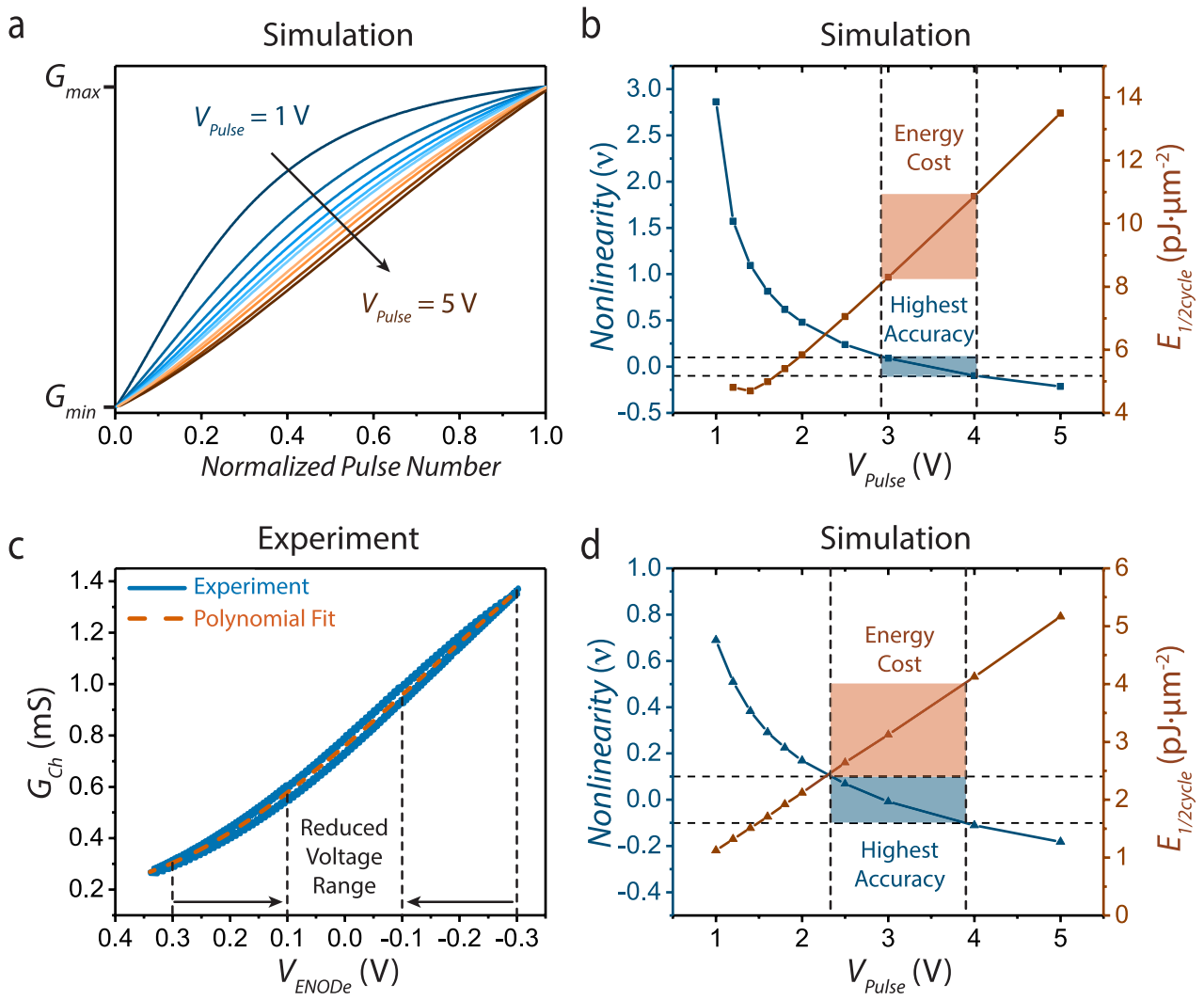

Figure 2. Minimizing ENODe asymmetric nonlinearity (ν): (a) conductance versus pulse number for ENODes programmed with increasing pulse amplitude V_{pulse}, (b) asymmetric nonlinearity ν and half-cycle energy $E_{1/2\ cycle}$ versus V_{pulse}. (c) By limiting the conductance range utilized, (d) $E_{1/2\ cycle}$ and V_{pulse} can be reduced at the cost of a smaller synaptic weight range. Dashed lines in (b) and (d) indicate the desired linearity for a neural algorithm accelerator ($-0.1 < \nu < 0.1$) [23].

carrier mobility [22]. The combination of the voltage asymmetry and conductance asymmetry leads to the 'shark-fin' shape seen in figure 1(e), which is undesirable when applying a blind-update programming scheme [23]. In the next section, we describe how nonlinearity can be minimized by tuning the write pulse and external circuitry.

Minimizing asymmetric nonlinearity by increasing pulse amplitude

To quantify the linearity of the simulated G_{ENODe} versus write pulse number response plotted in figure 2(a), we fit our data according to the definition of asymmetric nonlinearity from [23, 24] for each V_{pulse}:

$$G = G_1\left(1 - e^{-\nu P}\right) + G_{min} \tag{2}$$

$$\text{where} \quad G_1 = \frac{G_{max} - G_{min}}{1 - e^{-\nu}} \tag{3}$$

where G is the device conductance as a function of the normalized number of programming pulses (P), G_{max} and G_{min} are the maximum and minimum conductance state, respectively, and ν is the parameter characterizing asymmetric nonlinearity (ν closer to 0 is more linear). The absolute number of pulses is normalized to fit the form of equations (2) and (3) describing ν. Although increasing V_{pulse} reduces nonlinearity (figure 2(a)), it also increases the energy cost. To quantify both effects and find the optimum write scheme, we compute the energy cost per cycle for each programming scheme using:

$$E_{switch} = \int_0^{t_{pulse}} f * \frac{V_{pulse}^2}{R_{Limit}} * dt \approx f * \frac{V_{pulse}^2}{R_{Limit}} * t_{pulse} \tag{4}$$

$$E_{1/2cycle} = \sum_1^n E_{switch} = f * \frac{V_{pulse}^2}{R_{limit}} * t_{pulse} * n \tag{5}$$

where $E_{1/2\ cycle}$ is the total switching energy to span the desired conductance range of the ENODe, E_{switch} is the energy to

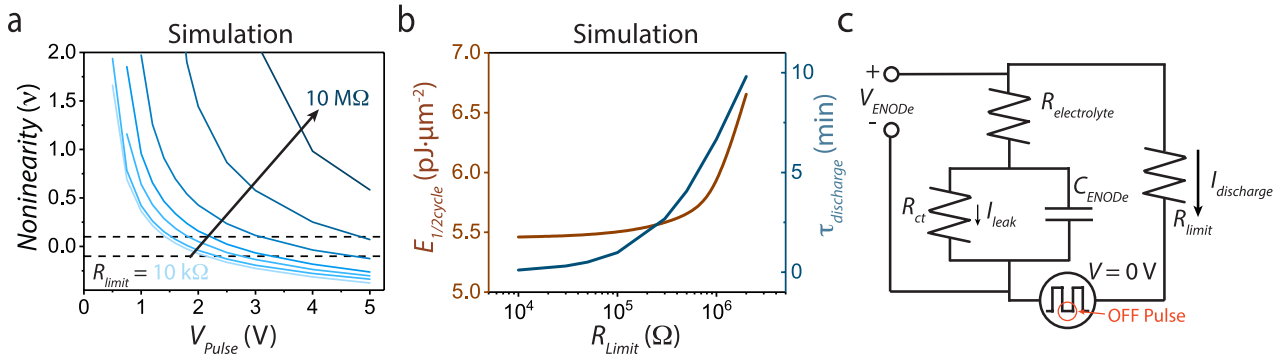

Figure 3. Simulating varied limit resistance R_{limit}: (a) nonlinearity as a function of pulse amplitude V_{pulse} for ENODes with increasing R_{limit} (from light blue to dark blue) when cycled between ±0.3 V, (b) half-cycle energy consumption $E_{1/2\ cycle}$ as a function of R_{limit} for a fixed $V_{pulse} = 3$ V. (c) Schematic showing discharge pathway for low R_{limit} values between programming pulses.

switch the device to an adjacent state, n is the number of states that span the dynamic range of the ENODe, and f is the fraction of I_{pulse} traveling through C_{ENODe}. Figure 2(b) compares the v and $E_{1/2\ cycle}$ as a function of V_{pulse}. The dashed lines highlight the region that satisfies the required linearity for high accuracy neural algorithm accelerator ($-0.1 < v < 0.1$) [23]. The ENODes presented here can operate in the high accuracy range, albeit at a relatively high voltage. More concretely, for an ENODe cycled between ±0.3 V, the minimum V_{pulse} to achieve high accuracy in an array is 3 V with $E_{1/2\ cycle} = 7.5$ pJ · μm^{-2}. It would be desirable to further reduce both the applied voltage and the energy consumption.

One strategy to reduce the applied voltage and therefore energy cost is to reduce the voltage range accessed during programming, as indicated in figures 2(c) and (d). This reduces V_{pulse} and $E_{1/2\ cycle}$ to ca. 2.4 V and 2.5 pJ · μm^{-2}, respectively. However, this comes at the cost of the dynamic range; when using the full programming range (ca. ±0.3 V), ENODes have an G_{max}/G_{min} of ca. 4.5, whereas when the operating conductance range is reduced to ±0.1 V, the G_{max}/G_{min} ratio is only 1.7. Therefore, although the ENODes presented here meet the stringent linearity criteria using ~2.4 V write pulses, this leads to a relatively low G_{max}/G_{min} ratio, setting a low noise tolerance for an integrated array. Thus, there is a trade-off between high noise tolerance (full range) and low power (reduced range).

Reducing limit resistance for high speed and low power

In order to retain the charge state across the ENODe, and therefore memory state, we insert an R_{limit} to impede discharge of the device through the programming circuit. However, a high R_{limit} leads to inefficient writing by both increasing t_{switch} and E_{switch}, resulting in increased v (figure 3(a)) and increased $E_{1/2\ cycle}$ (figure 3(b), orange trace). Therefore, R_{limit} values should be increased to minimize self-discharge only by as much as necessary for the desired application. In contrast, low R_{limit} values have several benefits, as outlined below.

It is evident from the simulation that lower R_{limit} reduces the optimal V_{pulse} to achieve the desired linearity (dashed horizontal lines in figure 3(a)). To explain this behavior, first we consider how the fractional charging current, ($I_{pulse} \cdot f$), depends on R_{limit}:

$$I_{leak} = \frac{V_{ENODe}}{R_{ct}} \quad \text{and} \quad I_{pulse} = \frac{V_{pulse}}{R_{limit}} \quad (6) \text{ and } (7)$$

$$f = \frac{I_{pulse} - I_{leak}}{I_{pulse}} = 1 - \frac{V_{ENODe} * R_{limit}}{V_{pulse} * R_{ct}}. \quad (8)$$

As R_{limit} is decreased, f increases, resulting in increased linearity in the ENODe response to square voltage pulse inputs. Additionally, the increase in f also leads to decreased energy costs for programming due to decreased total current, given by equations (4) and (5). Lowering R_{limit} also increases the switching speed of the ENODe. When $I_{leak} \ll I_{pulse}$ ($f = \sim 1$), the equivalent switching time can be estimated as a charging RC circuit as follows:

$$t_{switch} = \frac{1}{n} * C_{ENODe} \frac{(V_{max} - V_{min})}{I_{pulse}} = \frac{1}{n} * R_{limit} * C_{ENODe} \frac{(V_{max} - V_{min})}{V_{pulse}} \quad (9)$$

where V_{max} and V_{min} correspond to the maximum and minimum programmed voltage across C_{ENODe}, respectively.

Although decreasing R_{limit} decreases t_{switch}, v, V_{pulse}, and E_{switch} and thus improves device performance considerably, decreased R_{limit} also results in rapid decay of ENODe memory, eliminating the non-volatile aspect of the device (figure 3(b), blue trace). The characteristic discharge time, $\tau_{discharge}$, is given by the following equation:

$$\tau_{discharge} = R_{limit} * C_{ENODe}. \quad (10)$$

For the case when the discharge current ($I_{discharge}$) through the external circuit dominates. For the resistances used here, $\tau_{dischrage}$ ranges from ca. 6 s (for $R_{limit} = 10$ kΩ) to ca. 6000 s ($R_{limit} = 10$ MΩ). This is a crucial drawback, as the ENODe state must be maintained in order to do useful computations after training. In order to be limited by materials performance rather than the programming circuit, the discharge time $\tau_{discharge}$ should be greater than the discharge time due to parasitic reactions such as oxidation. In the next section,

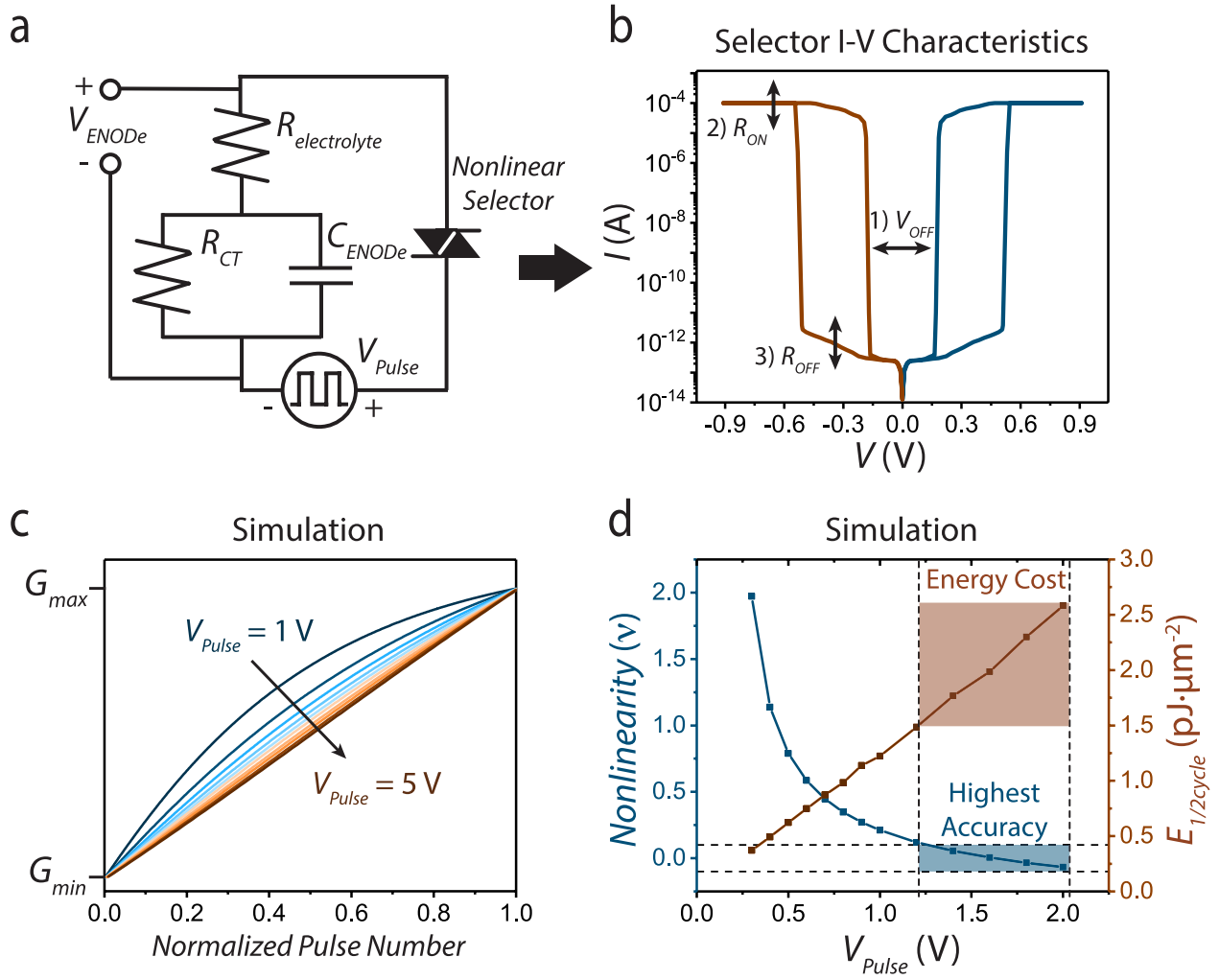

Figure 4. Device simulation with a nonlinear selector: (a) circuit diagram of a nonlinear selector device integrated with an ENODe, (b) IV characteristics of a high performance nonlinear selector from [25] showing (1) turn-off voltage V_{OFF}, (2) ON resistance R_{ON}, and (3) OFF resistance R_{OFF}, (c) conductance G_{ENODe} versus normalized pulse number for ENODes programmed through a selector device with a reduced voltage range (±0.15 V), (d) nonlinearity and energy cost of an ENODe programmed through a nonlinear selector with 10^8 ON/OFF ratio. The non-linear selector enables linearity at lower write pulse amplitudes.

we discuss how volatility can be minimized by integrating a nonlinear selector with the ENODe gate.

Nonlinear selector improves linearity and reduces switching energy

In order to minimize the effect of ENODe discharge between pulses, a nonlinear selector device can be inserted between the ENODe source and gate (figures 4(a) and (b)). The nonlinear selector acts as an electronic switch which uses voltage threshold filament formation between two metal electrodes to switch between an OFF state (no filaments) and ON state (filament forming a conductive bridge between electrodes) [25]. There are three important characteristics that determine the performance of a nonlinear selector coupled to an ENODe (figure 4(b)): (1) the turn-off voltage (V_{OFF}), (2) the ON resistance (R_{ON}), and (3) the OFF resistance R_{OFF}. V_{OFF} determines the programming voltage range, and therefore G_{min}/G_{max} that can be used; if the ENODe charges beyond V_{ON}, it will discharge through the selector until it reaches the V_{OFF} and the selector resistance increases. R_{ON} determines the write V_{pulse} and E_{switch} required to achieve linear G_{ENODe} versus pulse number as illustrated in the previous section. R_{OFF} determines the ENODe discharge rate by inserting it in place of R_{limit} in equation (10). Here, we insert the characteristics from [25] (OFF resistance of 10^{13} Ω and an ON/OFF ratio of 10^8, slope of <1 mV·dec^{-1}, and turn ON/OFF time of 75/250 ns) into our simulation to demonstrate the effectiveness of the nonlinear selector when coupled with an ENODe (figures 4(c) and (d)).

In the simulation (figures 4(c) and (d)), V_{ENODe} is limited to ±0.15 V to match the approximate V_{OFF} of the selector [25]. The required V_{pulse} to achieve sufficient v is reduced to 1.25 V (versus 3 V) primarily because of the reduced R_{ON} of the selector (~10^5 Ω) compared to R_{limit} (10^6 Ω) used in the previous sections. The limited voltage range of ±0.15 V also contributes to the reduced V_{pulse} requirement. Because the total charge (and therefore integrated current) required

to change the ENODe state is determined by C_{ENODe}, E_{switch} will decrease even after inserting the selector device due to the lowered V_{pulse}. Additionally, the selector device does not have the drawback of rapid discharge, or loss of state, associated with low R_{limit} values due to the high R_{OFF} (10^{13} Ω). The simulation shows $E_{1/2\ cycle}$ as low as 17 pJ · μm^{-2} can be achieved with desired linearity $\nu < 0.1$, which corresponds to $E_{switch} = 170$ fJ · μm^{-2} for an ENODe with 100 conductance states.

Inserting a selector in place of R_{limit} eliminates the tradeoff between switching energy and retention time that is problematic for some memristor devices. The nonlinear selector minimizes the effect of circuit discharge between programming pulses, which would be detrimental during both training and operation of the crossbar array. This allows the state-retention of the ENODe to be materials-limited rather than circuit-limited. In addition, the selector provides a low load during programming, allowing the ENODe to maintain previously reported low energy consumption [19]. Furthermore, because of the ENODe's three terminal architecture, the selector is decoupled from the channel (only couples the source-gate circuit) and thus does not distort the read signal, as is the case for two terminal memristors [14]. Thus, the selector is an ideal alternative to R_{limit}; the resistance is maximized to retain the programmed state but minimized during write to avoid high V_{pulse} and E_{switch}, enabling low-power operation.

Conclusion

In this work, we present a general model to describe the linearity of ENODe response to square programming pulses with arbitrary amplitude V_{pulse} to determine optimal write schemes to utilize parallel read-write operations. In our analysis, we find a tradeoff between the maximum/mininmum conductance ratio G_{max}/G_{min} and energy consumption due to the linearity requirement. Additionally, we demonstrate the need for a nonlinear selector device, which minimizes resistance during programming to reduce switching time t_{pulse}, voltage V_{pulse}, and energy E_{switch}, and maximizes resistance during read to minimize leakage of the ENODe charge. Finally, we project linear scaling of E_{switch} and t_{switch} by decreasing the ENODe volume, and therefore device capacitance C_{ENODe}. Using PEDOT/PEI:PSS as a model channel material with a nonlinear selector device, we project $E_{switch} = 170$ fJ and $t_{switch} = 500$ ns using $V_{pulse} = 1.3$ V for a 1 μm × 1 μm × 200 nm (length × width × thickness) channel with 100 conductance states. The predicted t_{switch} is estimated based on the switching speed of the selector and the drift velocity of protons in PEDOT:PSS rather than the RC charging time of the circuit, which would give a t_{switch} <1 ns (see supplementary text 1). We chose to project to a feature size of 1 μm because it is the resolution limit for our current photolithographic process [26]. Our future works aim to investigate the switching speed limitations for further scaled devices.

We also use the insights of the model to identify the critical materials properties for ENODe channels. We find that the write speed is improved by reducing C_{ENODe}. This can be achieved by scaling down the channel dimensions, e.g. by standard lithography, and by selecting low capacitance organic channels. To increase state retention, parasitic reactions leading to loss of state must be minimized. State retention may be improved by eliminating electron transfer pathways between the electrolyte and the channel, such as by encapsulating in an inert environment to avoid oxidation. Finally, we find that the critical parameter when selecting channel materials is the G_{Ch} versus V_g response. An ideal material will have a broad linear region with a steep slope in order to maximize the G_{max}/G_{min} ratio within a minimal V window. Our future work aims to expand the scope of the model to include solid-state electrolytes and to identify and leverage the structure-property relationships of organic semiconductors to design next generation ENODe materials.

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