A 160 GHz Frequency Quadrupler based on Heterogeneous Integration of GaAs Schottky Diodes onto Silicon using SU-8 for Epitaxy Transfer

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***Abstract*—An integrated frequency quadrupler operating at 160 GHz, producing 100 mW of output power, and achieving peak efficiency of 25.5% is described. The quadrupler design is based on prior art and consists of GaAs Schottky diodes with epitaxy transferred to a micromachined silicon carrier forming a heterogeneously-integrated chip. A newly-developed fabrication process that eliminates high temperature annealing and utilizes SU-8 for adhesive bonding was employed to realize the circuit. The new process improves device yield and reliability compared to previous implementations.**

***Index Terms*—Schottky diode, frequency multiplier, heterogeneous integration, submillimeter-wave.**

I. Introduction

Sources operating at submillimeter wavelengths are commonly implemented using a chain of frequency multipliers that are based on GaAs Schottky diodes [1], [2]. Although cascading multipliers is a practical solution to generating submillimeter-wave power, a number of issues are associated with this technique; the input stages of a multiplier chain must typically accommodate significant drive power, as the overall efficiency of large chains is often no more than a few percent. Moreover, mismatch between adjacent multipliers can readily perturb earlier stages in a cascade by pulling them from their optimum operating point through loading effects, thus reducing efficiency and output power. Consequently, intermediate matching or isolation networks are frequently inserted between adjacent stages, contributing to loss and system complexity.

A balanced circuit architecture for realizing a "unilateral" multiplier that mitigates the loading effects presented to prior multiplier stages and that addresses a number of the issues outlined above was described in [3]. In 2014, that design concept was extended to develop a monolithic balanced quadrupler operating at 160 GHz and producing 70 mW output power with 29% peak efficiency [4]. In this paper, a new epitaxy transfer and heterogeneous integration process that utilizes adhesive bonding with SU-8 is described and applied, for the first time, to implement a quadrupler based on the concept first reported in [4]. The new fabrication process addresses a number of issues that limited the device yield in previous monolithic frequency multiplier designs and has resulted in an integrated quadrupler with peak efficiency of 25.5% and maximum output power of 100 mW at 160 GHz.

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II. Circuit Architecture and Design

The circuit architecture for the balanced quadrupler is depicted in fig. 1(a). The input feeds a quadrature hybrid coupler that, in turn, drives two balanced frequency doublers. The outputs of these doubler stages are of equal amplitude and out-of-phase. Consequently, they can directly drive an output balanced doubler stage, thus producing a frequency quadrupler. Provided the input stages of the multiplier are identical, no power is reflected at the input port. Mismatches associated with the input doublers result in power scattered to the isolation port of the hybrid, which acts as a power dump. The input of the quadrupler, as a result, is matched over the operating bandwidth of the hybrid coupler, resulting in a unilateral multiplier.

Varactor diodes used for the quadrupler design consisted of n-type GaAs epitaxy with modulation layer 280 nm thick and

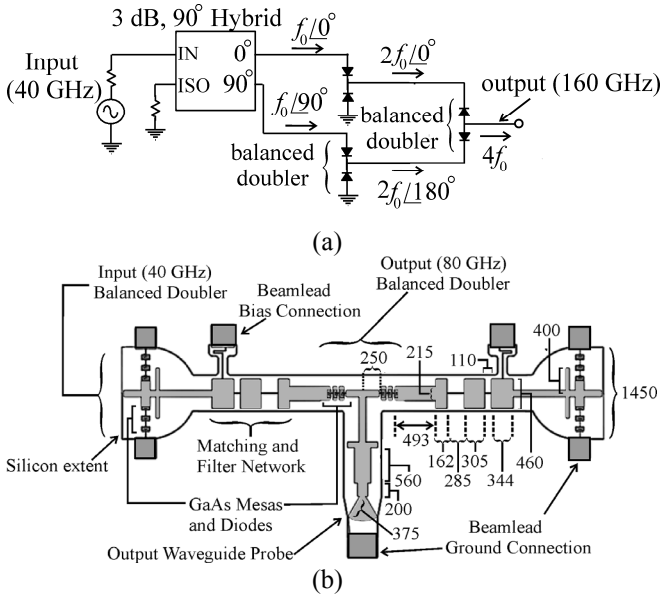

Fig. 1. (a) Quadrupler circuit architecture and (b) layout of the integrated quadrupler chip. The quadrature hybrid is implemented off-chip (in waveguide) and all dimensions noted are in μm.

doping concentration of 2×10^{17} cm^{-3} and buffer layer 1 µm thick with doping concentration of 5×10^{18} cm^{-3}. Harmonic balance analysis performed on 9.6 µm and 8 µm diameter varactors fabricated from this epitaxy, determined the optimum impedances to be $10 + j70\ \Omega$ for the input at 40 GHz and $10 + j50\ \Omega$ for the second stage input at 80 GHz. Final design of the quadrupler was accomplished by partitioning the circuit geometry into its three primary sections — an input doubler stage, an output doubler stage, and the intermediate matching network— and simulating each using *HFSS*. Scattering parameters obtained were imported into Keysight's *ADS* to perform harmonic balance analysis on the full quadrupler and to verify its operation.

A layout of the complete integrated quadrupler chip is shown in fig. 1(b). The circuit incorporates three sets of balanced doublers comprising a total of 18 varactor diodes, and includes intermediate matching and filter networks, an output waveguide probe, and integrated beamleads for biasing. The chip is 7.5 mm from end-to-end and made of 15 µm thick, high-resistivity (ρ > 10 kΩ-cm) silicon onto which the GaAs varactors have been integrated.

III. Fabrication Process

The integrated quadrupler shown in figure 1(b) was fabricated using a new epitaxy transfer process by which the GaAs needed to form Schottky diodes is bonded to a silicon-on-insulator (SOI) substrate. The process utilizes epitaxy consisting of a semi-insulating 650 µm GaAs handle with 1 µm AlGaAs etch stop layer, n-GaAs and n+-GaAs device layers (as described previously), and a 90 nm highly-doped (>10^{19} cm^{-3}) graded $In_xGa_{1-x}As$ cap layer (x: 0→0.6) to allow the formation of low resistance ohmic contacts using a Ti/Pd/Au/Ti metal stack-up that does not require thermal annealing.

Initially, an ohmic metal stack-up, Ti/Pd/Au/Ti (20/40/400/20 nm) is evaporated over the entire highly-doped $In_xGa_{1-x}As$ cap layer. The ohmic metal surface is subsequently bonded to the SOI wafer using SU-8 as an adhesive layer. The relatively low curing temperature of SU-8 (100−140ºC) coupled with its relatively low percent volume shrinkage after crosslinking [5], [6] results in a robust epitaxy transfer that is not prone to wafer fracture or delamination arising from swelling of the adhesive layer or mismatches in thermal expansion coefficients.

After the bonding step, the thick GaAs handle is thinned in a nitric acid solution and removed in a citric acid etch. The exposed AlGaAs etch stop layer is removed with hydrofluoric acid, revealing the GaAs device layer field. Fig. 2(a) shows a scanning electron micrograph (SEM) of the cross-section of the epitaxy after this step and illustrates the quality of the bond. The SU-8 layer between the ohmic metal and high-resistivity silicon layer is uniform (~250 nm thick) with no observable voids.

After removal of the handle GaAs and etch-stop layer, diode mesa areas are defined photolithographically and formed by a combination of wet etches, sputter etches, and reactive-ion etches that stop on the silicon surface [6]. Subsequently, device mesas are lithographically patterned and formed using a H_2SO_4: H_2O_2: DI wet etch, resulting in GaAs mesas sitting atop ohmic metal pedestals, shown in fig. 2(b). The remaining diode processing steps utilize standard lithographic patterning to form the anode, airbridge finger contact, ohmic contact overlay metallization, and

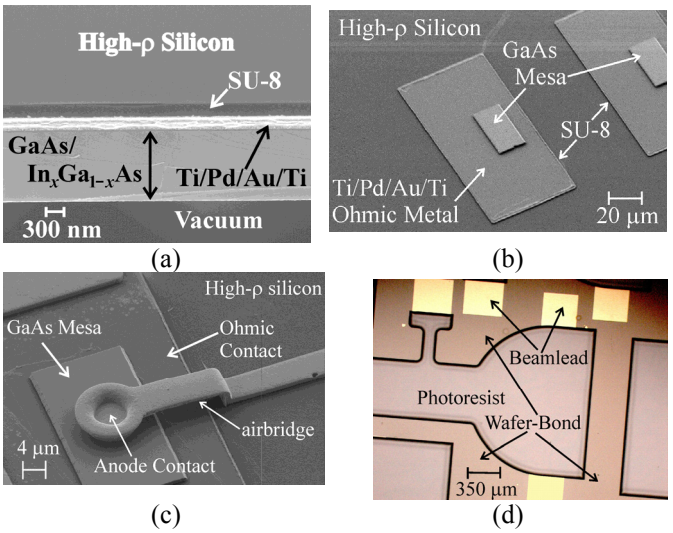

Fig. 2. Images illustrating steps of the fabrication process. (a) SEM image of the bonded epitaxy. (b) Formation of the GaAs mesas and ohmic metal pedestals. (c) Anode and airbridge structures. (d) Backside lithography used to define the chip geometry.

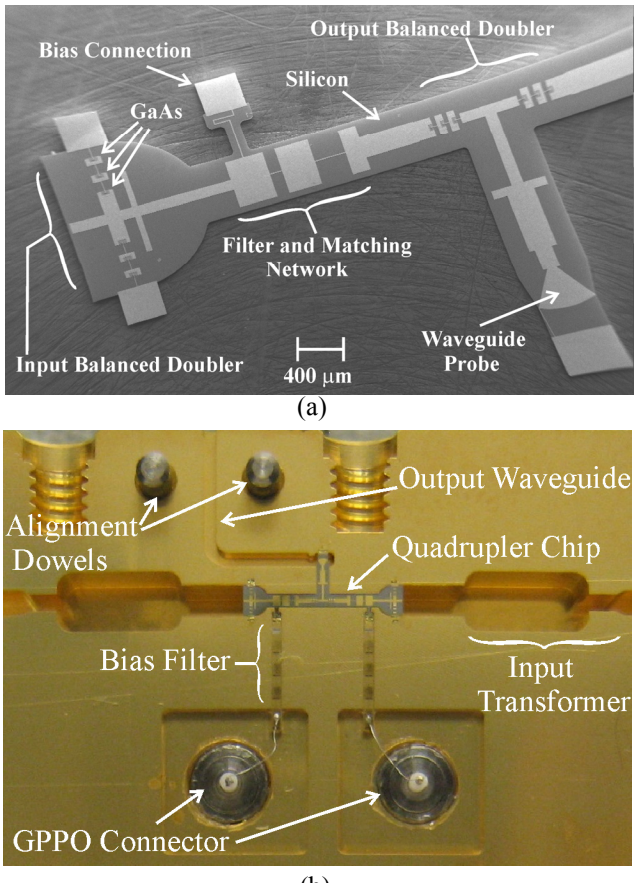

Fig. 3. (a) SEM image of the completed quadrupler chip. (b) The quadrupler chip mounted to its waveguide housing. The quadrature hybrid is not shown.

other circuit features on the high-resistivity silicon surface. Fig. 2(c) shows an SEM image of the final diode device structure. For the quadrupler implemented in this work, the diameters of the diodes are nominally 9.6 μm for the input stage doublers and 8 μm for the output stage doubler.

Once fabrication of the diodes is completed, the silicon carrier to which they are bonded is micromachined to form an integrated chip with geometry tailored to fit the waveguide housing to which it will be affixed. Initially, the surface of the wafer with diode circuitry is attached to a sacrificial carrier using wafer-bond adhesive. Following this, the thick "handle" silicon layer of the SOI is removed through a combination of lapping and plasma etching. The buried oxide is then removed with a buffered oxide etch. In the final step, backside lithography defines the chip geometry, including integrated beamleads, and a silicon etch forms the final 15 μm thick chips. Individual chips are then released by removing the sacrificial carrier. Fig. 2(d) shows an image of the backside lithography prior to release from the sacrificial carrier wafer. An SEM image of the completed quadrupler chips is shown in fig. 3(a). Fig. 3(b) shows a photograph of the chip mounted to its housing. Note that the 40 GHz input quadrature hybrid is implemented in waveguide, but is not shown in fig. 3(b) due to its relatively large size.

IV. Measurements

Characterization of the quadrupler is done using an Agilent E8257D frequency synthesizer followed by a Spacek Labs SP408-35-26 amplifier with 35 dB gain and 36 to 43 GHz bandwidth. An Erickson PM5 power meter is used to measure the multiplier output power in the WR-5.1 band.

Fig. 4 shows the input-output power relation for an input frequency of 40 GHz and diode (reverse) bias of 12 V. Peak efficiency of 25.5% occurs for an input of 280 mW. Beyond 280 mW, the multiplier begins saturating and the efficiency drops. The output power over the full 36—43 GHz operating bandwidth of the Spacek power amplifier is shown in fig. 5, for an input power level of 285 mW and bias of 12 V. The power measured at the isolation port of the hybrid coupler, normalized to the available power from the input power amplifier, is also shown and provides a measure of the quality of the input match to the quadrupler. The peak power under these operating condition is 72 mW and the output power is greater than 20 mW over an output bandwidth of 146—176 GHz (18.5% fractional bandwidth).

Output power of the quadrupler as a function of input power near the design frequency (160 GHz) is shown in fig. 6. The saturation characteristic of the multiplier is evident and a maximum output power of 100 mW (20 dBm) was measured at 159 GHz. This output power corresponds to an input power of 650 mW and overall quadrupler efficiency of 15%.

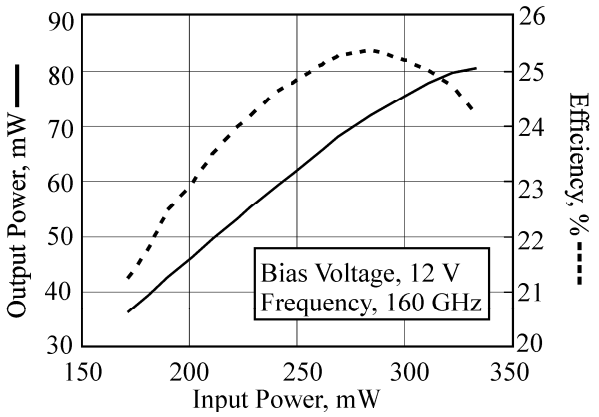

Fig. 4. Quadrupler output power and efficiency vs. input power.

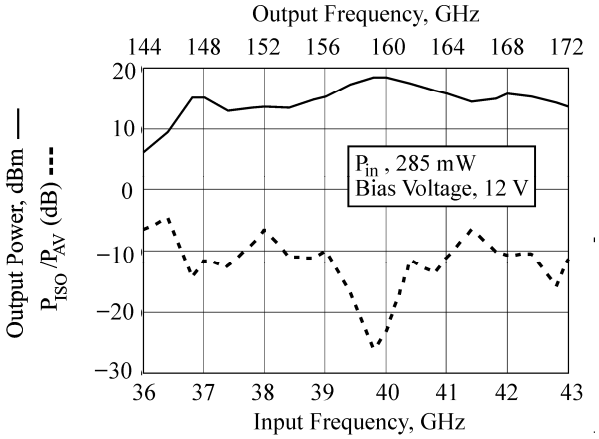

Fig. 5. Output power and power measured at the isolation port, normalized to available power. vs. frequency

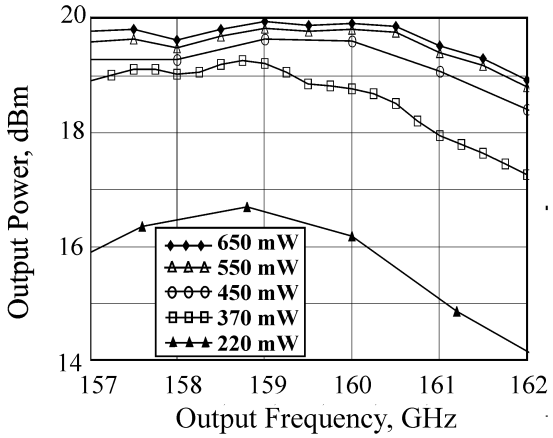

Fig. 6. Power output vs frequency for different input power levels.

V. Summary

This work has presented a new implementation of an integrated frequency quadrupler, based on prior art [4]. A modified fabrication process that eliminates high-temperature thermal processes and utilizes SU-8 as an adhesive for epitaxy transfer and heterogeneous integration was adopted to realize the circuit. This approach has resulted in a more robust and reliable process for developing III-V based submillimeter-wave circuits integrated on silicon membrane carriers. A quadrupler fabricated with the new process has produced an output power of 100 mW at 160 GHz and peak efficiency of 25.5%.

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