Investigation of Phonon-Carrier Interactions in Silicon-Based MEMS Resonators

Hakhamanesh Mansoorzare and Reza Abdolvand
Department of Electrical and Computer Engineering
University of Central Florida
Orlando, Florida, USA
hakha@knights.ucf.edu

Hedy Fatemi
Qorvo Inc.
Apopka, Florida, USA

***Abstract*—In this work, a technique is introduced for isolating the energy loss associated with the interaction of charge carriers with acoustic phonons in thin film piezoelectric-on-silicon (TPoS) MEMS resonators. This method facilitates the investigation of acoustoelectric loss mechanism. The variation in quality factor (Q) and insertion loss of high frequency TPoS resonators is reported while the surface carrier concentration of the silicon layer is varied through application of a voltage to the metal-dielectric-silicon capacitor that is intrinsically formed during the conventional fabrication of TPoS resonators. A maximum of 3% improvement in the insertion loss (IL~9 dB) of a ~926 MHz resonance mode is recorded when a 4 V bias is applied to the said capacitance which is believed to stem from a reduction in interaction of acoustic phonons with carriers.**

Keywords—acoustoelectric; loss; phonon-carrier; piezoelectric resonator; RF MEMS

I. Introduction

In micromechanical resonators made of semiconducting substrates (e.g. silicon), several energy loss mechanisms have been investigated and found to contribute in limiting the quality factor (Q) at high frequencies (~1GHz). These can be categorized into intrinsic losses (due to phonon-phonon and phonon-carrier interactions or the dielectric material) that are material/operation dependent or extrinsic losses (due to transfer of energy to the surrounding, surface effects, and resistivity of electrodes) that are a function of the resonator design [1]. Most of these dissipative processes have been extensively studied, however, until now, there has been very little focus on the loss associated with the interactions of acoustic phonons and charge carriers (phonon-carrier or acoustoelectric loss). Research on the interaction of elastic waves and charge carriers dates back to 1941 and the work by Shaposhnikov in which he suggested that elastic waves interacting with an electron plasma undergo attenuation [2]. Later, detection of a DC current in parallel with the propagation of acoustic waves [3] inspired the idea of acoustoelectric (AE) amplification [4] whereby, transfer of momentum from supersonic electrons to acoustic phonons in a piezoelectric semiconductor medium (CdS) results in amplification of acoustic wave. Relative velocity of phonons and electrons determines whether attenuation or amplification takes place and the latter requires a higher electron velocity. Nevertheless, low electron mobility in such materials mandated application of very high voltages in order for supersonic drifts to appear. Consequently, using separate piezoelectric and semiconductor media – a piezoelectric-semiconductor heterostructure – was proposed as the solution [5].

A stress wave propagating in a piezoelectric-semiconductor heterostructure interacts with charge carriers of the semiconductor through two distinct mechanisms. First, the deformation potential, in which the mechanical oscillation of a resonant body distorts fermi levels and the process of relaxation of electrons back to a new equilibrium results in loss. Second, the piezoelectrically-induced electric fields associated with the elastic waves, having both longitudinal and transverse components, extend into the adjacent semiconductor layer, excite currents, and cause charge bunching [6]. Both of these mechanisms result in transfer of momentum from the elastic waves to charge carriers and a loss mechanism known as the AE loss [7]. In this work we investigate the impact of AE loss on the overall Q and insertion loss of AlN-on-silicon resonators and conclude that this source of loss is not negligible.

II. Silicon Resonator with Variable Charge Density

Thin film piezoelectric-on-silicon (TPoS) [8] resonators are fabricated by depositing a stack of AlN/Mo/AlN/Mo on a silicon-on-insulator (SOI) substrate (Fig. 1).

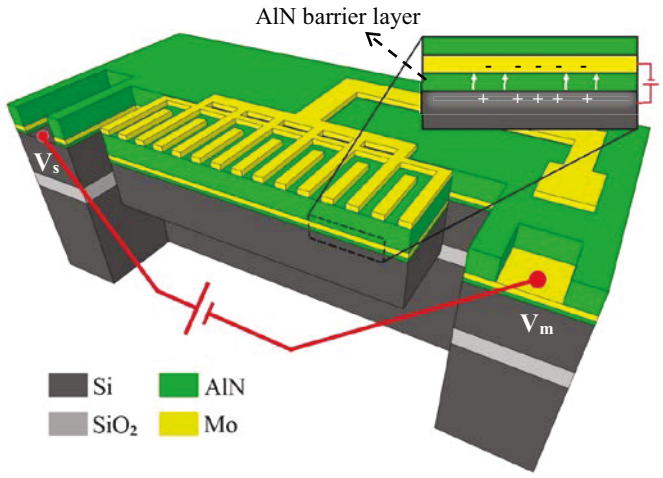

Fig. 1. Schematic of a cross section of the resonators studied herein, showing the integrated MIS capacitor and points of contact for applying voltages V_m respective to V_s. White arrows represent electric field within the capacitor.

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The first AlN layer (typically 20-50 nm thick) is the barrier layer for the next Molybdenum film which is shown to improve the C-plane growth of the subsequent AlN film. In this work, the metal-insulator-semiconductor (MIS) capacitor that results from the barrier layer sandwiched between the first metal and the silicon (Fig. 1) is utilized to modify the surface carrier concentration in the silicon, similar to the operation of field effect transistors. In order to modify the surface carrier concentration, a DC voltage supply will be connected between the silicon and the bottom Mo layer (Fig. 1). The behavior of AlN MIS capacitors should be understood before any conclusion could be drawn from our studies. Fortunately, this behavior has been previously studied and characterized [9].

In this work, high-order extensional mode TPoS resonators fabricated on a 3 µm lightly boron-doped (doping concentration in the order of 10^{13} cm^{-3}) Si are utilized. The fabrication process flow (Fig. 2) starts with sputter depositing the first AlN/Mo stack and patterning the Mo layer using SF_6/O_2 dry etching in order to define points of contact to the device Si layer in forthcoming steps. Next, the second AlN/Mo stack is sputtered and the top Mo layer is patterned (same recipe) so that the top electrodes are formed (Fig. 2 (a)). Then, the AlN is wet etched in a heated TMAH solution to create access to the bottom electrode and Si layer (Fig. 2 (b)). The resonator body is then formed by plasma etching the full stack of material down to the SOI buried oxide (BOX) layer (Fig. 2 (c)). Handle layer silicon is then etched from the backside in a deep-reactive-ion-etching chamber using Bosch process and the resonator is finally released by wet etching the BOX layer in a buffered oxide etchant (Fig. 2 (d)).

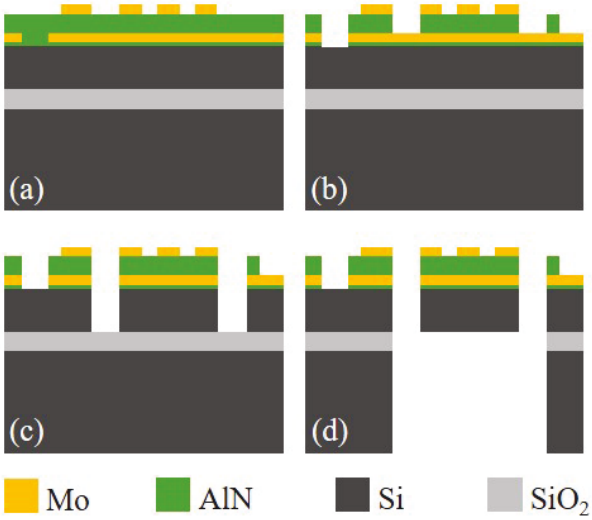

Fig. 2. Simplified fabrication process flow of the devices studied herein.

III. Acoustoelectric Loss In Silicon

The component of loss that arises from the deformation potential is directly proportional to the total doping concentration of the semiconductor layer and is considered a less significant dissipative process [10]. On the other hand, the depth of penetration of the electric field associated with the stress in AlN layer into the Si is limited by its Debye length which is inversely proportional to the doping concentration:

$$L_D = \sqrt{\frac{\varepsilon_{Si} k_B T}{q^2 N_d}} \tag{1}$$

Where ε_{Si} is the permittivity of Si, k_B is the Boltzmann's constant, T is the temperature, q is the elementary charge, and N_d is the doping concentration. Equating the set of equations for the electric field in Si with that of the piezoelectric coupling for AlN at their boundary results in a dispersion equation [11], the solution of which yields the AE attenuation coefficient:

$$\alpha = \frac{q^2 \sigma}{2 v_a \varepsilon_{AlN} \varepsilon_{Si}} \left(1 + \frac{\sigma}{\varepsilon_{AlN} \varepsilon_{Si} \omega^2} \left(1 + \frac{L_D{}^2 \omega^2}{v_a{}^2} \right)^2 \right)^{-1} \tag{2}$$

In which v_a is the acoustic velocity, σ (equals to $q\mu N_d$, where μ is the carrier mobility) is the electrical conductivity, ω is the angular frequency, and ε_{AlN} is the permittivity of AlN respectively. This model predicts that a proportionality exists between AE loss and carrier concentrations at small values of carrier concentration and an inverse proportionality at the higher end of the spectrum [5]. The normalized AE loss predicted from eqn. 2 as a function of the carrier density in the Si layer and the frequency of operation is plotted in Fig. 3.

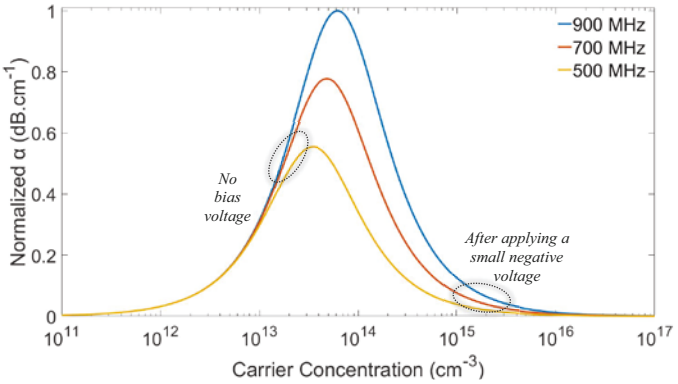

Fig. 3. Normalized AE loss as a function of the concentration of acceptor holes and frequency; the ovals indicate the carrier density at zero and a small negative bias.

IV. Measurements and Verification

To measure the effect of carrier density on loss, the voltage applied to the embedded MIS capacitor in a targeted TPoS resonator is varied while the frequency response (i.e. S_{21}) is measured using a Rohde & Schwarz ZNB 8 network analyzer and a pair of Cascade Microtech GSG probes at room temperature in atmospheric pressure. The biasing DC voltage is applied through wire-bonds in between a bottom electrode contact pad and an exposed silicon contact pad and is varied at 1 V steps. The measurement is repeated several times for the same resonance mode and also carried out for three different resonance modes.

The observed trend of variations in Q as a function of the applied voltage for a resonator operating at 802 MHz is plotted in Fig. 4, demonstrating a 3.2% improvement in accumulation regime, while reversing polarity of the applied voltage exhibited negligible variations.

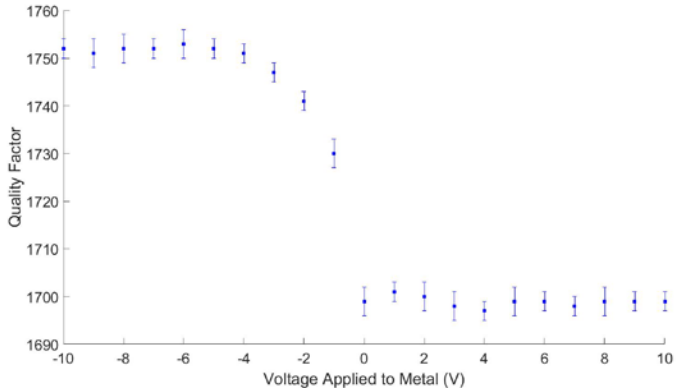

Fig. 4. Average quality factor of the resonator with highest variation in Q as a function of the voltage applied to metal plate.

The measured S_{21} of the resonator at 927 MHz is displayed in Fig. 5 for 3 values of applied voltage. As seen, an improvement in loss is measured upon application of a negative voltage to the metal plate (V_m) with respect to the Si layer (V_s), but the improvement appears to reach a saturation at voltages above 4 V. Conversely, minor changes are measured once the polarity of the voltage is reversed.

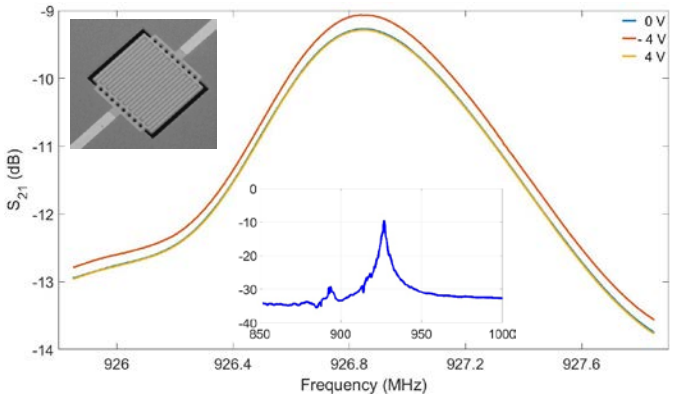

Fig. 5. Measured S_{21} at different voltages applied to metal plate showing a considerable improvement at accumulation regime while negligible change is measured due to inability to form an inversion layer (curves are over each other).

The measurement results are believed to be consistent with the prediction from eqn. 2 (and plotted in Fig. 3) considering that a sharp rise in carrier (hole) concentration after application of a small negative voltage is expected at the silicon surface while the concentration is almost unchanged for positive voltages [9]. The accumulation density is estimated to be pushed beyond 10^{15} cm^{-3} by applying a -1 V or higher which corresponds to a shrinkage in the Debye length from around 1.2 µm to fewer than 100 nm. It is evident from Fig. 3 that such a carrier density corresponds to a decrease in AE attenuation compared to the original concentration. The insensitivity of carrier concentration to positive voltages is associated with the absorption of minority carriers at the interface of AlN with silicon [9]. The results are summarized in the table below.

TABLE I. MEASUREMENT RESULTS

Applied Voltage (V_m - V_s)	**Average Loss of Resonators Operating at:**		
	485 MHz	***754 MHz***	***927 MHz***
0 V	13.83	15.38	9.31
- 4 V	13.59	15.07	9.07
% improvement	1.73	2.01	2.57

It is worth mentioning that in order to ensure that the results do not stem from the direct application of a voltage to the network analyzer, probably due to an unwanted short circuit on the path, both coaxial DC block for suppressing and bias tee for direct application of the DC voltage were attached to the network analyzer and tested.

V. CONCLUSION

The inherent MIS capacitor of the TPoS resonators – formed as a result of the barrier AlN layer – was utilized to modify the doping concentration at the surface of the Si, adjacent to the AlN barrier layer through applying a DC voltage. By so doing, the intrinsic loss component due to the interaction of phonons and charge carriers was isolated. Such interactions can be results of penetration of piezoelectrically coupled electric fields in the Si layer or the deformation potential and are influenced by the doping concentration of Si. Upon increasing the doping concentration at the AlN-Si boundary, improvements, up to 3.2%, in Q of the resonators were recorded, the higher the frequency the more the improvement. Such observations are believed to be caused by the decrease in the Debye length of the device Si layer, showing that this source of loss is not negligible and needs to be further studied and characterized.

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