A Soft-Matter Biomolecular Memristor Synapse for Neuromorphic Systems

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Abstract—The goal of neuromorphic computing is to recreate the computational power and efficiency of the human brain with circuitry. The ability of the brain to solve complex real time tasks, while consuming 20 W of power on average, is made possible through its connection density, adaptability, and parallel processing. Recreating these features using traditional electronics circuit elements is incredibly difficult, and therefore, soft-matter memristors made of biomolecules similar to those found in biological synapses and capable of emulating various synaptic features can be used as neuromorphic hardware. In this work, we introduce and experimentally demonstrate an electronic neuron circuit capable of interacting with ionic, soft-matter memristors. These memristors are proven to exhibit short-term plasticity, especially paired-pulse facilitation and depression found in presynaptic terminals — features that are not found in state-of-theart solid-state memristors. We make use of these features for applications in online learning by developing a synapse-neuron circuit which implements spike-rate-dependent plasticity (SRDP) as a learning function.

I. Introduction

Neuromorphic computing aims at emulating the processing power and efficiency of the brain. The co-location of memory and computation in the brain as well as its massively parallel structure create a powerful and highly efficient computational scheme that is not found in conventional computers [1] [2]. Moreover, the brain has the ability to adapt through synaptic plasticity, which allows online learning while processing. Generally, there are two forms of synaptic plasticity, long- and short-term. In this work, we will focus on short-term plasticity as it is an inherent property of the device discussed herein.

Short-term synaptic plasticity, especially paired-pulse facilitation (PPF) and paired-pulse depression (PPD), occurs when the time relationship between neuron spikes causes increases or decreases in the accumulation of spikes in the subsequent neuron [3]. The physiological causes of short-term plasticity, which is exclusively pre-synaptic, are directly related to the concentration of calcium ions in the pre-synaptic terminal leading to a greater release (PPF) or a reduced release (PPD) of synaptic vesicles [4]. This means that short-term plastic effects are dependent on only input spike fires, unlike STDP or long-term plasticity.

In this work, we closely examine a soft-matter memristor [5] which resembles biological synapses and exhibits short-term plasticity (PPF and PPD) similar to that found in pre-synaptic terminals. More interestingly, the processes responsible for such behavior also resemble the physiological phenomena that create short-term synaptic plasticity in vivo. Experimental results show the memristor connected to discrete neural network circuitry emulates short-term synaptic plasticity. These components can create larger networks with the intent to build neural network structures that use this phenomena to adaptively solve problems [6].

II. PROPERTIES OF THE BIOMOLECULAR MEMRISTOR

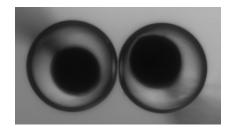


Fig. 1. A biomolecular memristor constructed from a peptide-doped lipid bilayer (5nm thick) formed at the interface for two lipid coated aqueous droplets (each c.a. 1mm in diameter) in oil.

A. The Soft Matter Synapse Device

The soft-matter memristive device used as a synapse is described in [5]. In brief, it is formed by assembling a lipid bilayer at the cojoining interface of two lipid-encased droplets of water in oil seen in Figure 1. Each droplet contains lipids, salt (sodium chloride, NaCl), and alamethicin peptides. The lipids form a monolayer around each droplet and when the droplets are brought together a lipid bilayer forms at the interface. The device uses voltage-activated alamethicin peptides to facilitate ionic current between the droplets across the highly insulating lipid membrane. Like sodium and calcium channels in axons, voltage-driven insertion of alamethicin creates ion channels that are voltage and time dependent. The

conductance of the device is dependent on applied voltage, time, and previous state. Upon reaching the channel insertion threshold, the device's conductance non-linearly increases over time due to the insertion of channels before reaching steady state. When voltage is removed, the inserted channels exit the membrane, which then restores its insulating state. The temporal component of channel inserting and exiting gives the device memristive properties, while the voltage threshold for channel insertion gives non-linear resistance. These features combine for a device that is suited to mimic biological synapses.

B. Device Characteristic

Unlike solid state electronics, the soft-matter memristor operates on a time-scale and voltage range similar to its biological counterpart [5]. Voltages above a two hundred millivolts will destroy the bilayer, requiring precise voltage control around the device. To efficiently utilize the memristive properties of the alamethicin channels, low voltages must be applied to switch resistance states. Furthermore, the necessary time required for the applied voltage to cause the memristor to switch to the low resistance state is approximately 100ms. Switching from the low resistance state back to the high resistance state takes about 10ms. Thus, the device operates at a similar time scale to the processing speed of biological synapses. The change in resistance due to the applied voltage mimics the change in synaptic efficiency based on the short-term synaptic plasticity effects of neural connections.

Moreover, the device displays properties different from transition metal memristors where the high resistance is $10G\Omega$ and the low resistance is $100k\Omega$, while parasitic capacitance is on the order of hundreds of picofarads. Both the resistance ratio and parasitic capacitance are directly related to the device characteristics, such as size, alamethicin concentration, etc. For use as a memristor, reducing the parasitic capacitance is important and will be further explained in Section III-B. Other important device characteristics to control are the insertion and exiting rates of the alamethicin. Quicker insertion and slower exiting produces a faster device that retains its memory longer. Having the ability to manipulate the device properties allows for improved synaptic features that closely resemble biology.

III. NEUROMORPHIC SHORT-TERM LEARNING CIRCUIT

A. Neuron Circuitry

The neuron circuit used follows the leaky integrate and fire model [7]. It is built with integrator and comparator opamps and uses a similar reset system to the axon hillock neuron circuit [8] [9]. The neuron takes input current from the biomolecular memristor and integrates it as a stored voltage. The stored voltage is then compared against the neuron's threshold voltage. Upon crossing the threshold, the neuron outputs a voltage spike and resets its accumulated voltage. While resetting, the neuron blocks all incoming spikes.

The input current is stored as a voltage by the capacitor C_{Mem} in the feedback loop of the first op-amp seen in Figure 2. The stored voltage V_{mem} is compared against the

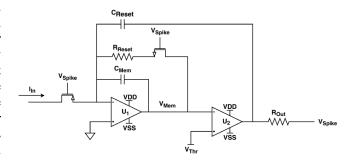


Fig. 2. Schematic of analog leaky integrate and fire neuron

threshold voltage V_{Thr} . When the stored voltage drops below the threshold voltage, the output of the second op-amp rises from the negative rail to the positive rail, creating the neuron's output voltage spike V_{Spike} . When the neuron fires, the ptype transistor at the input is switched off and blocks input current. The switching of the output voltage from low to high drives the accumulated voltage through the positive feedback capacitor C_{Reset} . V_{Mem} is driven to the negative rail at the start of the spike. V_{Spike} turns on the n-type transistor in the negative feedback loop of the first op-amp. V_{Mem} increases up to V_{Thr} due to leakage through the n-type transistor and its series resistor R_{Reset} . When V_{Mem} has increased back above the threshold, the output of the second op-amp drops from a high to low voltage. This switch ends the high voltage spike of the neuron and causes V_{Mem} to rise up to the reset voltage through the positive feedback capacitor C_{Reset} . The n-type transistor in the feedback loop of the first op-amp turns off, drastically reducing the leakage of the circuit. The p-type transistor at the input turns on and once again allows current to flow into the neuron.

The time that V_{Spike} is high defines the spike width of the system and is set by the n-type transistor. The refractory period is set by the p-type transistor at the input. These two neuron characteristics are almost equivalent because the V_{Spike} is used to control both of the transistors. Since the refractory period is not extended far beyond the spike width, spikes can be generated close to one another. Unlike transition metal oxide memristors, the soft-matter memristor decays quickly from its on resistance state to its off resistance state. To take advantage of the temporal component of the biomolecular memristor, the spikes must be generated in close succession. Therefore, voltage spikes across the device must be close to one another and long enough to cause switching in the device. The neuron is set to create voltage spikes with a defined width of 15ms. The spike width is set by choosing the values of C_{Reset} and R_{Reset} to drive the stored voltage and to increase the leakage resistance during the spike, respectively. Resistor and capacitor values used in the physical circuit are shown in Table I.

B. Synapse Circuitry

The synapse consists of the soft-matter memristor M_1 and solid-state electronics seen in Figure 3. It is imperative that the

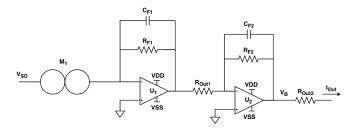


Fig. 3. Schematic synapse circuitry including biomolecular memristor

voltage drop across M_1 does not exceed 200mV, otherwise the device will break. Both terminals of the memristor are controlled by the surrounding circuitry in order to limit the voltage across the device. The output node is held at a virtual ground due to the negative feedback of the first operational amplifier. The input voltage V_{SD} at the memristor is either zero volts or the applied spike voltage, 150mV. Since the applied voltage is constant, the output current of the memristor is proportional to its resistance state. Thus, the resistance state of the memristor represents the synaptic weight. The parasitic capacitance is neglected.

he feedback loops of the amplifiers each consist of a resistor and capacitor. The resistors are used to amplify the output current M_1 . The capacitors are used to stabilize the op-amps. The memristor's characteristics, described in Section II-B, help to determine the appropriate values for these components. To maximize the output range of the synapse, the feedback resistor R_{F1} should be sized similarly to the lowest resistance state of the DIB. The capacitor C_{F1} should be sized such that there is stability without signal integration. The values of the components used in the circuit are shown in Table I. Since the capacitance of the DIB is approximately 100pF, the first stage uses a larger 1nF feedback capacitor to attenuate parasitic capacitive effects. The resistance of the DIB is generally much larger than the $500k\Omega$ resistor in the first feedback loop. This results in a gain that is less than one, attenuating the signal. The second stage amplifies the signal, since the resistance R_{Out1} between the stages is chosen to be smaller than the feedback resistance R_{F2} . No capacitance is needed between the two op-amps, and a smaller feedback capacitor C_{F2} is used.

IV. TESTS AND RESULTS

Two tests were run to determine the effects of short-term plasticity. The pulse pairing tests determine the relationship between two spikes for different spikes voltages and times applied to the memristor. The spike rate tests show the continued activation of the memristor and the proper operation of the neuron.

A. Spike Rate Dependent Plasticity

In the spike rate tests, the circuitry for the synapse and neuron is verified as seen in Figures 4 and 5. Here we see the input voltage across the memristor, V_{SD} , creates an output

TABLE I CIRCUIT COMPONENT VALUES

Circuit	Component	Value
Neuron	R_{Reset}	150kΩ
	R_{Out}	$6.8 \mathrm{k}\Omega$
	C_{Mem}	1μF
	C_{Reset}	500nF
Synapse	R_{F1}, R_{F2}	500kΩ
	R_{Out1}, R_{Out2}	100kΩ
	C_{F1}	1nF
	C_{F2}	27pF

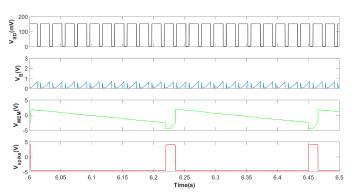


Fig. 4. Experimental node voltages from physical results for spike trains. 150mV input voltage spikes with 15ms on and 5 ms off time.

of the gain stage, V_B , that drives the accumulation, V_{Mem} in the neuron. The accumulated voltage eventually causes the neuron to cross the threshold and create and output voltage spike, V_{out} . Controlled parameters of the neuron include its leakage and threshold voltage, which was set to -2.5V.

The effect of two different input spike rates causing different output spike rates is shown in Figures 4 and 5. The spikes occur 5ms and 1ms apart, respectively. The time window shown for the voltages in the figures is after the memristor has reached a steady state response. The slower spike rate in Figure 4 takes more spikes than the faster spike rate in Figure 5 showing facilitation is increased with higher frequency of inputs. Both of theses spikes occur within the 10ms pore exit time of the memristor. Because of this, the overall spike strength is higher than if the spikes were farther apart in time.

B. Pulse Paired Facilitation

The short-term effects of pulse pairing, derived from the synaptic device, are characterized in Figures 6 and 7. The pulse pairing test looks at two isolated spikes and the difference between the output rms voltage V_B during each spike. For Figure 6, the tests consisted of two spikes of different voltages, 120 mV to 150 mV, applied to the synapse with different time between spikes. Each spike is 50 ms. For Figure 7, the length of a spike was varied, 20 ms to 50 ms, while the applied voltage was constant at 150 mV. Both tests used the same synapse

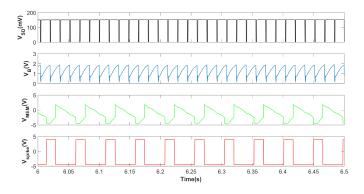


Fig. 5. Experimental node voltages from physical results for spike trains. 150mV input voltage spikes with 15ms on and 1 ms off time.

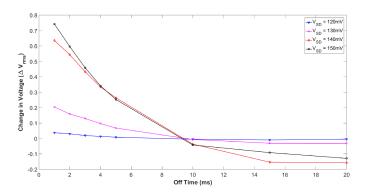


Fig. 6. Experimental change in synapse output voltage between two spikes vs. change in time between spikes for different spike voltages.

circuit. The synapse shows facilitation when the two spikes are within 10ms of each other. When the spikes are beyond 10ms the synapse shows depression. This is seen clearly in the highest voltage and longest tests, black in the figures, but the same curve shape is held between all tests. These figures show the nature of the short term memory of the device.

V. Conclusion

To achieve biologically realistic synaptic plasticity we use a soft matter memristor. This work shows how the integration of the memristor with electronics produces a viable circuit element for recreating short term synaptic plasticity. The memristor can be connected with a solid state neuron to produce output with unique accumulations in the neuron based on input spike patterns. The memristor shows both pulse paired facilitation and depression. With the data collected, larger spiking neural networks can be generated to solve tasks using this form of synaptic plasticity. Improvements can be made in the memristor in its characteristics and its reliability. Following the device changes, the circuit will need to be updated appropriately. Having control over the insertion and exiting rates of the channels in the biomolecular memristor will help create different synaptic responses. Reducing parasitic capacitance will allow for a lower capacitance system that relies entirely on the memristive switching in the device. This work will be

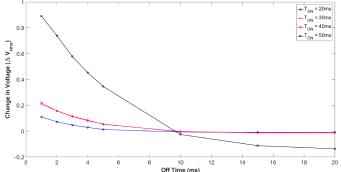


Fig. 7. Experimental change in synapse output voltage between two spikes vs. change in time between spikes for different spike widths.

used as a building block in a larger system for spiking neural network hardware.

ACKNOWLEDGMENT

The authors would like to thank Dr. Mark Dean, Nick Skuda, Sam Brown, Sam Zimmermann, Gangotree Chakma, Md. Musabbir Adnan, Sagarvarma Sayyaparaju, and Sherif Amer from the University of Tennessee, Knoxville for interesting and useful discussions on this topic.

This material is based in part upon research sponsored by the National Science Foundation under Grant No. NCS-FO-1631472. The U.S. Government is authorized to reproduce and distribute reprints for Governmental purposes notwithstanding any copyright notation thereon.

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