A Fully Integrated Injection-Locked Picosecond Pulse Receiver for 0.29ps$_{rms}$-Jitter Wireless Clock Synchronization in 65nm CMOS

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***Abstract*—This paper reports a picosecond pulse receiver based on a three-stage divide-by-8 injection-locked frequency divider. The receiver operates for pulses with center frequency of 77 GHz and locks its output to the 9.6-GHz repetition rate with an effective locking range of 142 MHz. This receiver, which consumes 42 mW dc power, is used to demonstrate wireless clock synchronization with a 0.29ps RMS timing jitter and indicates an estimated sensitivity of −65.5 dBm in detecting picosecond pulses.**

***Index Terms*—CMOS, impulse receiver, injection-locking, millimeter-wave, on-chip antennas, phase noise, time transfer, timing jitter, wireless synchronization.**

I. Introduction

Ultra-short pulses are envisioned as a promising solution for short-range wireless communication, imaging radars, broadband spectroscopy, and precision localization due to their large bandwidth and short time duration. Pulse-based systems could be immune to multi-path interferences due to distortion of the pulse shape caused by such effects. Furthermore, the wide bandwidth of a pulse spreads the power into plenty of low-power frequency tones which eases their coexistence with other narrowband systems. UWB systems have been presented over the past decade to accomplish these applications [1–2]. These pulses are usually as short as 1 ns and occupy the frequency band of 3.1 GHz to 10.6 GHz. More recently, picosecond pulses in the mm-wave regime have been used to achieve larger bandwidth, higher data rate, and better imaging resolution [3]. In order to implement imaging and localization systems using picosecond pulses, high-accuracy wireless time transfer needs to be performed among separate chips to synchronize them. Wireless synchronization enables us to build widely-spaced imaging arrays that can enhance the angular resolution of the image by increasing the aperture size. It also enables precise localization systems based on time of arrival of the picosecond pulses. Fig. 1 illustrates a picosecond pulse radar, time-domain and frequency-domain shapes of picosecond pulses, and the architecture of the reported picosecond pulse receiver for wireless synchronization of the repetition rate (clock) of a pulse train.

II. Proposed Architecture

In the past, several methods have been utilized to synchronize a system to a received pulse. Digital techniques, such as that described in [1], cannot be pushed to higher frequencies to detect and synchronize picosecond pulses. Self-mixing or direct detection methods, such as in [4], can potentially cover a wider range of frequencies but are prone to noise. In [2], an injection-locking scheme was used to lock a VCO to the clock of the UWB pulses while exposing the VCO to all the received frequency tones. In the presented receiver, only one high-power tone of the pulse is used to lock the VCO and is divided down to the repetition frequency of the pulse (f_{rep}). Since f_{rep} can be as high as few GHz for picosecond pulses, we have the ability to select only one tone to lock the VCO and, unlike [2], prevent the adjacent tones from pulling the oscillator frequency. In this architecture, shown in Fig. 1, a high-power tone near the center frequency of the pulse (~80 GHz) is selected and amplified to injection-lock a chain of three cross-coupled oscillators at frequencies of 40, 20, and 10 GHz. Assuming the repetition rate of the pulse is within the locking range around 10 GHz, the receiver output will be locked to the received pulses with low jitter. According to [5], the locking range of an injected cross-coupled frequency divider is approximated as

$$\omega_{\mathrm{L}} \approx \frac{\omega_0}{2Q} \times \frac{K.I_{\mathrm{inj}}}{I_{\mathrm{osc}}} \qquad (1)$$

where ω_{L} denotes the locking range of the oscillator, ω_0 is the resonance frequency, Q is the tank quality factor, I_{inj} and I_{osc} are the injection and the oscillation currents, and K is the conversion gain of the mixer created by the cross-coupled transistors that convert the injected frequency to the oscillation frequency. If a single-stage divide-by-8 divider is implemented, more injected power is required to have the same locking range as the presented three-stage architecture, due to a lower K. Therefore, three stages of divide-by-2 frequency dividers form a more practical solution when the injected power is limited, such as in broadband picosecond pulses. Other frequency dividers, such as CML, have limited bandwidths which make them ineffective for an 80-GHz input.

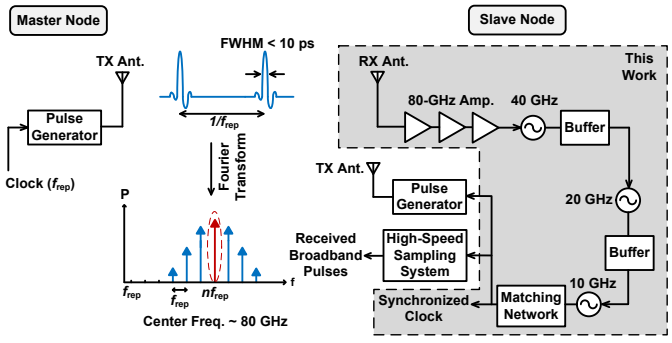

Figure 1. Master and slave nodes of a wirelessly synchronized distributed picosecond pulse array and the architecture of the receiver used for pulse-based wireless clock synchronization.

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The complete schematic of the designed receiver is shown in Fig. 2. An on-chip planar inverted-cone antenna is used to capture the broadband pulses centered at 80 GHz. The antenna is designed to exhibit a wideband operation while maintaining a broad radiation pattern. Due to the low efficiency of on-chip antennas caused by substrate modes in a silicon substrate, a 250μm-thick undoped silicon wafer and a silicon lens with a diameter of 6 mm are mounted on the back side of the board to increase the radiation efficiency. The parameters of the LNA are optimized to have the peak gain at 80 GHz while being unconditionally stable. The 80-GHz VCO is implemented with transmission lines in its LC tank but the other two oscillators are designed with symmetric inductors. Three tuning voltages (V_1, V_2, and V_3) are provided to control the resonance frequencies of these VCOs. These voltages may be tuned to adjust the center frequencies of the VCOs so that each VCO is able to lock the next one. The output of the chip can be locked to the received signal as long as all three VCOs are locked to each other. This receiver is fabricated in a 65nm LP CMOS process and occupies a total area of 0.9 mm^2, including the pads and the on-chip antenna.

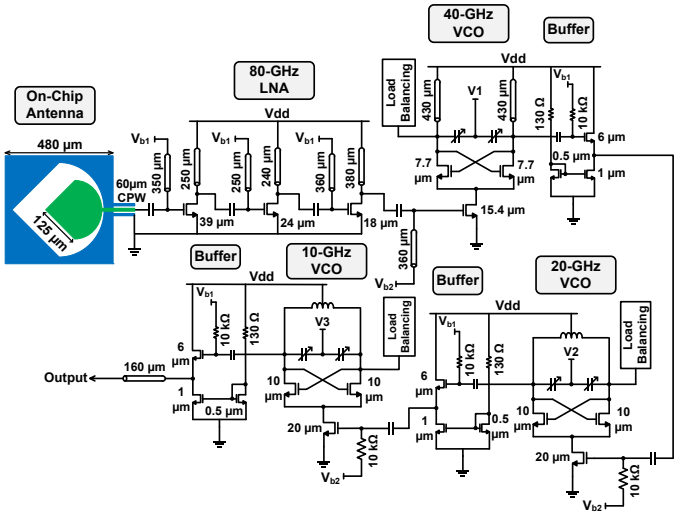

Figure 2. Schematics of the receiver.

III. Measurements

A. Receiver Characterization

A test setup with a single-tone continuous-wave source, shown in Fig. 3, is used to observe the free-running behavior of the receiver and to characterize its tuning and locking ranges. A Keysight E8257 signal source generates a signal in the K_u band (more specifically 12.5–13 GHz) which is applied to a Millitech active multiplier chain (AMC-10-RFHB0). The multiplier operates with a nominal +3dBm input power and produces a signal in the W band (75–110 GHz). A Millitech W-band pyramidal horn antenna (SGH-10) with +24dB gain radiates this signal towards the receiver. The receiver chip is mounted and wire-bonded to a board, through which the output is connected to a Keysight N9030A spectrum analyzer.

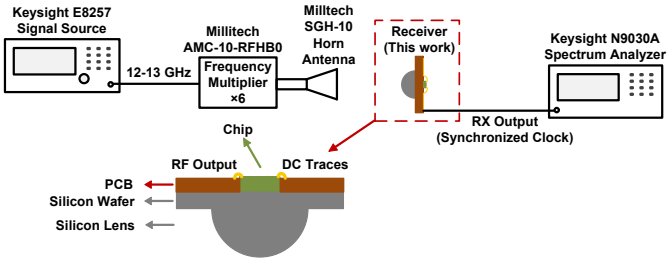

Figure 3. Measurement setup for characterizing the receiver.

The measured tuning range of the output is plotted in Fig. 4(a). It shows that for every VCO tuning voltage, the output frequency varies in two different modes. When each oscillator is locked to its previous one, the output frequency can be proportionally tuned by tuning the previous stages. Whereas, in the free-running mode, the last oscillator stage is solely tuned by its own tuning voltage. In the latter mode, the tuning range can be as high as 400 MHz centered at 9.8 GHz. Fig. 4(b) shows the measured locking range of the receiver output at a 5-mm distance between the horn antenna and the receiver. The measured locking range is smaller than a single cross-coupled VCO since it is limited to the overlap of the locking ranges of three VCOs. Due to the tuning capability of the VCOs, it is possible to achieve a wider locking range by adjusting the tuning voltage of the three VCOs. In this work, the effective locking range of the output can be as high as 141 MHz when the tuning voltages are adjusted accordingly (Fig. 4(c)).

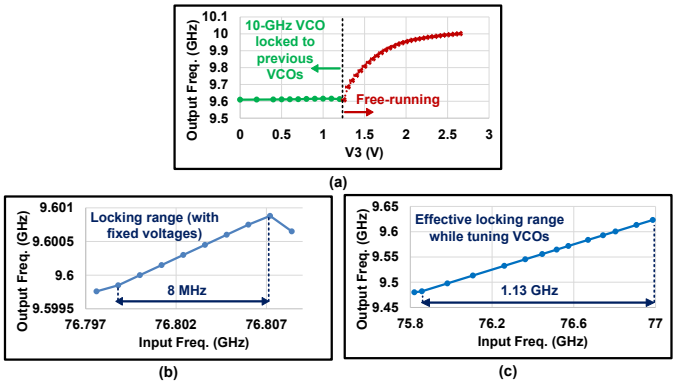

Figure 4. (a) Measured tuning range of the receiver. (b) Measured locking range. (c) Measured effective tuning range.

B. Wireless Synchronization with Picosecond Pulses

A silicon-based pulse-radiating chip with the capability of radiating pulses as short as a few picoseconds is used in another test setup, shown in Fig. 5(a), to demonstrate the performance of the receiver for low-jitter wireless clock synchronization. The pulse generator is triggered by the signal source, which sets the repetition rate of the radiated pulses. In this test, we operate the source with a 4.8GHz rate while the free-running frequency of the receiver is tuned at 9.601 GHz. The measured free-running and locked spectrum of the receiver output as well as a phase noise comparison are reported in Fig. 6(a) and 6(b). The effect of bond wire and cable losses at 10 GHz make the

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TABLE I

COMPARISON WITH OTHER SILICON CHIPS USED FOR WIRELESS PRECISION CLOCK SYNCHRONIZATION.

	[1]	[2]	[4]	[6]	**This Work**
Process	180nm CMOS	90nm CMOS	130nm SiGe BiCMOS	130nm CMOS	65nm CMOS
Wireless Source	UWB Pulse (3 GHz)	UWB Pulse (4 GHz)	Picosecond Pulse (50 GHz)	CW (18 GHz)	**Picosecond Pulse (80 GHz)**
RMS Jitter [ps]	4.6	7.6	0.4	5 (pk-pk)	**0.29**
Clock Frequency [GHz]	3	0.5	3.1	2.25	**9.6**
Clock Range [GHz]	Not tunable	0.07	9	0.202	0.14
Maximum Measurement Distance [mm]	0.5	200	100*	2.5	30**
Sensitivity [dBm]	N/A	−64	N/A	N/A	**−65.5**
On-Chip Antenna	Yes	No	Yes	Yes	**Yes**
Active Area [mm^2]	0.54	2***	1.89***	1.14	**0.46**
DC Power [mW]	43	45	146	80	**41.6**

* A lens was used between the TX and the RX.

** Limited to transmitter power. RX sensitivity is better than [2].

*** Total area including the pads.

measured power lower than its actual value. The locked output of the receiver has a −85dBc/Hz phase noise at the offset frequency of 10 kHz. The free-running output has a phase noise of −50 dBc/Hz at the same offset.

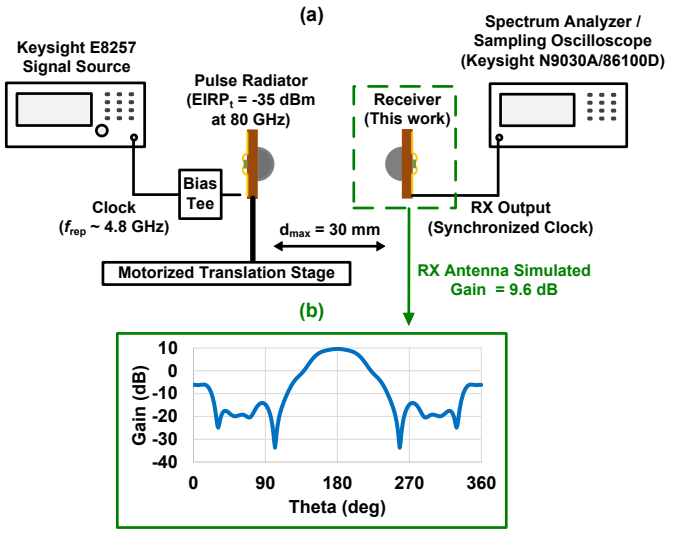

Figure 5. (a) Wireless synchronization setup with a picosecond pulse source. (b) Simulated gain of the on-chip antenna with lens at 80 GHz.

The maximum distance to see the locking behavior is 30 mm as we are limited to a measured EIRP of −35 dBm from the transmitter at 80 GHz. Friis transmission equation is used to estimate the sensitivity of the receiver:

$$P_{\mathrm{r,min}} = EIRP_{\mathrm{t}} + G_{\mathrm{r}} + 20\log\left(\frac{\lambda}{4\pi R_{\max}}\right) \qquad (2)$$

where $EIRP_{\mathrm{t}}$ is the equivalent isotropically radiated power of the transmitter, G_{r} is the gain of the receiver antenna, and λ is the operating wavelength. Based on equation (2) and the antenna gain, simulated with CST (Fig. 5(b)), the estimated sensitivity of the receiver is −65.5 dBm. The time-domain waveform of the output is shown in Fig. 6(c) and 6(d), indicates an RMS jitter of 290 fs for the synchronized output. This jitter should be compared with the jitter of the signal source used to trigger the pulse generator, which is 260 fs, measured at the same frequency, same power level, and with the same averaging number of 64. The small added jitter is the combined effect of the receiver chip, the pulse generator chip, and the channel.

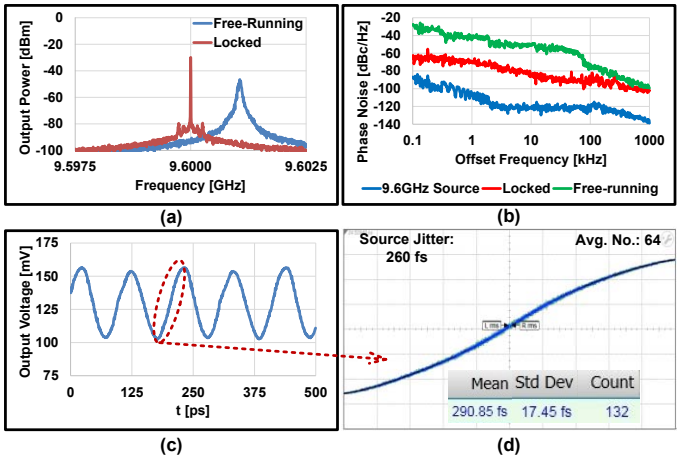

Figure 6. Measured time-domain and frequency-domain results of the wireless clock synchronization using picosecond pulses.

IV. CONCLUSION

The fabricated pulse receiver consumes a DC power of 42 mW from a 1.3-V power supply. The performance of this three-stage injection-locked receiver is compared with other continuous-wave or pulse-based receivers used for wireless clock synchronization in Table I, indicating that this receiver achieves the smallest RMS jitter in timing synchronization and

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a high sensitivity in detecting picosecond pulses. The die micrograph of the receiver is shown in Fig. 7.

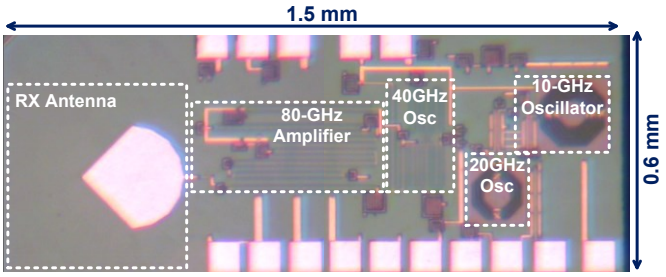

Figure 7. Chip micrograph of the receiver.

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