An Efficient Adder Architecture with Three-Independent-Gate Field-Effect Transistors

Jorge Romero González
Department of Electrical and Computer Engineering
University of Utah
Salt Lake City, Utah, 84112
Email: jorge.romerogonzalez@utah.edu

Pierre-Emmanuel Gaillardon
Department of Electrical and Computer Engineering
University of Utah
Salt Lake City, Utah, 84112
Email: pierre-emmanuel.gaillardon@utah.edu

***Abstract*—Three-Independent-Gate Field-Effect Transistors (TIGFETs) extend the functional diversity of a single transistor by allowing a dynamic electric reconfiguration of the polarity. This property has been shown to unlock unique circuit level opportunities. In this article, a ripple-carry 32-bit adder is uniquely designed using simulated TIGFET technology and its metrics are compared against CMOS *High-Performance* (HP) and CMOS Low-Voltage. By adopting TIGFET's polarity control characteristic, the proposed ripple-carry adder architecture uses efficient exclusive OR and majority gates to compute complementary carry signals in parallel, leading to a 38% decrease in logic depth as compared to the standard CMOS design. Additionally, a 38% reduction in contacted gates reduces the effects coming from an interconnect-limited design. The results show that the decrease in the logic depth and the reduction in contacted gates lead to a 3.8× lower energy-delay product and a 5.6× lower area-delay product as compared with CMOS HP. The boost in performance coming from realizing arithmetic circuits with TIGFET transistors makes them a promising next-generation high-performance device technology.**

I. Introduction

Successful scaling of *Complementary Metal-Oxide-Semiconductor* (CMOS) *Field-Effect Transistors* (FETs) has reached the nanometer regime with remarkable improvements in the switching speed, density, and power of highly integrated circuits. Recent advances in CMOS technology has utilized innovative high-mobility channel materials and non-planar device structures to further increase device performance. The *International Technology Roadmap for Semiconductors (ITRS)* [1] was launched to map future generations and developed a roadmap for Research and Development (R&D) targets for the following years. Predictions of a scaling bottleneck at the 5-nm node gave the increasing urgency to find device technologies that may replace CMOS in the near future.

Novel emerging logic technologies allow for different transport mechanisms, gating mechanisms or switching variables not seen in standard MOSFETs. While these alternative transistors do not yet have the proper momentum for full integration into leading chip manufacturers, some do have the potential to lead future generations. As a candidate for highly energy-efficient devices, *Carbon Nanotube FETs* (CNFETs) are expected to achieve a higher *energy-delay product* (EDP) than CMOS [2] coming from their high mobility and low power supply capabilities. Notable for reducing short channel effects, FETs with 2-D channel materials from the transition-metal-dichalconides family [3, 4] can result in high-performing devices due to their enhanced ON-current characteristics [5]. *Negative-Capacitance FETs* (NCFETs) [6] use the negative capacitance of a ferroelectric layer to provide voltage amplification and achieve sub 60mV/decade subthreshold slope. Similarly, *Tunnel FETs* (TFETs) [7] utilize quantum-mechanical band-to-band tunneling at the device-level to achieve rapid switching and offer improved ON-current / OFF-current ratios. In particular, the *Heterojunction II-V TFETs* (HetJFETs) [8] and the *van der Walls FET* (vdWFET) [9] are expected to reduce the switching energy and provide a higher throughput than CMOS *High-Performance* (HP) [10].

As an attempt to eliminate ambipolar characteristics in Schottky-barrier CNFETs [11], dual-gate CNFETs [12] unveiled reconfigurable (electrostatic doping) technology. This allowed for pure n-type and p-type characteristics to be obtained from an ambipolar device. To exploit electrostatic doping properties in silicon, *Three-Independent Gate FET* (TIGFET) technology uses three MOS gate terminals on a semiconducting channel and Schottky barriers at source and drain [13]. At the device-level, TIGFET devices see a functionality increase with (1) the dynamic reconfiguration of the polarity (n-type or p- type) by utilizing the independent control of the gates [14], (2) the dynamic control of the subthreshold slope due to a positive feedback induced by weak impact ionization [15], and (3) the dynamic control of the threshold voltage by the operation of two switching mechanisms (thermally-assisted tunneling through Schottky barriers or carrier transport similar to conventional MOSFETs) [13]. At the circuit-level, TIGFET's dynamic control of the polarity allows for novel circuit architectures that lead to beneficial performance metrics [16–22].

The addition of two binary words is an essential operation of any arithmetic logic unit. Designing efficient adders is crucial to increase the performance of processors as adders are often used for complex multiplication and division operations. In this paper, TIGFET technology is used to develop a novel adder architecture that can only be realized with efficient exclusive OR (XOR) and majority (MAJ) circuits. The design adopts (1) 16 TIGFET transistors rather than 44 MOSFET transistors per adder stage and (2) the parallel propagation of complementary carry signals. Multiple adder implementations have been researched to reduce the area, speed, or power [23]. These include the ripple-carry, carry-look-ahead,

carry-select, and carry-skip. The ripple-carry adder (RCA) is commonly used in digital signal processing systems, such as in *arithmetic logic units* (ALUs) [24–26] and *adaptive logic modules* (ALMs) [27] for *Field Programable Gate Arrays* (FPGAs), where the design specifications may require a reduction in power and area at the expense of increased delay. This paper redesigns CMOS' RCA with the help of TIGFET technology and presents a novel ripple-based carry adder architecture that reduces the logic depth and achieves significant reductions in delay and area. In particular, for the 32-bit adder, TIGFET technology consumes 3.83× (4.18×) lower EDP, 5.60× (51.9×) lower ADP, 53.8× lower (1.65× larger) standby power, 150× (15.4×) lower standby energy, and 1.39× (2.31×) higher throughput as compared with CMOS HP (CMOS LV).

The remainder of this paper is organized as follows. Section II discusses background material of TIGFET technology. The arithmetic architecture for TIGFET technology is shown in Section III. The results are outlined in Section IV and the paper is concluded in Section V.

II. Background

In this section, we briefly review polarity controllable technologies and the device structure, working principle, logic behavior and gate-level opportunities of the TIGFET technology.

A. Generalities

Reconfigurable transistors are able to configure their electrostatic properties to behave as efficient n-type or a p-type device. They utilize multiple MOS gates on a metal-semiconductor-metal heterostructure channel. The first attempt at a polarity controllable device used three gated regions on a carbon nanotube channel [12]. This device was shown to exhibit symmetric n-type and p-type ON-currents, excellent OFF-state currents, and the steepest subthreshold slope for nanotube devices (63 mV/dec). The first reconfigurable silicon-based device used two gated regions on a $NiSi_2$-Si-$NiSi_2$ channel [28]. These devices captured dual-polarity characteristics with large $> 1 \times 10^9$ I_{ON}/I_{OFF} ratio. The natural extension of the dual-gate reconfigurable Si-based device is to utilize three gates on a Si channel as shown in Fig. 1.

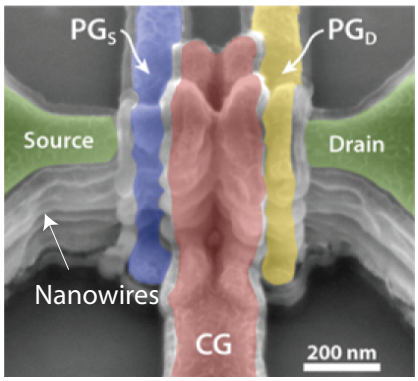

Fig. 1: Scanning electron microscope image of a fabricated silicon-nanowire-based TIGFET device [13]. The channel structure contains four vertically stacked silicon nanowires between nickel silicide source and drain pillars.

By independently controlling all three MOS gates, the *Three-Independent-Gate FET* (TIGFET) technology offers novel device-level functionalities [13]. The structure shown in Fig. 1 is composed of three MOS gate electrodes with CG at the center and *Polarity Gate at Source* (PGS) and *Polarity Gate at Drain* (PGD) near the source and drain, respectively. The channel has a metal-semiconductor-metal composition resulting in Schottky barriers at the source and drain. The potential at PGS and PGD modulate the Schottky junction's effective barrier height to (respectively) allow electrons or holes to flow into the channel. Modulating the Schottky barriers' properties grants electrostatic control of the device polarity not possible with conventional MOSFETs. To enable n-type and p-type symmetrical currents, mid-gap workfunction of the source and drain metals must be designed. NiSi-Si-NiSi compositions can be grown to achieve this condition [14]. The potential at CG turns the device ON or OFF by modulating a potential barrier in the center of a channel, similar to the gate of a MOSFET.

The TIGFET technology can be applied to a variety of device structures and semiconductor materials with mid-gap workfunction metals. In particular, silicon nanowire structures [13, 28], silicon fin structures [15], 2D materials [29–31], and carbon nanotubes [12] have been fabricated with three-terminal technologies. Vertically stacked nanowires [32–35] have proven to increase the drive current in TIGFET technology. In this paper, a single nanowire-based NiSi-Si-NiSi device has been considered for the reconfigurable technology for its simpler device structure and performance.

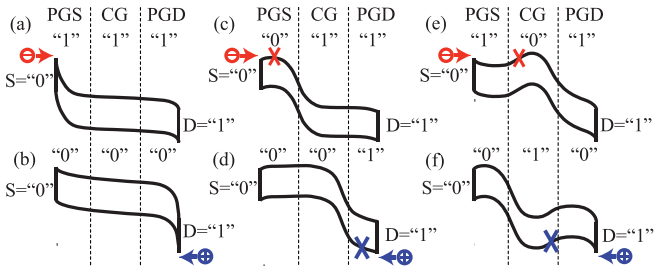

Fig. 2: Band diagrams under different bias conditions. (a)(b) ON-state, (c)(d) OFF-state due to PGS/PGD control, (e)(f) OFF-state due to CG control.

B. Working Principle

TIGFET transistors have two forms of switching mechanisms. First, the potential at PGS or PGD allow for thermally-assisted tunneling through the Schottky barriers. If there exists a large enough potential difference between PGS and source, then the Schottky barriers become thin enough to allow electrons to flow into the channel as shown in the band diagrams of Fig. 2(a). The same is true for a large potential between PGD and drain to allow holes to flow into the channel as shown in the band diagrams of Fig. 2(b). When the potential difference between PGS and source or PGD and drain is zero, carriers do not flow through the Schottky junctions and the device is in the OFF-state as shown in the band diagrams of Fig. 2(c)(d). The second switching mechanism is through the control of the CG gate. Similarly to the gate of a MOSFET, the

CG gate creates a potential barrier in the center of the channel region to control the flow of the current. The OFF-state of this switching mechanism is shown in Fig. 2(e)(f) while the ON state is shown in Fig. 2(a)(b).

An abstract symbolic representation of the TIGFET technology is shown in Fig. 3. The single TIGFET transistor with potentials PGS, CG, and PGD at the gates is shown in Fig. 3(a). The PGD switching control (using thermally assisted tunneling through the Schottky barriers) creates a unipolar n-type device when PGS and CG are set high as shown in Fig. 3(b). The CG switching control (by modifying the carrier diffusion into the channel) similarly creates a unipolar n-type device when the polarity gates are set high, as shown in Fig. 3(c). The TIGFET devices can behave as p-type transistors if the gates are set low (rather than high). Lastly, when the potential at PGD is set high, the TIGFET transistor represents two n-type devices in series with CG and PGD as the gates, as shown in Fig. 3(d). On the other hand, if PGS is set low, then the TIGFET transistor behaves as two p-type transistors in series with CG and PGS as the gates.

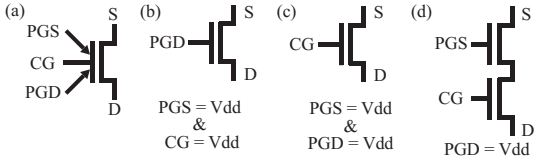

Fig. 3: (a) The symbol representation of a TIGFET device. (b) PGD control of the nFET channel. (c) CG control of the nFET channel. (d) Series nFET transistors with CG and PGD at gate.

C. Logic Gate-level Opportunities

The circuit opportunities of TIGFET technology has been largely investigated in literature [16–22]. First, TIGFET technology can emulate regular MOSFETs by realizing unipolar n-type and p-type devices when both polarity gates (PGS and PGD) are fixed to a constant bias. This property allows for a CMOS-style TIGFET circuit design obtained by a 1-to-1 replacement of MOSFETs with TIGFETs. As an illustration, Fig. 4(a) depicts an inverter designed using one n-type and one p-type TIGFET device in the pull-down and pull-up networks of the inverter, respectively. Second, the capability of TIGFET technology to emulate two series n-type (or p-type) MOSFETs with a single TIGFET transistor allows for device merging. This property leads to a reduction of TIGFET transistors at the gate-level. For instance, the pull-down network of a CMOS-style two-input NAND contains two n-type MOSFETs. As such, the pull-down network of a TIGFET-style two-input NAND will contain one TIGFET transistor with PGD set high while the pull-up network will contain a 1-to-1 replacement of MOSFETs with TIGFETs. The two-input NAND can therefore be mapped using three TIGFET transistors as shown in Fig. 4(b). Third, TIGFETs can be electrically reconfigured as an n-type or p-type device by placing input signals at the polarity gates (PGS and PGD). This polarity control property leads to innovative circuit-level opportunities not possible with MOSFETs. For instance, Fig. 4(c) shows the realization of a three-input XOR gate $((A \oplus B) \oplus C)$ by utilizing four TIGFET transistors (plus two inverters) rather than 16 MOSFET transistors from standard CMOS design. In addition, Fig. 4(d) shows the realization of a TIGFET-based three-input MAJ gate $(MAJ(A, B, C))$ with four transistors (plus two inverters) rather than 24 MOSFET transistors from standard CMOS design. These circuit realizations allow for higher-level circuit architecture to be designed, such as the novel adder architecture with TIGFET technology reported in Sec. III. We refer the reader to [18–22] for further circuit opportunities with TIGFET technology such as dual-V_T inverter, dual-V_T NAND, 4-1 static multiplexer, 6T static random-access memory, true single phase clocking flip-flop, multiplexers and power-gated differential cascade voltage switch logic.

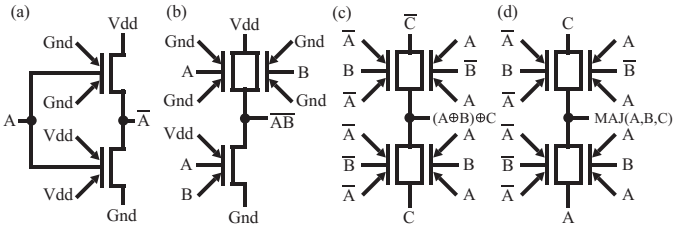

Fig. 4: TIGFET circuit representations of (a) an inverter, (b) a two-input NAND gate, (c) a three-input XOR gate, and (d) a three-input MAJ gate

III. TIGFET's Ripple-Carry Adder Architecture

The addition operation is a fundamental component of all arithmetic logic units and is often used as a primitive to perform complex operations such as multiplication and division. The ripple-carry adder (RCA), as the most straightforward implementation, is commonly used in digital signal processing systems where ALUs [24–26] and ALMs [27] are needed. While the application of these adders are low-power consumption, they may suffer from high delays. This gives us the motivation to modify the ripple-carry adder with TIGFET technology and achieve reductions in logic depth and transistor count.

A. TIGFET-Based 1-Bit Full-Adder Design

A 1-bit full-adder with TIGFET technology can be designed using XOR/MAJ gates as shown in Fig. 5. The input signals are A, B, and carry-in (Cin) while the output signals are summation (Sum) and carry-out ($Cout$). The Sum signal is calculated to be $(A \oplus B) \oplus Cin$ by applying a three-input XOR and the $Cout$ signal is calculated to be majority of the inputs $(MAJ(A, B, Cin))$ by applying a three-input MAJ gate as shown in Fig. 5. Three inverters are added to the adder to invert the input signals. The proposed design only uses 14 transistors and shortens the critical path - passing through one inverter and parallel Sum and $Cout$ gates, implemented by compact three-input XOR and the three-input MAJ gates. TIGFETs are already of interest in such structure as this allows an interesting compactness for implementing a full-adder.

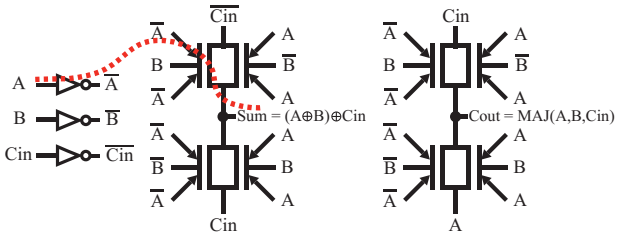

Fig. 5: The novel gate full-adder design with three inverters to invert A, B, and Cin, one three-input XOR gate to output Sum, and one three-input MAJ gate to output $Cout$. The resulting critical signal is shown in red.

B. Optimized Adder Architecture with TIGFET Technology

In the previous case, the $\overline{Cin}$ signal is computed from Cin with an inverter at every stage. In order to reduce the logic depth, one can imagine to compute both regular and complimented carry signals at every stage and propagate those signals to the next stage. Unfortunately, the parallel computation of the complementary carry signals ($Cout$ and $\overline{Cout}$) with CMOS is prohibited since the carry circuits are expensive. However, TIGFET-based XOR and MAJ gates are cheap to produce with only four TIGFET transistors each. Therefore, the $\overline{Cout}$ signal can be computed by using an additional three-input MAJ gate with $\overline{A}$, $\overline{B}$, and $\overline{Cin}$ as the inputs. The 1-bit full adder shown in Fig. 6 uses two 3-input MAJ gates to simultaneously compute both regular and inverted carry signals. This comes with a low additional area cost (only two more transistors per stage) and low additional energy cost (difference between the three-input MAJ gate and the inverter). If this full adder is used as a stage for an n-bit adder, then the inverter contribution of the critical signal at each stage level is removed and this leads to a reduction in the logic depth from $2n$ to $n+1$ (taking into account the inverter to invert the initial Cin).

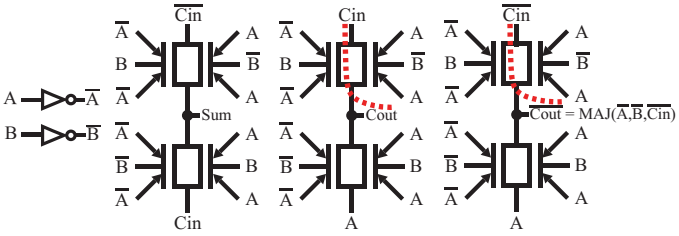

Fig. 6: A single stage of an n-bit adder showing the parallel computation of $\overline{Cout}$ by $MAJ(\overline{A},\overline{B},\overline{Cin})$. The resulting critical signal is shown in red.

The resulting critical path of an n-bit adder goes through a single inverter (all inputs (A_n and B_n) are inverted in parallel at the beginning) and goes through the parallel propagation of $Cout$ and $\overline{Cout}$ through all n-stages as shown in Fig. 7. The propagation of the carry signals passes through TIGFET's transmission gate logic and requires an inverter to be added for every five stages to account for degraded signals. The total logic depth is $6/5n+1$ for the optimized 32-bit adder.

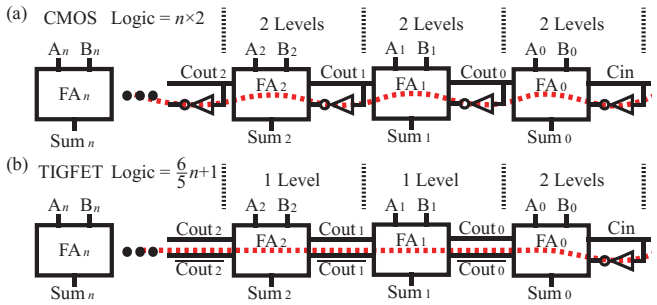

Fig. 7: (a) CMOS' stage diagram for the n-bit ripple-carry adder and (b) TIGFET's stage diagram for the optimized adder architecture. The logic depths are shown per stage and the resulting critical signal is shown in red.

IV. Experimental Evaluation

In this section, the extraction of TIGFET's device-level characteristics is outlined using a 15-nm silicon-nanowire-based structure. The benchmarking results are presented for TIGFET's optimized 32-bit adder and the origin explanation of the EDP and the *Area-Delay-Product* ADP for the multiple 32-bit adder TIGFET architectures are given.

A. TIGFET Predictive Device Evaluation

To evaluate the performance of TIGFET technology, we employed the Beyond-CMOS Benchmarking (BCB) [10, 36–38] methodology. Started by the Nanoelectric Research Initiative, the BCB methodology [10] now contains a large range of circuits with various metrics and uses a full set of guidelines to obtain data from the device community. For the arithmetic architecture metric, the BCB methodology contains evaluations in the area, delay, energy, and power of the 32-bit ripple-carry adder. In order to establish a method to estimate these performance metrics, various adjustment parameters were simulated in the BCB methodology that are common for non-tunneling based technologies [10]. To put the TIGFET transistor in the BCB methodology in a fair way, several device-level characteristics must be evaluated under the same physical design considerations as the CMOS HP device. These building blocks include calculating the area, the ON-current density (J_{ON}), the OFF-current density (J_{OFF}), the nominal voltage (V_{DD}), and the parasitic capacitance of the intrinsic transistor. The device geometry of the TIGFET transistor, as shown in Fig. 8, uses the same standard design rules followed in the BCB methodology [10] (ITRS's 15 nm technology node [1]). The length of the gates and the separation between the MOS gates were set to 15 nm and a dielectric layer (HfO_2) of 6.92 nm was used. The channel structure was a 8 nm silicon nanowire.

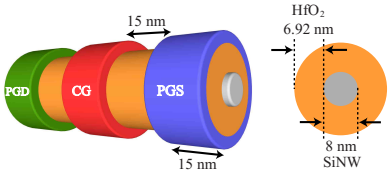

Fig. 8: Experimental drawing of the TIG SiNWFET.

TCAD Sentaurus from Synopsys was used to determine the current densities and nominal voltage of the SiNW-based TIGFET device using classical semiconductor properties. A SiNW MOSFET (with well-designed short channel effects [39] and channel dimensions) was simulated in parallel to the TIGFET device in order to establish a proper baseline comparison. The ON-current density and OFF-current density was calculated to be $J_{ON} = 501\ \mu A/\mu m$, and $J_{OFF} = 3.8\ nA/\mu m$ with $V_{DD} = 0.9V$. The I-V curve that was extracted from TCAD Sentaurus, as shown in Fig. 9, illustrates the electrical reconfiguration of the polarity (between n-type and p-type).

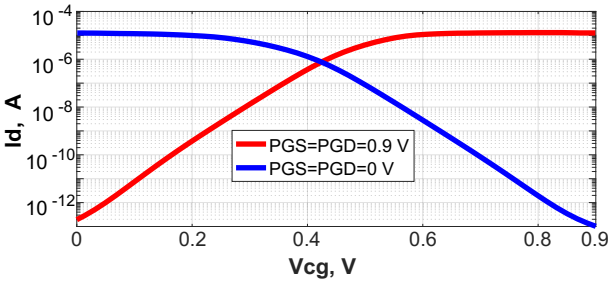

Fig. 9: Drain current (I_D) versus CG voltage (V_{CG}) for the SiNW-based TIGFET at $V_{DD} = 0.9\ V$. The red and blue curves indicate the nMOS and pMOS realization, respectively [22].

3D Poisson electrostatic simulations were performed in COMSOL Multiphysics to determine the parasitic and intrinsic capacitances of the SiNW-based TIGFET device. The extracted capacitances are shown in Fig. 11 for the multiple modes of TIGFET operations [22]. The forth mode of operation as shown in Fig. 11(d) gives a maximum total capacitance of 1.24×10^{-16} F. A similar baseline comparison was made here between TIGFET and CMOS HP (finFET). The results show that this value is approximately twice as large as the total capacitance of the simulated silicon fin-based CMOS HP device. In order to mitigate routing bottlenecks, coming from the two additional contacted MOS gates per TIGFET device, a Sea-of-Tile design [35] is implemented in this work to achieve similar routing efficiency as CMOS technology [40]. We refer the reader to [22] for the layout design for TIGFET technology that is used in this work.

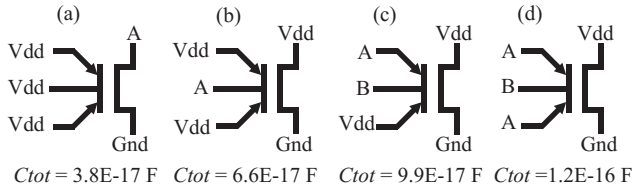

Fig. 11: The total capacitance (C_{tot}) for the multiple modes of operation. A and B correspond to different inputs. The transistors in (a), (b), and (c) are nFET configurations. The input gates set to VDD may be set to GND for the pFET configurations.

B. Adder Architecture Results

The benchmarking comparison between TIGFET's optimized adder architecture and several other beyond-CMOS devices are shown in Fig. 10 for the 32-bit adder. The electrical circuit estimations include the switching delay, switching energy, active power, standby power, standby energy, power density and throughput.

The switching delay is the time that it takes for the signal to transmit through the critical path of the 32-bit adder and is equal to the total capacitance times the supply voltage divided by the ON-current. This metric is important as it shows how fast the circuit cycles. The switching energy, on the other hand, is the energy consumed per the adder cycle. This term can be similarly calculated by multiplying the total capacitance by the supply voltage squared. The switching energy versus switching delay plot is shown in Fig. 10(a). While the dashed lines show the constant EDP trend, the preferred corner is bottom left as this corresponds to devices with low energy consumption and fast switching (lower EDP values). This plot gives TIGFET technology a 3.83× lower EDP as compared with CMOS HP and a 4.18× lower EDP as compared with CMOS LV. While TIGFETs are shown to have the best EDP for the 32-bit adder, other alternative technologies have similar promising EDP metrics. In particular, the tunnel FETs show lower EDP than both CMOS technologies - coming from their low supply voltage and relatively large ON-current / OFF-current ratios.

The active power is the power of the active circuit, expressed as the switching energy divided by the switching delay. On the other hand, the standby power is the power consumed in the off state, calculated by the supply voltage times the OFF-current. These two power metrics are plotted in Fig. 10(b). The 53.8× lower standby power between TIGFET and CMOS HP comes from TIGFETs low OFF-current as compared with CMOS HP. CMOS LV shows 1.65× lower standby power as compared with TIGFETs due to its low-voltage supply and low OFF-current metrics. The increase in active power in TIGFET technology comes from having faster switching speeds while having a similar switching energy as compared with CMOS HP. The results coming from the steep-slope devices (in white and blue) come as expected. As the devices offer smaller supply voltage, their OFF-current decreases and this leads to smaller standby components. It is also worth pointing out that the spin-based device (SWD) [41] here allows for ultra low voltage operation that leads to low power consumption.

Next, the standby energy is the energy consumed in the off state, calculated by the standby power times the switching delay. The switching energy and standby energy are plotted in Fig. 10(c) with the preferred corner at the bottom left. This plot gives TIGFET technology a 147× lower standby energy as compared with CMOS HP and a 15.4× lower standby energy as compared with CMOS LV. The TIGFET technology achieves lower standby energy as compared to most technologies. This is possible due to TIGFETs relatively low standby power at high switching speed.

Lastly, the power density and the throughput are plotted in Fig. 10(d). The throughput metric describes the useful work that can be performed by a circuit and is calculated by the

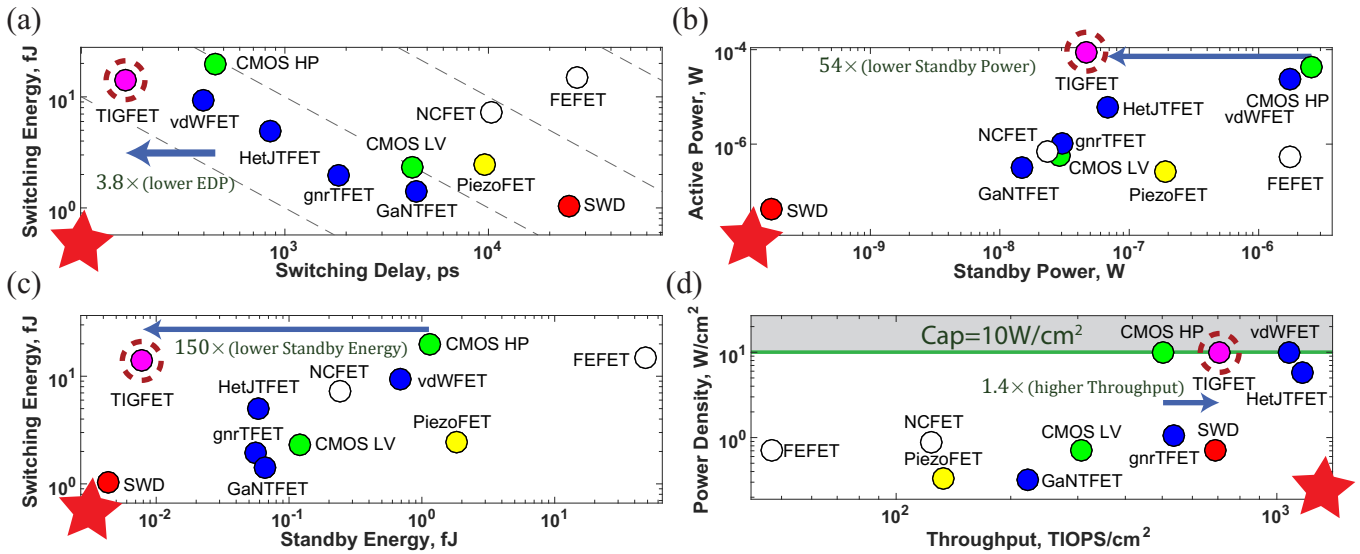

Fig. 10: Benchmark for the 32-bit adder. (a) Switching energy and switching delay. (b) Active power and standby power. (c) Switching energy and standby energy. (d) Power density and throughput. The red stars show the optimum corners.

inverse of the total area times the switching delay. The power density is the sum of the active power and the standby power divided by the total area. This is an important factor for chip design as it shows the amount of power consumed within the chip. The power density is capped at 10 W/cm^2. This was assumed in [37] to take into consideration the amount of power that can be removed by a heat sink in chips. The faster devices that consume the maximum power (TIGFETs, CMOS HP, and vdWFETs included) have, consequently, reduced throughput by decreasing the frequency when circuits run at high power densities. TIGFET technology experience 1.39× higher throughput as compared with CMOS HP and 2.31× higher throughput as compared with CMOS LV.

C. Breakdown Analysis of EDP and ADP

TIGFET's benchmarks show very promising results. However, this comes as a surprise since TIGFET's device-level characteristics can be deemed as "bad" compared with the CMOS technologies, as discussed in Sec. IV-A. A reasonable argument can be made here that shows the device-level functionality increase of TIGFET technology leads to efficient gates that, in turn, allow for high-performance arithmetic architectures. It is possible to explain where the performances are coming from for TIGFETs optimized RCA design by analyzing the different contributions at the device-level and at the gate-level. In this subsection, the EDP and ADP performances of the 32-bit adder (normalized to CMOS HP) are analyzed in detail with three different circuit scenarios as shown in Fig. 12: (1) The straightforward replacement of MOSFETs with TIGFETs, (2) the introduction of the three-input XOR and the three-input MAJ TIGFET gates as discussed Sec. III-A, and (3) the parallel generation of the complementary carry signals as proposed in Sec. III-B.

1) 1-to-1 Replacement: The 1-to-1 replacement of MOSFET transistors with TIGFET transistors is the simplest form of the 32-bit adder design. The CMOS-based adder, as used in this paper, is composed of two-input NAND gates. Since this design neglects the use of TIGFET's functionality increase, the performance sees a 15.8× increase in EDP and 2.67× increase in ADP as compared with CMOS HP. The increase in EDP and ADP is primarily due to TIGFETs 1.59× larger overall capacitance, reduced drive current (3.6× smaller), increased supply voltage (23% larger), and 1.97× larger adder design area. These performance results would normally impede further device development. However, this adder design does not take into consideration the functionality increase of TIGFET transistors.

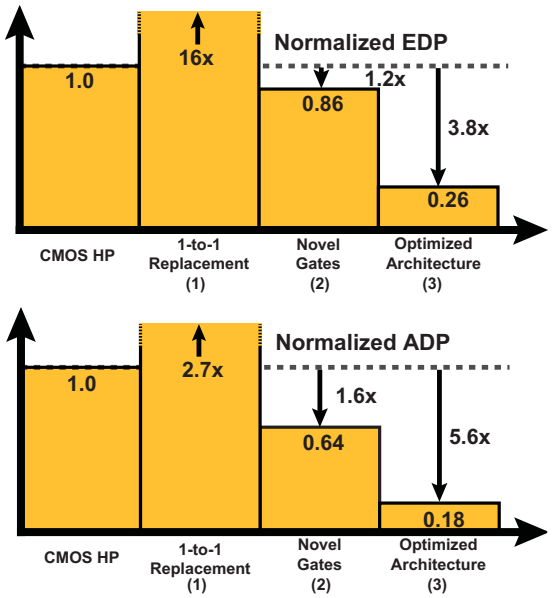

Fig. 12: Normalized EDP and normalized ADP for the 32-bit adder for CMOS HP using (1) the 1-to-1 replacement of MOSFETS with TIGFETs design, (2) the novel gates design, and (3) the novel adder architecture.

2) Full-Adder With Novel Gates: Next, the TIGFET's capability to produce efficient three-input XOR gates and three-input MAJ gates allows for the redesign of a 1-bit full-adder, as shown in Fig. 5. This single stage is used to construct an XOR/MAJ gate-based ripple-carry adder (containing three inverters per stage) and observe a 1.17× lower EDP and a 1.57× lower ADP as compared to CMOS HP. The increase in performance primarily comes from a reduction in the number of transistors (14 TIGFET transistors rather than 44 MOSFET transistors) which leads to 1.89× less contacted gates, 2.39× smaller 32-bit adder area, and 63% decrease in overall average capacitance as compared with CMOS HP.

3) Optimized Adder Architecture: In the previous adder architecture, the carry signal, i.e., the critical path, goes through 32 stages of the 1-bit adders. These adder stages contain inverters to generate $\overline{Cin}_n$. However, this design can be further improved by generating $\overline{Cin}_n$ using a second three-input MAJ gate, as shown in Fig. 6, resulting in a 3.83× improvement in EDP and a 5.60× improvement in ADP as compared with CMOS HP. This is primarily due to the parallel generation of both Cin_n and $\overline{Cin}_n$ which removes the carry inverters from the critical path - decreasing the logic depth by 38.4% while containing 2.05× smaller 32-bit adder area. Fig. 13 shows the EDP and ADP metrics for the optimized adder architecture as the number of bits are varied between 1 and 32 bits. The results show that the metrics favorably decrease as the number of bits increase. The initial decrease in EDP and ADP between the 1-bit and the 4-bit adder comes from the usage of a single inverter in the critical paths for the 1-bit and 4-bit adder. However, there is an increase in the number of inefficient inverters used for the degradation of signals at the 8-bit, 16-bit, and 32-bit adders. While this leads to a slow down in adder performance, both the EDP metric and the ADP metric for TIGFET technology display exceptional results for the 32-bit adder technology.

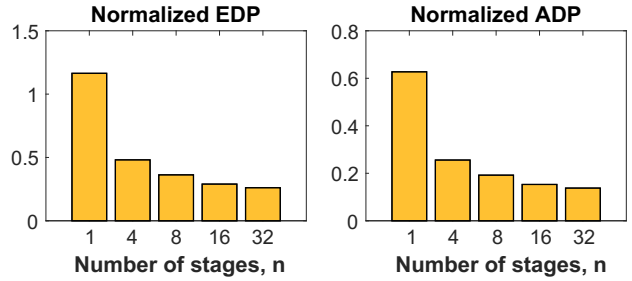

Fig. 13: The EDP and ADP metrics (normalized to CMOS HP) for TIGFET's novel adder architecture as a function of stage quantity.

4) Future Progress: TIGFETs bear the promise of improved robustness to process variations as identified in [42] as the source and drain doping is absent in reconfigurable technology. To increase the performance capabilities of TIGFET technology, the use of novel channel materials such as bi-layer WSe_2 has been experimentally demonstrated to increase the device-level performances [30]. An MX_2 simulated material reached a benefit of 7.2× larger EDP for the 32-bit adder by using $J_{ON} = 1500\,\mu A/\mu m$ and $>10^9$ ON/OFF current ratio at the 10-nm gate length [31], closing the gap with MOSFETs at the device-level and providing an adder with 2× benefit as compared with SiNW-based TIGFETs, as consistent with [43].

V. Conclusion

In this paper, a ripple-carry 32-bit adder architecture is investigated using TIGFET technology as an effort to appropriately illustrate the benefits of TIGFET's functionality increase and compare its performances with CMOS HP and CMOS LV. The same feature size, channel material, and oxide thickness was used to ensure a full compatibility with standard CMOS processes. Additionally, the TIGFET technology can benefit from traditional technology node scaling (oxide thickness reduction, reduced contact size, higher mobility and low band-gap channel materials, etc.) to boost its performance. We illustrated the three 32-bit adder architectures and how each design improves the performance. The final optimized design is able to generate, in parallel, both Cin and $\overline{Cin}$ that leads to a reduction in 38.4% logic depth and a reduction in 38.0% contacted gates as compared with CMOS HP and CMOS LV. The optimized 32-bit adder design leads to a 3.83× (4.18×) lower EDP, 5.60× (51.9×) lower ADP, 53.8× lower (1.65× larger) standby power, 150× (15.4×) lower standby energy, and 1.39× (2.31×) higher throughput as compared with CMOS HP (CMOS LV).

Acknowledgment

This material is based upon work supported by the National Science Foundation under Grant No. 1644592 and under CAREER Award No. 1751064.

References

[1] (2015) International technology roadmap for semiconductors. [Online]. Available: http://www.itrs2.net/

[2] M. M. Shulaker *et al.*, "Carbon nanotube computer," *Nature*, vol. 501, p. 526, Sep 2013.

[3] Q. H. Wang *et al.*, "Electronics and optoelectronics of two-dimensional transition metal dichalcogenides," *Nature Nanotechnology*, vol. 7, p. 699, Nov 2012, review Article.

[4] L. Yu *et al.*, "Graphene/mos2 hybrid technology for large-scale two-dimensional electronics," *Nano Letters*, vol. 14, no. 6, pp. 3055–3063, 2014, pMID: 24810658.

[5] H. Wang *et al.*, "Integrated circuits based on bilayer mos2 transistors," *Nano Letters*, vol. 12, no. 9, pp. 4674–4680, 2012, pMID: 22862813.

[6] G. A. Salvatore *et al.*, "Demonstration of subthrehold swing smaller than 60mv/decade in fe-fet with p(vdf-trfe)/sio2 gate stack," in *2008 IEEE International Electron Devices Meeting*, Dec 2008, pp. 1–4.

[7] A. M. Ionescu *et al.*, "Tunnel field-effect transistors as energy-efficient electronic switches," *Nature*, vol. 479, no. 7373, p. 329–337, 2011.

[8] H. Kroemer, "A proposed class of hetero-junction injection lasers," *Proceedings of the IEEE*, vol. 51, no. 12, pp. 1782–1783, Dec 1963.

[9] Y. M. Banadaki *et al.*, "Scaling effects on static metrics and switching attributes of graphene nanoribbon fet for emerging technology," *IEEE Transactions on Emerging Topics in Computing*, vol. 3, no. 4, pp. 458–469, Dec 2015.

[10] D. E. Nikonov *et al.*, "Benchmarking of beyond-cmos exploratory devices for logic integrated circuits," *IEEE Journal on Exploratory Solid-State Computational Devices and Circuits*, vol. 1, pp. 3–11, Dec 2015.

[11] P. Avouris *et al.*, "Carbon nanotube electronics," *Proceedings of the IEEE*, vol. 91, no. 11, pp. 1772–1784, Nov 2003.

[12] Y.-M. Lin *et al.*, "High-performance carbon nanotube field-effect transistor with tunable polarities," *IEEE Transactions on Nanotechnology*, vol. 4, no. 5, pp. 481–489, Sept 2005.

[13] J. Zhang *et al.*, "Polarity-controllable silicon nanowire transistors with dual threshold voltages," *IEEE Transactions on Electron Devices*, vol. 61, no. 11, pp. 3654–3660, Nov 2014.

[14] M. D. Marchi *et al.*, "Polarity control in double-gate, gate-all-around vertically stacked silicon nanowire fets," in *2012 International Electron Devices Meeting*, Dec 2012, pp. 8.4.1–8.4.4.

[15] J. Zhang *et al.*, "A schottky-barrier silicon finfet with 6.0 mv/dec subthreshold slope over 5 decades of current," in *2014 IEEE International Electron Devices Meeting*, Dec 2014, pp. 13.4.1–13.4.4.

[16] M. H. B. Jamaa *et al.*, "Novel library of logic gates with ambipolar cntfets: Opportunities for multi-level logic synthesis," in *2009 Design, Automation Test in Europe Conference Exhibition*, April 2009, pp. 622–627.

[17] M. Raitza *et al.*, "Exploiting transistor-level reconfiguration to optimize combinational circuits," in *Design, Automation Test in Europe Conference Exhibition (DATE), 2017*, March 2017, pp. 338–343.

[18] J. Zhang *et al.*, "Configurable circuits featuring dual-threshold-voltage design with three-independent-gate silicon nanowire fets," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 61, no. 10, pp. 2851–2861, Oct 2014.

[19] P. E. Gaillardon *et al.*, "Advanced system on a chip design based on controllable-polarity fets," in *2014 Design, Automation Test in Europe Conference Exhibition (DATE)*, March 2014, pp. 1–6.

[20] L. Amarú *et al.*, "Power-gated differential logic style based on double-gate controllable-polarity transistors," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 60, no. 10, pp. 672–676, Oct 2013.

[21] E. Giacomin *et al.*, "Low-power multiplexer designs using three-independent-gate field effect transistors," in *2017 IEEE/ACM International Symposium on Nanoscale Architectures (NANOARCH)*, July 2017, pp. 33–38.

[22] J. Romero-Gonzalez *et al.*, "Bcb evaluation of high-performance and low-leakage three-independent-gate field effect transistors," *IEEE Journal on Exploratory Solid-State Computational Devices and Circuits*, vol. 4, pp. 1–9, 2018.

[23] I. Koren, *Computer arithmetic algorithms*, 2nd ed. A K Peters/CRC Press, 2002.

[24] X. Inc. (2013) 7 series fpgas configurable logic block user guide. [Online]. Available: https://www.xilinx.com/support/documentation /user_guides/ug474_7Series_CLB.pdf

[25] D. Lewis *et al.*, "Architectural enhancements in stratix v^{TM}," in *Proceedings of the ACM/SIGDA International Symposium on Field Programmable Gate Arrays*, ser. FPGA '13. New York, NY, USA: ACM, 2013, pp. 147–156.

[26] M. Nicolaidis, "Carry checking/parity prediction adders and alus," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 11, no. 1, pp. 121–128, Feb 2003.

[27] H. Parandeh-Afshar *et al.*, "Exploiting fast carry-chains of fpgas for designing compressor trees," in *2009 International Conference on Field Programmable Logic and Applications*, Aug 2009, pp. 242–249.

[28] A. Heinzig *et al.*, "Reconfigurable silicon nanowire transistors," *Nano Letters*, vol. 12, no. 1, pp. 119–124, 2012.

[29] S. Nakaharai *et al.*, "Electrostatically reversible polarity of dual-gated graphene transistors," *IEEE Transactions on Nanotechnology*, vol. 13, no. 6, pp. 1039–1043, Nov 2014.

[30] G. V. Resta *et al.*, "Polarity control in wse2 double-gate transistors," *Scientific Reports*, vol. 6, p. 29448, Jul 2016, article.

[31] ——, "Scaling trends and performance evaluation of 2-dimensional polarity-controllable fets," *Scientific Reports*, vol. 7, p. 45556, Mar 2017.

[32] R. M. Y. Ng *et al.*, "Vertically stacked silicon nanowire transistors fabricated by inductive plasma etching and stress-limited oxidation," *IEEE Electron Device Letters*, vol. 30, no. 5, pp. 520–522, May 2009.

[33] N. Singh *et al.*, "Si, sige nanowire devices by top-down technology and their applications," *IEEE Transactions on Electron Devices*, vol. 55, no. 11, pp. 3107–3118, Nov 2008.

[34] D. Sacchetto *et al.*, "Fabrication and characterization of vertically stacked gate-all-around si nanowire fet arrays," in *2009 Proceedings of the European Solid State Device Research Conference*, Sept 2009, pp. 245–248.

[35] S. Bobba *et al.*, "Process/design co-optimization of regular logic tiles for double-gate silicon nanowire transistors," in *2012 IEEE/ACM International Symposium on Nanoscale Architectures (NANOARCH)*, July 2012, pp. 55–60.

[36] K. Bernstein *et al.*, "Device and architecture outlook for beyond cmos switches," *Proceedings of the IEEE*, vol. 98, no. 12, pp. 2169–2184, Dec 2010.

[37] D. E. Nikonov *et al.*, "Overview of beyond-cmos devices and a uniform methodology for their benchmarking," *Proceedings of the IEEE*, vol. 101, no. 12, pp. 2498–2533, Dec 2013.

[38] C. Pan *et al.*, "Beyond-cmos non-boolean logic benchmarking: Insights and future directions," in *Design, Automation Test in Europe Conference Exhibition (DATE), 2017*, March 2017, pp. 133–138.

[39] D. Jang *et al.*, "Device exploration of nanosheet transistors for sub-7-nm technology node," *IEEE Transactions on Electron Devices*, vol. 64, no. 6, pp. 2707–2713, June 2017.

[40] O. Zografos *et al.*, "Novel grid-based power routing scheme for regular controllable-polarity fet arrangements," in *2014 IEEE International Symposium on Circuits and Systems (ISCAS)*, June 2014, pp. 1416–1419.

[41] ——, "Design and benchmarking of hybrid cmos-spin wave device circuits compared to 10nm cmos," in *2015 IEEE 15th International Conference on Nanotechnology (IEEE-NANO)*, July 2015, pp. 686–689.

[42] P. E. Gaillardon *et al.*, "Vertically-stacked silicon nanowire transistors with controllable polarity: A robustness study," in *2013 14th Latin American Test Workshop - LATW*, April 2013, pp. 1–6.

[43] C. S. Lee *et al.*, "32-bit processor core at 5-nm technology: Analysis of transistor and interconnect impact on vlsi system performance," in *2016 IEEE International Electron Devices Meeting (IEDM)*, Dec 2016, pp. 28.3.1–28.3.4.