Exploiting Switching of Transistors in Digital Electronics for RFID Tag Design

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***Abstract*— A novel RFID tag and a backscattering channel created by switching transistors in digital electronic circuits have been introduced. The proposed RFID tag is highly reconfigurable, can operate at carrier frequencies from 1 to 20 GHz and reach a maximum distance of 2 m. RFID tags with 6 bits and 36 bits were implemented at 5.8 GHz and 17.46 GHz, respectively, providing up to 68.7 billion (2^{36}) combinations of unique IDs.**

I. Introduction

A radio-frequency identification (RFID) system is a wireless automatic identification system [1]–[3]. Applications of RFID include supply-chain management, asset tracking, data exchange, telemetry, access control, etc. There are two main classes of RFID tags: *chip-based*, which use an integrated circuit (IC) chip to store tag information [4], and *chipless*, which use the electromagnetic signature of the all-passive tag substrate to store the information [5]. The RFIDs can also be classified as passive, semi-passive, and active depending on whether the tag uses electromagnetic sources for power and communication, uses battery power for only its IC circuits, or uses battery power for both IC circuits and communication.

This paper proposes an semi-passive RFID tag implemented in a field-programmable gate array (FPGA), which requires neither a tag antenna nor RF front-end circuits. Our proof of concept demonstrates the potentials of enabling backscatter-based mobile applications, e.g., Apple Pay which is currently realized by near-field communication (NFC) chips, **at zero cost** by leveraging FPGA chips that already exist in smartphones, e.g., Apple iPhone 7 and Samsung Galaxy S5 [6].

The proposed RFID is based on a new backscatter channel created by switching activity of transistors in digital electronic circuits, such as microprocessors. The variation between high-state and low-state of transistors' gates changes the radar cross section (RCS) of the circuit and results in a modulated reflected signal. This paper illustrates that the RFID tag can be interrogated at various frequencies between 1 GHz and 20 GHz at distance up to 2 m away from the tag. RFIDs with 6 bits and 36 bits were implemented at 5.8 GHz and 17.46 GHz, respectively, providing abundant number of bits comparable to [5] and flexible bit configuration.

II. RFID Design by Exploiting Switching of Transistors in Digital Electronics

In this section we propose a programmable RFID tag that is based on a new backscatter channel induced by switching transistors in digital electronics. Compared to traditional RFID tags, proposed RFID tag does not require any pre-designed antennas, two-state RF loads (Z_0 and Z_1), and RF front-end circuits, e.g., matching networks, resonant circuits, etc. Fig. 1 (b) shows a block diagram of the proposed RFID. The modulation mechanism of this RFID tag results from switching activity in digital logic, e.g., programmable logic gates and flip-flops inside an FPGA chip. Different patterns of flip-flop toggling and toggling of different numbers of flip-flops change the equivalent impedance of the FPGA chip, and this impedance variation modulates the signal power reflected from the chip. By controlling the activity of the chip's logic and flip-flops, we can transmit information through backscatter modulation.

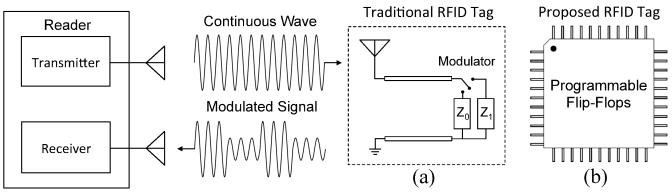


Fig. 1. Comparison between (a) traditional RFID tag and (b) proposed RFID tag.

A simplified internal structure of an FPGA chip is shown in Fig. 2 (a), where logic blocks are arranged in a two-dimensional grid and are connected by a programmable-routing interconnect. This symmetrical grid is connected to I/O blocks which make off-chip connections. Logic blocks can be simplified as programmable flip-flops shown in Fig. 2 (b-1). Most flip flops are based on CMOS-NAND latches due to their low latency. An equivalent output circuit of an CMOS-NAND latches is shown in Fig. 2 (b-2). When input voltage is low, NMOS transistors are off and PMOS transistors are on. A direct path exists between V_{out} and V_{DD}, resulting in a high output state. On the other hand, high input results in a low output state. As shown in Fig. 2 (b-3), there exists a finite resistance between the output and V_{DD} and between the output and the ground, respectively. The switching between NAND logic's high output state (R_1) and low output state (R_0) creates impedance variation, which is analogous to the variation in antenna terminating impedance in typical RFID tags. The

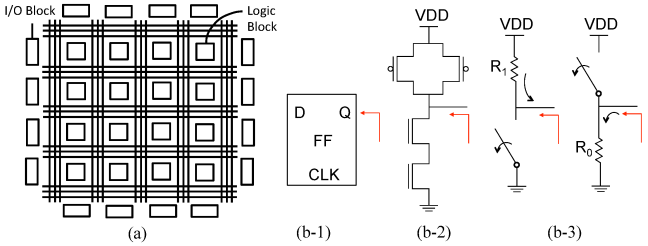
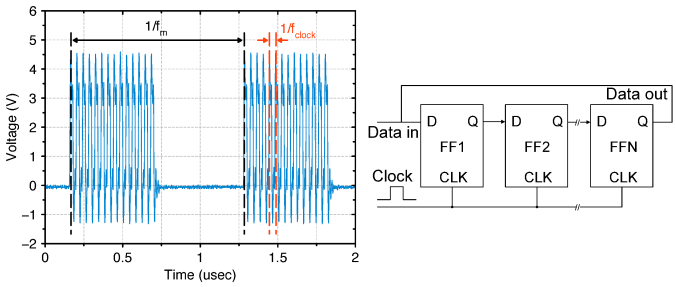


Fig. 2. (a) Simplified internal structure of FPGA; RFID tag circuit model: (b-1) programmable flip-flop, (b-2) equivalent output circuit of a CMOS-NAND latches, (b-3) high-state resistance, R_1 (PMOS on resistance) and low-state resistance, R_0 (NMOS on resistance).

impedance variation creates a difference in the circuit's RCS and thus modulates the electronic backscatter signals.

In order to modulate the electronic backscatter signals, we have programmed flip-flops to switch in a pattern shown in Fig. 3 (a). Flip-flops continuously switch between high state and low state at a clock frequency (f_{clock}) of 50 MHz for half of clock cycle and stay quiet for the other half of the clock cycle. The switching cycle (modulating frequency, f_m) directly relates to the modulated signal bandwidth, i.e., the first harmonic of the modulated backscatter signal will be located at $f_{carrier} \pm f_m$. By changing f_m, we can easily upshift or downshift the modulated signals, making design very flexible.



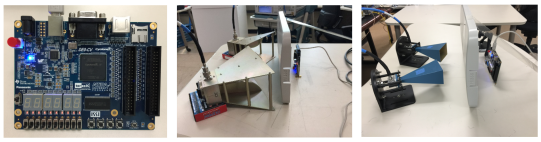
(a) (b)

Fig. 3. (a) Flip-flops switching signal pattern at f_m=900 kHz; (b) Simplified building block of an N-bit shift register.

In addition to the switching pattern, the number of simultaneously-switched elements is another factor that affects electronic backscatter modulation. The more flip-flops are switching in unison, the stronger the backscatter signal is. To control the number of elements that switch simultaneously, we use an N-bit shift register, where N can be used to control the number of simultaneously-toggled flip-flops. Fig. 3 (b) shows a simplified schematic for a 3-bit shift register, created by connecting N=3 flip-flops (FFs). To generate multiple bits as demonstrated in Section IV, we use multiple shift registers to switch at different modulating frequencies (f_m).

III. Measurement Setup

An Agilent MXG N5183A Signal Generator with input power of 15 dBm is used as a signal source and an Agilent MXA N9020A Vector Signal Analyzer is used to record the signals. An Altera DE0-Cyclone V FPGA board is used as the RFID tag as shown in Fig. 4 (a). Double ridge horn antennas (Com-Power AH-118) in Fig. 4 (b) operating from 0.7 GHz to 18 GHz with average isotropic gain of 10 dBi and WR-62 standard gain horn antennas (PE9854/SF-20) in Fig. 4 (c) operating from 12.4 GHz to 18 GHz with average isotropic gain of 20 dBi are used as Tx and Rx for the measurements.

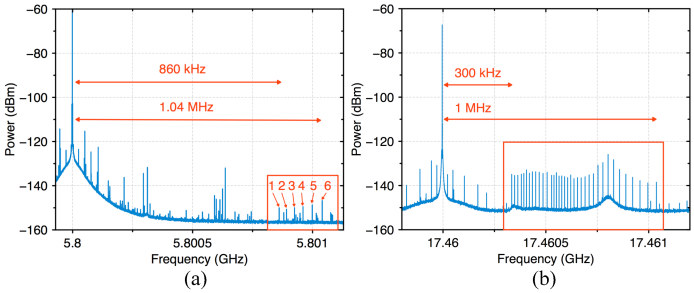


(a) (b) (c)

Fig. 4. (a) Altera Cyclone V FPGA board; measurement setup for the (b) 6 bits RFID at 5.8 GHz and the (c) 36 bits RFID at 17.46 GHz.

IV. Applications: 6 Bits and 36 Bits RFIDs

We demonstrate two possible implementations of the RFID tag by just changing the interrogation frequency. One example is 5.8 GHz 6 bits RFID tag implemented in the bands typically used for RFID communications. The second example is exploration of mm-wave RFID at the 17.46 GHz with 36 bits. Measurement results of the 5.8 GHz 6 bits and the 17.46 GHz 36 bits RFID tags at a distance of 20 cm are presented in Figs. 5 (a) and (b), respectively. **Note that conductive traces on an FPGA board that connect the FPGA chip to GPIO pins may act as antennas and radiate the backscatter signal. In order to minimize impact of other board elements, all GPIO pins are disconnected from the FPGA processor during logic synthesis such that no current flows in the traces**. Results show that the 6 bits RFID tag works at the licensed RFID frequency band at 5.8 GHz with SNRs higher than 5 dB (from 5 dB to 10 dB). The 36 bits RFID tag achieves SNRs higher than 12 dB (from 12 dB to 20 dB) with sidebands separated at least 15 kHz apart, which provides sufficient margins for bit detection. After sweeping across interrogation frequencies between 1 GHz and 20 GHz, it has been found that frequency range between 17 and 18 GHz provides the strongest SNR and maximum distance can reach up to 2 m. Note that a 3-mm thick plastic case is placed between the Tx/Rx and the FPGA board to demonstrate that the proposed RFID tag can be potentially integrated into electronic devices with plastic enclosures.



(a) (b)

Fig. 5. Measurement results of the (a) 5.8 GHz 6 bits RFID and the (b) 17.46 GHz 36 bits RFID.

V. Conclusions

A novel RFID tag and a backscattering channel created by switching transistors in digital electronic circuits have been introduced. The proposed RFID tag is highly reconfigurable, can operate at carrier frequencies from 1 to 20 GHz and reach a maximum distance of 2 m. RFID tags with 6 bits and 36 bits were implemented at 5.8 GHz and 17.46 GHz, respectively, providing up to 68.7 billion (2^{36}) combinations of unique IDs.

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