Wideband Full-Duplex Wireless via Frequency-Domain Equalization: Design and Experimentation

Tingjun Chen†, Mahmood Baraani Dastjerdi†, Jin Zhou‡, Harish Krishnaswamy†, Gil Zussman†
†Electrical Engineering, Columbia University
‡Electrical and Computer Engineering, University of Illinois at Urbana-Champaign
{tingjun@ee, b.mahmood, harish@ee, gil@ee}.columbia.edu, jinzhou@illinois.edu

ABSTRACT

Full-duplex (FD) wireless can signicantly enhance spectrum eciency but requires tremendous amount of self-interference (SI) cancellation. Recent advances in the RFIC community enabled wideband RF SI cancellation (SIC) in *integrated circuits (ICs)* via frequency-domain equalization (FDE), where RF lters channelize the SI signal path. Un- like other FD implementations, that mostly rely on delay lines, FDE-based cancellers *can be realized in small-form- factor devices*. However, the fundamental limits and higher layer challenges associated with these cancellers were not explored yet. Therefore, and in order to support the integra- tion with a software-dened radio (SDR) and to facilitate experimentation in a testbed with several nodes, we design and implement an FDE-based RF canceller on a printed cir- cuit board (PCB). We derive and experimentally validate the PCB canceller model and present a canceller congu- ration scheme based on an optimization problem. We then extensively evaluate the performance of the FDE-based FD radio in the SDR testbed. Experiments show that it achieves 95 dB overall SIC (52 dB from RF SIC) across 20 MHz bandwidth, and an average link-level FD gain of 1.87×. We also conduct experiments in: (i) uplink-downlink networks with inter-user interference, and (ii) heterogeneous networks with half-duplex and FD users. The experimental FD gains in the two types of networks conrm previous analytical results. They depend on the users' SNR values and the number of FD users, and are 1.14×–1.25× and 1.25×–1.73×, respectively. Finally, we numerically evaluate and compare the RFIC and PCB implementations and study various design tradeos.

CCS CONCEPTS

• **Networks** → **Network architectures**; *Wireless access networks*; • **Hardware** → *Wireless devices*; *Radio frequency and wireless circuits*.

KEYWORDS

Full-duplex wireless; frequency-domain equalization; wideband self-interference cancellation; software-dened radios

ACM Reference Format:
Tingjun Chen, Mahmood Baraani Dastjerdi, Jin Zhou, Harish Krishnaswamy, Gil Zussman. 2019. Wideband Full-Duplex Wireless via Frequency-Domain Equalization: Design and Experimentation. In *The 25th Annual International Conference on Mobile Computing and Networking (MobiCom '19), October 21–25, 2019, Los Cabos, Mexico.* ACM, New York, NY, USA, 16 pages. https://doi.org/10.1145/3300061.3300138

1 INTRODUCTION

Full-duplex (FD) wireless – simultaneous transmission and reception on the same frequency channel – can signicantly improve spectrum eciency at the physical (PHY) layer and provide many other benets at the higher layers [35, 41]. The main challenge associated with FD is the extremely strong self-interference (SI) signal that needs to be suppressed, re- quiring 90–110 dB of SI cancellation (SIC).

Recent work leveraging o-the-shelf components and software-dened radios (SDRs) has established the feasibility of FD wireless through SI suppression at the antenna interface, and SIC in analog/RF and digital domains [12, 20, 25, 32, 34]. However, RF cancellers achieving wideband SIC (e.g., [12, 34]) rely on transmission-line delays, which cannot be realized in small-form-factor nodes and/or inte- grated circuits (ICs) due to the required length for generating nanosecond-scale time delays and the lossy nature of the silicon substrate.[1]

[1]For instance, obtaining a nanosecond delay in silicon typically requires a 15 cm-long delay line.

ACM ISBN 978-1-4503-6169-9/19/10…$15.00
https://doi.org/10.1145/3300061.3300138

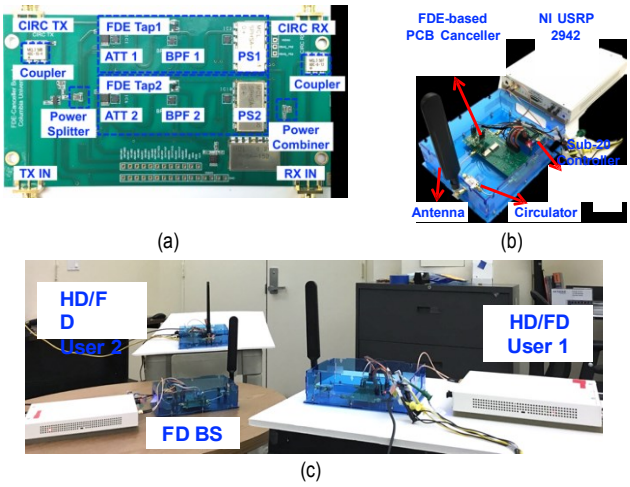


Figure 1: **(a) The frequency-domain equalization- (FDE-) based wideband RF canceller implemented using discrete components on a PCB, (b) the implemented FDE-based FD radio, and (c) the experimental testbed consisting of an FD base station (BS) and 2 users that can operate in either half-duplex (HD) or FD mode.**

A *compact IC-based* design is necessary for supporting FD in hand-held devices (e.g., handsets and tablets) [35, 44, 49, 50]. Specically, recent advances in the RFIC community allowed achieving wideband RF SIC in IC implementations based on the technique of frequency-domain equalization (FDE) [49]. In contrast to the delay line-based approaches (which are essentially performing time-domain equalization), the FDE-based RF canceller utilizes tunable, recongurable, high quality factor 2nd-order bandpass lters (BPFs) with amplitude and phase controls to emulate the frequency- selective antenna interface. In general, tunable, high quality factor BPFs are perhaps as hard to implement on an IC as nanosecond-scale delay lines. However, N -path lters repre- sent an exciting advance that has enabled their implementa- tion in nanoscale CMOS over the past few years [27, 40].

While major advances have been made at the IC level, existing work (e.g., [49]) has several limitations: (i) the fundamental limits of the achievable RF SIC based on the technique of FDE have not been fully understood, (ii) conguration schemes for this new type of RF canceller need to be devel- oped in order to achieve optimized and adaptive RF SIC in real-world environments, and (iii) the system-level perfor- mance of such IC-based FD radios has not been evaluated in dierent network settings. Therefore, in this paper we focus on FDE-based RF cancellers.

Since interfacing an RFIC canceller to an SDR presents numerous technical challenges, we design and implement an FDE-based RF canceller using discrete components on a printed circuit board (PCB). This canceller appears in Fig. 1(a) (we refer to it as the *PCB canceller*) and it emulates its RFIC counterpart.[2] This FDE-based PCB canceller facilitates the evaluation of the canceller conguration scheme and the experimentation using SDRs in a network with multiple FD nodes. Moreover, the PCB canceller is more robust and stable than its IC counterpart and as such can be integrated in the future in the open-access ORBIT [1] and COSMOS [3, 46] testbeds to allow the community to experiment with wideband compact FD wireless. For example, our previous *narrowband* RF canceller emulating its RFIC counterpart [48] is implemented on a PCB and is integrated in the ORBIT testbed [2, 17].

We present a realistic model of the PCB canceller. We then present its conguration scheme based on an optimization problem, which allows ecient adaption of the canceller to environmental changes. The PCB canceller model is experimentally validated and is shown to have high accuracy. We implement an FDE-based FD radio by integrating the PCB canceller with an NI USRP SDR, as depicted in Fig. 1(b).[3] This FD radio achieves 95 dB overall SIC across 20 MHz real-time bandwidth, enabling an FD link budget of 10 dBm average TX power level and -85 dBm RX noise oor. In particular, 52 dB RF SIC is achieved, from which 20 dB is obtained from the antenna interface isolation.

We also evaluate the performance and robustness of the FDE-based FD radio at the link-level in terms of packet reception ratio (PRR) and FD throughput gain, in both line-of-sight (LOS) and non-line-of-sight (NLOS) settings. The results show that the FDE-based FD radio achieves an average FD link throughput gain of 1.85→–1.91→. Moreover, the link SNR dierence when the radio operates in half-duplex (HD) and FD modes is less than 1 dB.

Using our testbed (see Fig. 1(c)), we extensively evaluate the network-level FD gain and conrm analytical results in two types of networks: (i) *UL-DL networks* consisting of one FD base station (BS) and two half-duplex (HD) users with inter-user interference (IUI), and (ii) *heterogeneous HD-FD networks* consisting of one FD BS and co-existing HD and FD users. For UL-DL networks, we show experimentally that the throughput gain is between 1.14→–1.25→ compared to 1.22→–1.3→ predicted by analysis. We discuss the relationship between the FD gain and UL and DL SNR values, as well as the IUI levels. For heterogeneous HD-FD networks, we demonstrate via experiments the impact of dierent user SNR values and the number of FD users on the FD gain. For example, in a 4-node network consisting of an FD BS and 3 users with various user locations and SNR values, median experimental FD gains of 1.25→ and 1.52→ can be achieved when one and two users become FD-capable, respectively.

To the best of our knowledge, this is the rst experimental study of FD gains in such networks using a testbed composed of both HD and FD radios. The results demonstrate

[2]The PCB canceller design is available at [4].

[3]A preliminary version of the system was demonstrated in [19].

the practicality and performance of FDE-based FD radios, which are suitable for small-form-factor devices. The results can also serve as building blocks for developing higher layer (e.g., MAC) protocols.

Finally, we numerically evaluate the FDE-based cancellers based on measurements and validated canceller models. We compute achievable RF SIC under practical constraints and discuss various canceller design tradeos. We also compare the performance of the RFIC and PCB cancellers. We show that our optimized canceller conguration scheme achives an order of magnitude higher RF SIC than the heuristic scheme used in the RFIC canceller [49].

To summarize, the main contributions of the paper are:

1. We present the design, implementation, modeling, and validation of the FDE-based PCB canceller, as well as an optimized canceller conguration scheme;
2. We experimentally evaluate the performance of our FDE-based FD radio with the PCB canceller and the optimized canceller conguration, including the achieved overall SIC and link-level FD gain;
3. We experimentally evaluate the FD throughput gain in various network settings with dierent user capabilities (i.e., HD or FD) and user SNR values.

The rest of the paper is organized as follows. Section 2 reviews related work. In Section 3, we present the problem formulation and RF canceller designs. We present the design, implementation, and model of the FDE-based PCB canceller, as well as the optimized canceller conguration scheme in Section 4. The canceller model is experimentally validated in Section 5. The performance of the FDE-based FD radio is experimentally evaluated in Sections 6. In Section 7, we numerically evaluate the FDE-based cancellers, and compare the RFIC and PCB implementations. We conclude and discuss future directions in Section 8.

2 RELATED WORK

Extensive research related to FD wireless is summarized in [41], including implementations of FD radios and systems, analysis of rate gains, and resource allocation at the higher layers. Below, we briey review the related work.

RF Canceller and FD Radio Designs. RF SIC typically involves two stages: (i) isolation at the antenna interface, and (ii) SIC in the RF domain using cancellation circuitry. While a separate TX/RX antenna pair can provide good isolation and can be used to achieve cancellation [6, 8, 20, 31, 32, 39], a shared antenna interface such as a circulator is more appropriate for single-antenna implementations [12, 23] and is compatible with FD MIMO systems. Existing designs of analog/RF SIC circuitry are mostly based on a time-domain interpolation approach [12, 34]. In particular, real delay lines

Table 1: **Nomenclature**

$\|z\|, \angle z$	Amplitude and phase of a complex value $z = x + jy$ ($x, y \in \mathbb{R}$), where $\|z\| = \sqrt{x^2 + y^2}$ and $\angle z = \tan^{-1}\frac{y}{x}$
B	Total wireless bandwidth/desired RF SIC bandwidth
K, k	Total number of frequency channels and channel index
f_k	Center frequency of the k^{th} frequency channel
M	Number of FDE taps in an FDE-based RF canceller
$H_{\text{SI}}(f_k)$	Frequency response of the antenna interface
$H^{\text{P}}(f_k)$	Frequency response of the FDE-based PCB canceller
$H^{\text{P}}_i(f_k)$	Frequency response of the i^{th} FDE tap in the PCB canceller
$A^{\text{P}}_i, \phi^{\text{P}}_i$	Amplitude and phase controls of the i^{th} FDE tap in the PCB canceller
$C_{\text{E},i}, C_{\text{Q},i}$	Digitally tunable capacitors that control the center frequency and quality factor of the i^{th} FDE tap in the PCB canceller

with dierent lengths and amplitude weighting [12] and phase controls [34] are used and their congurations are optimized to best emulate the SI channel. This essentially represents an RF implementation of a nite impulse response (FIR) lter. Based on the same RF SIC approach, several FD MIMO radio designs are presented [8, 10, 14, 22]. FD relays have also been successfully demonstrated in [11, 13, 15, 29]. Moreover, SIC can be achieved via digital/analog beamforming in FD massive-antenna systems [7, 26]. The techniques utilized in these works are incompatible with IC implementations, which are required for small-form-factor devices. In this paper, we focus on an FDE-based canceller, which builds on our previous work towards the design of such an RFIC canceller [49]. However, existing IC-based FD radios (e.g., [49]) have not been evaluated at the system-level in dierent network settings.

FD Gain at the Link- and Network-level. At the higher layers, recent work focuses on characterizing the capacity region and rate gains, as well as developing resource allocation algorithms under both perfect [5, 9] and imperfect SIC [24, 28, 37]. Similar problems are considered in FD multi-antenna/MIMO systems [26, 38, 47]. Medium access control (MAC) algorithms are studied in networks with all HD users [16, 21] or with heterogeneous HD and FD users [18]. Moreover, network-level FD gain is analyzed in [39, 42, 43, 45] and experimentally evaluated in [31, 33] where all the users are HD or FD. Finally, [30] proposes a scheme to suppress IUI using an emulated FD radio.

To the best of our knowledge, this is *the rst thorough study of wideband RF SIC achieved via a frequency-domain-based approach (which is suitable for compact implementations) that is grounded in real-world implementation and includes extensive system- and network-level experimentation*.

3 BACKGROUND AND FORMULATION

In this section, we review concepts related to FD wireless and RF canceller conguration optimization. We also present dierent RF canceller designs and specicaully the design of

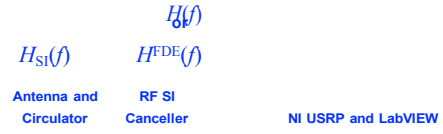


Figure 2: **Block diagram of an FD radio.**

the FDE-based RF canceller. Summary of the main notation is provided in Table 1.

3.1 FD Background and Notation

Fig. 2 shows the block diagram of a single-antenna FD radio using a circulator at the antenna interface. Due to the extremely strong SI power level and the limited dynamic range of the analog-to-digital converter (ADC) at the RX, a total amount of 90–110 dB SIC must be achieved across the antenna, RF, and digital domains. Specically, (i) SI suppres- sion is rst performed at the antenna interface, (ii) an RF SI canceller then taps a reference signal at the output of the TX power amplier (PA) and performs SIC at the input of the low-noise amplier (LNA) at the RX, and (iii) a digital SI canceller further suppresses the residual SI.

Consider a wireless bandwidth of B that is divided into K orthogonal frequency channels. The channels are indexed by $k \in \{1, \ldots, K\}$ and denote the center frequency of the k^{th} channel by f_k.[4] We denote the antenna interface response by $H_{SI}(f_k)$ with amplitude $|H_{SI}(f_k)|$ and phase $\angle H_{SI}(f_k)$. Note that the actual SI channel includes the TX-RX leakage from the antenna interface as well as the TX and RX transfer functions at the baseband from the perspective of the digital canceller. Since the paper focuses on achieving wideband RF SIC, we use $H_{SI}(f_k)$ to denote the antenna interface response and also refer to it as the *SI channel*. We refer to *TX/RX isolation* as the ratio (in dB, usually a negative value) between the residual SI power at the RX input and the TX output power, which includes the amount of TX/RX isolation achieved by both the antenna interface and the RF canceller/circuitry. We then refer to *RF SIC* as the absolute value of the TX/RX isolation. We also refer to *overall SIC* as the total amount of SIC achieved in both the RF and digital domains. The antenna interface used in our experiments typically provides a TX/RX isolation of around -20 dB.

3.2 Problem Formulation

Ideally, an RF canceller is designed to best emulate the antenna interface, $H_{SI}(f_k)$, across a desired bandwidth, $B = [f_1, f_K]$. We denote by $H(f_k)$ the frequency response of an RF canceller and by $H_{res}(f_k) := H_{SI}(f_k) - H(f_k)$ the *residual SI channel response*. The optimized RF canceller conguration is obtained by solving (P1):

$$\text{(P1) min:} \sum_{k=1}^{K} |H_{res}(f_k)|^2 = \sum_{k=1}^{K} |H_{SI}(f_k) - H(f_k)|^2$$

s.t.: constraints on conguration parameters of $H(f_k)$, $\forall k$.

The RF canceller conguration obtained by solving (P1) minimizes the residual SI power referred to the TX output. As described in Section 1, one main challenge associated with the design of the RF canceller with response $H(f_k)$ to achieve wideband SIC is due to the highly frequency- selective antenna interface, $H_{SI}(f_k)$. Moreover, an ecient RF canceller conguration scheme needs to be designed so that the canceller can adapt to time-varying $H_{SI}(f_k)$.

3.3 RF Canceller Designs

Delay Line-based RF Cancellers. An RF canceller design introduced in [12] involves using M delay line taps. Specically, the i^{th} tap is associated with a time delay of r_i, which is *pre-selected* and *xed* depending on the selected circu- lator and antenna, and an amplitude control of A_i. Since the Fourier transform of a delay of r_i is $e^{-2\pi f r_i}$, an M-tap delay line-based RF canceller has a frequency response of $H^{DL}(f_k) = \sum_{i=1}^{M} A_i e^{-j2\pi f_k r_i}$. The congurations of the amplitude controls, $\{A_i\}$, are obtained by solving (P1) with $H(f_k) = H^{DL}(f_k)$. In [12], an RF canceller of $M = 16$ delay line taps is implemented. In [34], a similar approach is considered with $M = 3$ and an additional phase control, ϕ_i, on each tap, resulting in an RF canceller model of $H^{DL}(f_k) = \sum_{i=1}^{3} A_i e^{-j(2\pi f_k r_i + i\phi_i)}$. As mentioned in Section 1, although such cancellers can achieve wideband SIC, this approach is more suitable for large-form-factor nodes than for compact/small-form-factor implementations.

Amplitude- and Phase-based RF Cancellers. A compact design that is based on an amplitude- and phase-based RF canceller realized in an RFIC implementation is presented in [48]. This canceller has a single-tap with one amplitude and frequency control, (A_0, ϕ_0), which can emulate the antenna interface, $H_{SI}(f_k)$, at *only one* given cancellation frequency f_1 by setting $A_0 = |H_{SI}(f_1)|$ and $\phi_0 = \angle H_{SI}(f_1)$. The same design is also realized using discrete components on a PCB (without using any length delay lines), and is integrated in the ORBIT testbed for open-access FD research [17]. However, this type of RF cancellers has limited RF SIC perfromacne and bandwidth, since it can only emulate the antenna interface at a single frequency.

An FDE-based RF Canceller. One compact design to achieve signicantly enhanced performance and bandwidth of RF

[4] We use discrete frequency values $\{f_k\}$ since in practical systems, the antenna interface response is measured at discrete points (e.g., per OFDM subcarrier). However, the presented model can also be applied to cases with continuous frequency values.

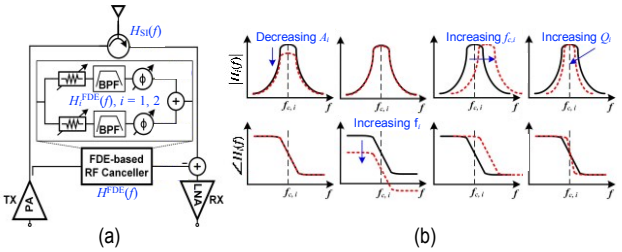


Figure 3: **(a) Block diagram of an FDE-based RF canceller with M = 2 FDE taps, and (b) illustration of amplitude and phase responses of an ideal 2nd-order BPF with amplitude, phase, center frequency, and quality factor (i.e., group delay) controls.**

SIC is based on the technique of frequency-domain equalization (FDE) and was implemented in an RFIC [49]. Fig. 3(a) shows the diagram of an FDE-based canceller, where parallel recongurable bandpass lters (BPFs) are used to emulate the antenna interface response across wide bandwidth. We denote the frequency response of a general FDE-based RF canceller consisting of M FDE taps by

$$H^{\text{FDE}}(f_k) = \sum_{i=1}^{M} H_i^{\text{FDE}}(f_k), \tag{1}$$

where $H_i^{\text{FDE}}(f_k)$ is the frequency response of the i^{th} FDE tap containing a recongurable BPF with amplitude and phase controls. Theoretically, any m^{th}-order RF BPF ($m = 1, 2, \ldots$) can be used. Fig. 3(b) illustrates the amplitude and phase of a 2nd-order BPF with dierent control parameters. For example, increased BPF quality factors result in "sharper" BPF ampli- tudes and increased group delay. Since it is shown [27, 49] that a 2nd-order BPF can accurately model the FDE N-path
lter, the frequency response of an FDE-based RFIC canceller with M FDE taps is given by

$$H^{\text{I}}(f_k) = \sum_{i=1}^{M} H_i^{\text{I}}(f_k) = \sum_{i=1}^{M} \frac{A_i^{\text{I}} \cdot e^{-j i f_i^{\text{I}}}}{1 - jQ_i \cdot \left(f_{c,i}/f_k - f_k/f_{c,i} \right)}. \tag{2}$$

Within the i^{th} FDE tap, $H_i^{\text{I}}(f_k)$, A_i^{I} and ϕ_i^{I} are the amplitude and phase controls, and $f_{c,i}$ and Q_i are the center frequency and quality factor of the 2nd-order BPF (see Fig. 3(b)). In the RFIC canceller, $f_{c,i}$ and Q_i are adjusted through a recongurable baseband capacitor and transconductors, respectively. As Fig. 3(b) and (2) suggest, one FDE tap features four de- grees of freedom (DoF) so that the antenna interface, $H_{SI}(f_k)$, can be emulated *not only in amplitude and phase, but also in the slope of amplitude and the slope of phase (i.e., group delay)*. Therefore, the RF SIC bandwidth can be signicantly enhanced through FDE when compared with the amplitude- and phased-based RF cancellers.

4 DESIGN AND OPTIMIZATION

In this section, we present our design and implementation of an FDE-based canceller using discrete components on a PCB (referred to as the *PCB canceller*). Recall that the motivation is to facilitate integration with an SDR platform, the experimentation of FD at the link/network level, and integration with open-access wireless testbeds. We then present a realistic PCB canceller model, which is later validated (Section 5) and used in the experimental and numerical evaluations (Sections 6 and 7).

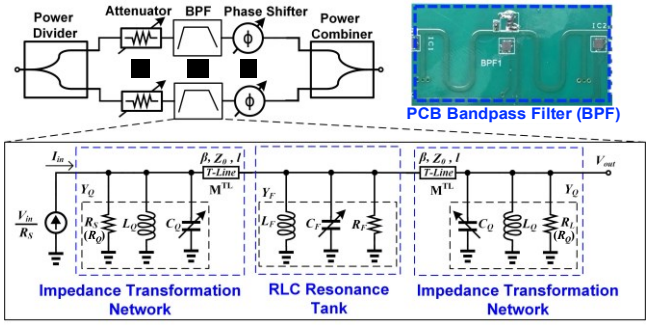


Figure 4: **Block diagram of the implemented M = 2 FDE taps in the PCB canceller (see Fig. 3(a)), each of which consists of an RLC bandpass lter (BPF), an attenuator for amplitude control, and a phase shifter for phase control.**

4.1 FDE PCB Canceller Implementation

Fig. 1(a) and Fig. 3(a) show the implementation and block diagram of the PCB canceller with 2 FDE taps. In particular, a reference signal is tapped from the TX input using a coupler and is split into two FDE taps through a power divider. Then, the signals after each FDE tap are combined and RF SIC is performed at the RX input. Each FDE tap consists of a recongurable 2nd-order BPF, as well as an attenuator and phase shifter for amplitude and phase controls. We refer to
the BPF here as the *PCB BPF* to distinguish from the one in the RFIC canceller (2). The PCB BPF (with size of 1.5 cm ⇥ 4 cm, see Fig. 4) is implemented as an RLC lter with impedance transformation networks and is optimized around 900 MHz operating frequency.[5] When compared to the N-path lter used in the RFIC canceller [49] that consumes certain amount of DC power, this discrete component-based passive RLC BPF has zero DC power consumption and can support higher TX power levels. Moreover, it has a lower noise level than the RFIC implementation.

The PCB BPF center frequency in the i^{th} FDE tap can be adjusted through the capacitor, $C_{F,i}$, in the RLC resonance tank. In order to achieve a high and adjustable BPF quality factor, impedance transformation networks including transmission-lines (T-Lines) and digitally tunable capacitors, $C_{Q,i}$, are introduced. In our implementation, $C_{F,i}$ consists of two parallel

[5]We select 900 MHz around the Region 2 902–928 MHz ISM band as the operating frequency but the approach can be easily extended to other bands (e.g., 2.4 GHz) with slight modication of the hardware design and proper choice of the frequency-dependent components.

capacitors: a xed 8.2 pF capacitor and a Peregrine Semiconductor PE64909 digitally tunable capacitor (4-bit) with a resolution of 0.12 pF. For $C_{Q,i}$, we use the Peregrine Semi-
conductor PE64102 digitally tunable capacitor (5-bit) with a resolution of 0.39 pF. In addition, the programmable attenuator has a tuning range of 0–15.5 dB with a 0.5 dB resolution, and the passive phase shifter is controlled by a 8-bit digital-to-analog converter (DAC) and covers full 360° range.

4.2 FDE PCB Canceller Model

Ideally, the PCB BPF has a 2nd-order frequency response from the RLC resonance tank. However, in practical implementation, its response deviates from that used in the FDE-based RFIC canceller (2). Therefore, there is a need for a valid model tailored for evaluating the performance and optimized conguration of the PCB canceller. Based on the circuit diagram in Fig. 4, we derive a realistic model for the frequency response of the PCB BPF, $H_i^{\mathrm{B}}(f_k)$, given by[6]

$$\begin{aligned} H^{\mathrm{B}}_i(f_k) = & R_s \Big(j\sin(2f3l)Z_0 Y_{\mathrm{F},i}(f_k) Y_{\mathrm{Q},i}(f_k) \\ & + \cos^2(f3l) Y_{\mathrm{F},i}(f_k) + 2\cos(2f3l) Y_{\mathrm{Q},i}(f_k) \\ & + j\sin(2f3l)/Z_0 + 0.5j\sin(2f3l) Z_0 (Y_{\mathrm{Q},i}(f_k))^2 \\ & - \sin^2(f3l) Z_0^2 Y_{\mathrm{F},i}(f_k) (Y_{\mathrm{Q},i}(f_k))^2 \Big)^{-1}, \end{aligned} \tag{3}$$

where $Y_{\mathrm{F},i}(f_k)$ and $Y_{\mathrm{Q},i}(f_k)$ are the admittance of the RLC resonance tank and impedance transformation networks, i.e.,

$$\begin{aligned} Y_{\mathrm{F},i}(f_k) &= 1/R_{\mathrm{F}} + j2\pi C_{\mathrm{F},i} f_k + 1/(j2\pi L_{\mathrm{F}} f_k), \\ Y_{\mathrm{Q},i}(f_k) &= 1/R_{\mathrm{Q}} + j2\pi C_{\mathrm{Q},i} f_k + 1/(j2\pi L_{\mathrm{Q}} f_k). \end{aligned} \tag{4}$$

In particular, to have perfect matching with the source and load impedance of the RLC resonance tank, R_{S} and R_{L} are set to be the same value of $R_{\mathrm{Q}} = 50\,\Omega$ (see Fig. 4). $f3$ and Z_0 are the wavenumber and characteristic impedance of the T-Line with length l (see Fig. 4). In our implementation, L_{F} = 1.65 nH, L_{Q} = 2.85 nH, $f3l \approx 1.37$ rad, and $Z_0 = 50\,\Omega$.

In addition, other components in the PCB canceller (e.g., couplers and power divider/combiner) can introduce extra attenuation and group delay, due to implementation losses. Based on the S-Parameters of the components and measurements, we observed that the attenuation and group delay introduced, denoted by A_0^{P} and τ_0^{P}, are constant across frequency in the desired bandwidth. Hence, we empirically set A_0 = -4.1 dB and τ_0 = 4.2 ns. Recall that each FDE tap is also associated with amplitude and phase controls, A_i^{P} and ϕ_i^{P}, the PCB canceller with two FDE taps is modeled by

$$H^{\mathrm{P}}(f_k) = A_0^{\mathrm{P}} e^{-j2\pi f_k \tau_0^{\mathrm{P}}} \Big(\sum_{i=1}^{2} A_i^{\mathrm{P}} e^{-j\phi_i^{\mathrm{P}}} H_i^{\mathrm{B}}(f_k) \Big), \tag{5}$$

where $H_i^{\mathrm{B}}(f_k)$ is the PCB BPF model given by (3). As a result, the i^{th} FDE tap in the PCB canceller (5) has conguration parameters $\{A_i^{\mathrm{P}}, \phi_i^{\mathrm{P}}, C_{\mathrm{F},i}, C_{\mathrm{Q},i}\}$, featuring 4 DoF.

4.3 Optimization of Canceller Conguration

Based on (P1), we now present a general FDE-based canceller conguration scheme that jointly optimizes all the FDE taps in the canceller.[7] Although our implemented PCB canceller has only 2 FDE taps, both its model and the conguration scheme can be easily extended to the case with a larger number of FDE taps, as described in Section 7.

The inputs to the FDE-based canceller conguration scheme are: (i) the PCB canceller model (5) with given num- ber of FDE taps, M, (ii) the antenna interface response, $H_{\mathrm{SI}}(f_k)$, and (iii) the desired RF SIC bandwidth, $f_k \in [f_1, f_K]$. Then, the optimized canceller conguration is obtained by solving (P2).

$$\begin{aligned} (\mathrm{P2}) \ \min: \ & \sum_{k=1}^{K} \left| H^{\mathrm{P}}_{\mathrm{res}}(f_k) \right|^2 = \sum_{k=1}^{K} \left| H_{\mathrm{SI}}(f_k) - H^{\mathrm{P}}(f_k) \right|^2 \\ \text{s.t.:} \ & A_i^{\mathrm{P}} \in [A_{\min}, A_{\max}], \ \phi_i^{\mathrm{P}} \in [-\pi, \pi], \\ & C_{\mathrm{F},i} \in [C_{\mathrm{F,min}}, C_{\mathrm{F,max}}], \ C_{\mathrm{Q},i} \in [C_{\mathrm{Q,min}}, C_{\mathrm{Q,max}}], \ \forall i. \end{aligned}$$

Note that (P2) is challenging to solve due to its non-convexity and non-linearity, as opposed to the linear program used in the delay line-based RF canceller [12]. This is due to the specic forms of the conguration parameters in (5) such as (i) the higher-order terms introduced by f_k, and (ii) the trigonometric term introduced by the phase control, ϕ_i^{P}. In addition, the antenna interface response, $H_{\mathrm{SI}}(f_k)$, is also frequency-selective and time-varying.

In general, it is dicult to maintain analytical tractability of (P2) (i.e., to obtain its optimal solution in closed-form). However, in practice, it is unnecessary to obtain the global optimum to (P2) as long as the performance achieved by the obtained local optimum is sucient (e.g., at least 45 dB RF SIC is achieved). In this work, the local optimal solution to (P2) is obtained using a MATLAB solver. The detailed implementation and performance of the optimized canceller conguration are described in Section 6.2.

5 MODEL VALIDATION

Validation of the PCB BPF. We rst experimentally validate the PCB BPF model, $H_i^{\mathrm{B}}(f_k)$, given by (3). The ground truth is obtained by measuring the frequency response (using S-Parameters measurements) of the PCB BPF using a test structure, which contains only the BPF, to avoid the eects of other components on the PCB. The measurements are conducted

[6] The details can be found in Appendix A.

[7] The RFIC canceller presented in [49] is congured based on heuristics. In Section 7, we show that the optimized conguration scheme can signicantly improve the RFIC canceller performance.

Table 2: **Four (C_F, C_Q) congurations used in the validations.**

	Highest Q-Factor	Lowest Q-Factor
Highest Center Freq.	Set 1: ($C_{F,min}$, $C_{Q,min}$)	Set 3: ($C_{F,min}$, $C_{Q,max}$)
Lowest Center Freq.	Set 2: ($C_{F,max}$, $C_{Q,min}$)	Set 4: ($C_{F,max}$, $C_{Q,max}$)

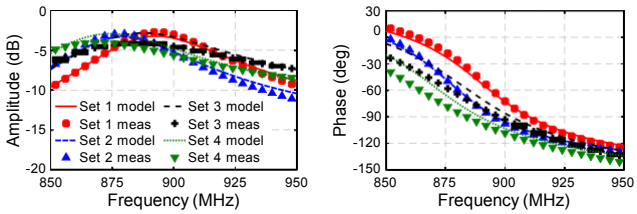


Figure 5: **Modeled and measured amplitude and phase responses of the implemented PCB BPF under dierent (C_F, C_Q) congurations indicated in Table 2.**

with varying (C_F, C_Q) congurations and the result of each conguration is averaged over 20 measurement instances.[8] The BPF center frequency is measured as the frequency with the highest BPF amplitude, and the BPF quality factor is com- puted as the ratio between the center frequency and the 3 dB bandwidth around the center frequency.

The PCB BPF has a *xed* quality factor of 2.7, achieved by using only the RLC resonance tank. By setting $C_Q = C_{Q,max}$ and $C_Q = C_{Q,min}$ (see Section 4.1), the measured lowest and highest achievable BPF quality factors are 9.2 and 17.8, respec- tively. This shows an improvement in the PCB BPF quality

factor tuning range of 3.4⇥–6.6⇥, achieved by introducing the impedance transformation networks. Similarly, by set- ting $C_F = C_{F,max}$ and $C_F = C_{F,min}$, the PCB BPF has a center frequency tuning range of 18 MHz.

Fig. 5 presents the modeled and measured amplitude and phase responses of the PCB BPF with 4 (C_F, C_Q) congura- tions (see Table 2) which cover the entire tuning range of the BPF center frequency and quality factor. The results show that the PCB BPF model (3) matches very closely with the measurements at the highest BPF quality factor value (Sets 1 and 2). In particular, the maximum dierences between the measured and modeled amplitude and phase are 0.5 dB and 7°, respectively. At the lowest BPF quality factor value (Sets 3 and 4), the dierences are 1.2 dB and 15°, thereby show- ing the validity of the PCB BPF model. The same level of accuracy of the PCB BPF model (3) is also observed for other (C_F, C_Q) congurations within their tuning ranges.

Validation of the PCB Canceller. We use the same experi- ments as in the PCB BPF validation to validate the PCB canceller model with 2 FDE taps, $H^P(f_k)$, given by (5). We consider two cases for controlled measurements: (i) only one FDE tap is active, and (ii) both FDE taps are active. Note that the programmable attenuators only have a maximal

[8]We drop the subscript i, since both PCB BPFs behave identically.

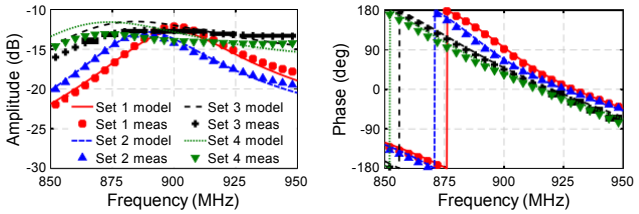


Figure 6: **Modeled and measured amplitude and phase responses of the PCB canceller, where only the rst FDE tap is active, under dif- ferent (C_F, C_Q) congurations indicated in Table 2.**

attenuation of only 15.5 dB (see Section 4.1) and at this max- imal attenuation, signals can still leak through the FDE tap, resulting in inseparable behaviors between the two FDE taps.

To minimize the eect of the second FDE tap, we set the rst FDE tap at its highest amplitude (i.e., lowest attenuation value of A_1^P) with varying values of ($C_{F,1}$, $C_{Q,1}$) while setting the second FDE tap with the lowest amplitude (i.e., highest attenuation value of A_2^P). Fig. 6 shows the modeled and mea- sured amplitude and phase responses of the PCB canceller in this case, i.e., only the rst FDE tap is active. At the high- est BPF quality factor value (Sets 1 and 2), the maximum dierences between the modeled and measured amplitude and phase are 0.9 dB and 8°, respectively. At the lowest BPF quality factor value (Sets 3 and 4), the errors are 1.5 dB and 12°, while still validating the PCB canceller model. We obtain similar results in the case where only the second FDE tap is active by setting highest attenuation value of A^P and low- est attenuation value of A_2^P. The measurements are repeated with dierent $\{A_i^P, \phi_i^P, C_{F,i}, C_{Q,i}\}$ settings for $i = 1, 2$, and all the results demonstrate the same level of accuracy of the PCB canceller model (5).

6 EXPERIMENTAL EVALUATION

In this section, we discuss the integration of the PCB can- celler described in Section 4 with an SDR testbed. Then, we present extensive experimental evaluation of the FDE-based FD radio at the node, link, and network levels.

6.1 Implementation and Testbed

FDE-based FD Radio and the SDR Testbed. Figs. 1(b) and 1(c) depict our FDE-based FD radio design (whose diagram is shown in Fig. 2) and the SDR testbed. A 698–960 MHz swivel blade antenna and a coaxial circulator with operating fre- quency range 860–960 MHz are used as the antenna interface. We use the NI USRP-2942 SDR with the SBX-120 daughter- board operating at 900 MHz carrier frequency, which is the same as the operating frequency of the PCB canceller. As mentioned in Section 4.1, our PCB canceller design can be

easily extended to other operating frequencies. and the antenna interface. The USRP has a measured noise oor of -85 dBm at a xed receiver gain setting.[9]

We implemented a full OFDM-based PHY layer using NI LabVIEW on a host PC.[10] A real-time RF bandwidth of B = 20 MHz is used through our experiments. The baseband complex (IQ) samples are streamed between the USRP and the host PC through a high-speed PCI-Express interface. The OFDM symbol size is 64 samples (subcarriers) with a cyclic-prex ratio of 0.25 (16 samples). Throughout the evaluation, $\{f_k\}_{k=1}^{52}$ is used to represent the center frequency of the 52 non-zero subcarriers. The OFDM PHY layer supports various modulation and coding schemes (MCSs) with constellations from BPSK to 64QAM and coding rates of 1/2, 2/3, and 3/4, resulting in a highest (HD) data rate of 54 Mbps. The digital SIC algorithm with a highest non-linearity order of 7 is also implemented in LabVIEW to further suppress the residual SI signal after RF SIC.[11]

In total, our testbed consists of 3 FDE-based FD radios, whose performance is experimentally evaluated at the node, link, and network levels. Regular USRPs (without the PCB canceller) are also included in scenarios where additional HD users are needed.

Optimized PCB Canceller Configuration. The optimized PCB canceller conguration scheme is implemented on the host PC and the canceller is congured by a SUB-20 controller through the USB interface. For computational eciency, the PCB canceller response (5) (which is validated in Section 5 and is independent of the environment) is pre-computed and stored. The detailed steps of the canceller conguration are as follows.

1. Measure the real-time antenna interface response, $H_{\text{SI}}(f_k)$, using a preamble (2 OFDM symbols) by dividing the received preamble by the known transmitted preamble in the frequency domain;
2. Solve for an initial PCB canceller conguration using optimization (P2) based on the measured $H_{\text{SI}}(f_k)$ and the canceller model (5) (see Section 4.3). The returned cong- uration parameters are rounded to their closest possible values based on hardware resolutions (see Section 4.1);
3. Perform a ner-grained local search and record the optimal canceller conguration (usually ~10 iterations).

[9]This USRP receiver noise oor is limited by the environmental interference at around 900 MHz. The USRP has a true noise oor of around -95 dBm at the same receiver gain setting, when not connected to an antenna.

[10]We consider a general OFDM-based PHY but do not consider the specic frame/packet structure dened by the standards (e.g., LTE or WiFi PHY).

[11]The digital SIC algorithm is based on Volterra series and a least-square problem, which is similar to that presented in [12]. We omit the details here due to limited space.

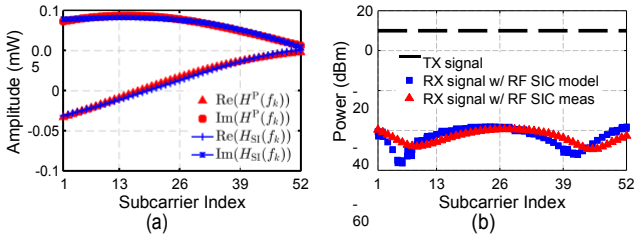


Figure 7: **(a) Real and imaginary parts of the optimized PCB canceller response, $H^{\text{P}}(f_k)$, vs. real-time SI channel measurements, $H_{\text{SI}}(f_k)$, and (b) modeled and measured RX signal power after RF SIC at** 10 dBm **TX power. An average** 52 dB **RF SIC across** 20 MHz **is achieved in the experiments.**

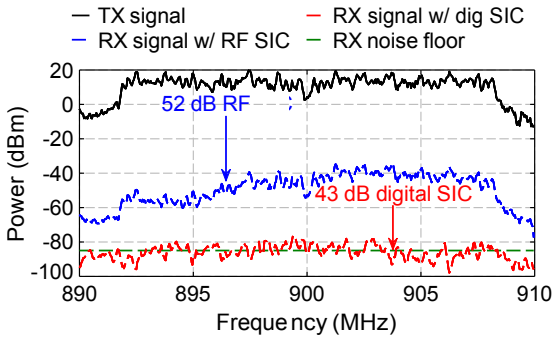


Figure 8: **Power spectrum of the received signal after SIC in the RF and digital domains with** 10 dBm **average TX power,** 20 MHz **bandwidth, and** -85 dBm **receiver noise oor.**

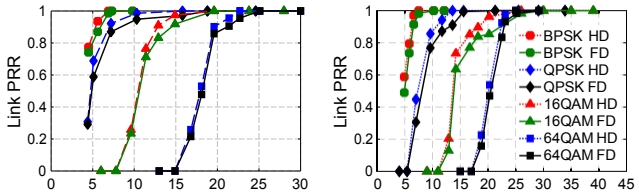
In our design, the optimized PCB canceller conguration can be obtained in less than 10 ms on a regular PC with quad-core Intel i7 CPU via a non-optimized MATLAB solver.[12]

6.2 Node-Level: Microbenchmarks

Optimized PCB Canceller Response and RF SIC. We set up an FDE-based FD radio running the optimized PCB canceller conguration scheme and record the canceller conguration, measured $H_{\text{SI}}(f_k)$, and measured residual SI power after RF SIC. The recorded canceller conguration is then used to compute the PCB canceller response using (5).

Fig. 7(a) shows an example of the optimized PCB canceller response, $H^{\text{P}}(f_k)$, and the measured antenna interface response, $H_{\text{SI}}(f_k)$, in real and imaginary parts (or I and Q). It can be seen that $H^{\text{P}}(f_k)$ closely matches with $H_{\text{SI}}(f_k)$ with maximal amplitude and phase dierences of only 0.5 dB and 2.5°, respectively. This conrms the accuracy of the PCB can- celler model and the performance of the optimized canceller conguration. Fig. 7(b) shows the modeled (computed by subtracting the modeled canceller response from the mea- sured $H_{\text{SI}}(f_k)$) and measured RX signal power after RF SIC at 10 dBm TX power. The results show that the FDE-based

[12]Assuming that the canceller needs to be congured once per second, this is only a 1% overhead. We note that a C-based optimization solver and/or an implementation based on FPGA/look-up table can signicantly improve the performance of the canceller conguration and is left for future work.



(a) **Code rate 1/2** (b) **Code rate 3/4**

Figure 9: **HD and FD link packet reception ratio (PRR) with varying HD link SNR and modulation and coding schemes (MCSs).**

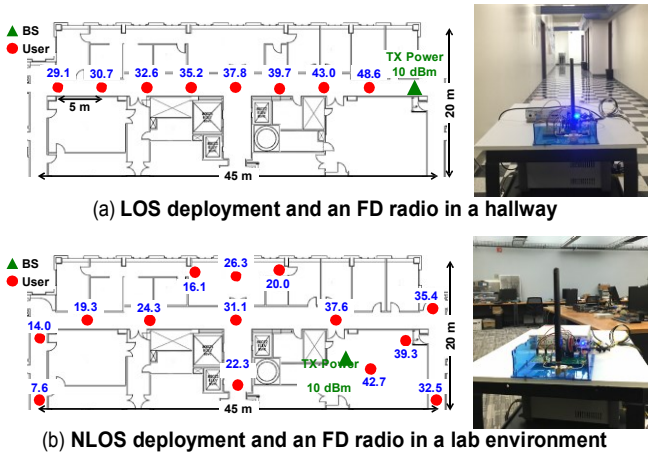
FD radio achieves an average 52 dB RF SIC across 20 MHz bandwidth, from which 20 dB is obtained from the antenna interface isolation. Similar performance is observed in various experiments throughout the experimental evaluation.

Overall SIC. We measure the overall SIC achieved by the FDE-based FD radio including the digital SIC in the same setting as described above, and the results are presented in Fig. 8. It can be seen that the FDE-based FD radio achieves an average 95 dB overall SIC across 20 MHz, from which 52 dB and 43 dB are obtained in the RF and digital domains, respectively. Recall from Section 6.1 that the USRP has noise oor of -85 dBm, the FDE-based RF radio supports a maximal average TX power of 10 dBm (where the peak TX power can go as high as 20 dBm). We use TX power levels lower than or equal to 10 dBm throughout the experiments, where all the SI can be canceled to below the RX noise oor.

6.3 Link-Level: SNR-PRR Relationship

We now evaluate the relationship between link SNR and link packet reception ratio (PRR). We setup up a link with two FDE-based FD radios at a xed distance of 5 meters with equal TX power. In order to evaluate the performance of our FD radios with the existence of the PCB canceller, we set an FD radio to operate in HD mode by turning on only its transmitter or receiver. We conduct the following experiment for each of the 12 MCSs in both FD and HD modes, with varying TX power levels. In particular, the packets are sent over the link simultaneously in FD mode or in alternating directions in HD mode (i.e., the two radios take turns and transmit to each other). In each experiment, both radios send a sequence of 50 OFDM streams, each OFDM stream contains 20 OFDM packets, and each OFDM packet is 800-Byte long.

We consider two metrics. The *HD (resp. FD) link SNR* is measured as the ratio between the average RX signal power in both directions and the RX noise oor when both radios operate in HD (resp. FD) mode. The *HD (resp. FD) link PRR* is computed as the fraction of packets successfully sent over the HD (resp. FD) link in each experiment. We observe from the experiments that the HD and FD link SNR and PRR values in both link directions are similar. Similar experiments and results were presented in [51] for HD links.



(a) **LOS deployment and an FD radio in a hallway**

(b) **NLOS deployment and an FD radio in a lab environment**

Figure 10: **(a) Line-of-sight (LOS), and (b) non-line-of-sight (NLOS) deployments, and the measured HD link SNR values (dB).**

Fig. 9 shows the relationship between link PRR values and HD link SNR values with varying MCSs. The results show that with sucient link SNR values (e.g., 8 dB for BPSK-1/2 and 28 dB for 64QAM-3/4), the FDE-based FD radio achieves a link PRR of 100%. With insucient link SNR values, the average FD link PRR is 6.5% lower than the HD link PRR across varying MCSs. This degradation is caused by the link SNR dierence when the radios operate in HD or FD mode, which is described later in Section 6.4. Since packets are sent simultaneously in both directions on an FD link, this average PRR degradation is equivalent to an average FD link

throughput gain of 1.87→ under the same MCS.

6.4 Link-Level: SNR Dierence and FD Gain

Experimental Setup. To thoroughly evaluate the link level FD throughput gain achieved by our FD radio design, we conduct experiments with two FD radios with 10 dBm TX power, one emulating a base station (BS) and one emulating a user. We consider both line-of-sight (LOS) and non-line-of-sight (NLOS) experiments as shown in Fig. 10. In the LOS setting, the BS is placed at the end of a hallway and the user is moved away from the BS at stepsizes of 5 meters up to a distance of 40 meters. In the NLOS setting, the BS is placed in a lab environment with regular furniture and the user is placed at various locations (oces, labs, and corridors). We place the BS and the users at about the same height across all the experiments.[13] The measured HD link SNR values are also included in Fig. 10. Following the methodology of [12], for each user location, we measure the *link SNR dierence*, which is dened as the absolute dierence between the average HD

[13] In this work, we emulate the BS and users without focusing on specic deployment scenarios. The impacts of dierent antenna heights and user densities, as mentioned in [36], will be considered in future work.

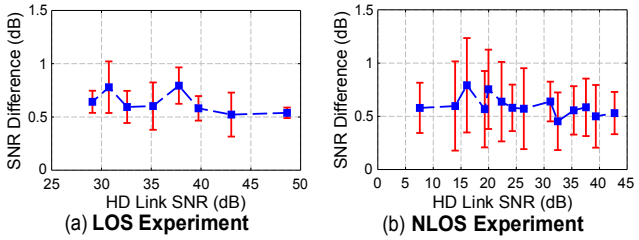


Figure 11: **Dierence between HD and FD link SNR values in the (a) LOS, and (b) NLOS experiments, with** 10 dBm **TX power and 64QAM-3/4 MCS.**

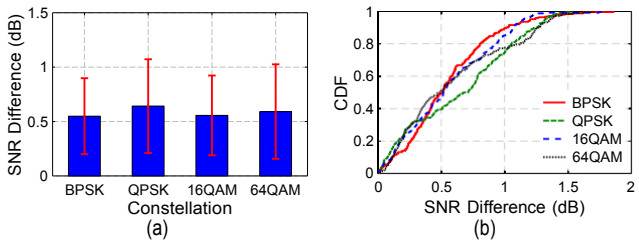


Figure 12: **Dierence between HD and FD link SNR values with** 10 dBm **TX power under varying constellations: (a) mean and standard deviation, and (b) CDF.**

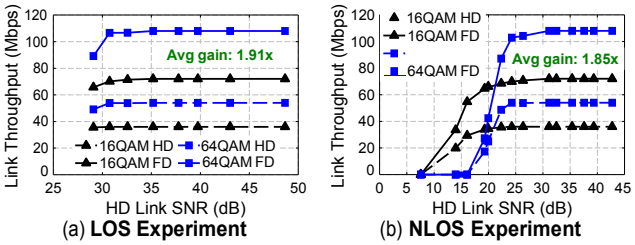


Figure 13: **HD and FD link throughput in the (a) LOS, and (b) NLOS experiments, with** 10 dBm **TX power and 16QAM-3/4 and 64QAM-3/4 MCSs.**

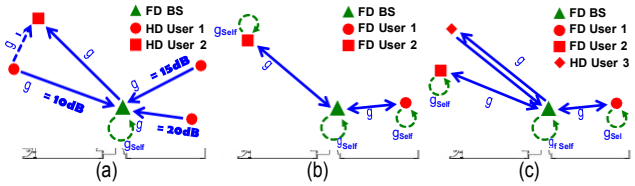


Figure 14: **An example experimental setup for: (a) the UL-DL networks with varying y_{UL} and y_{DL}, (b) heterogeneous 3-node network with one FD BS and 2 FD users, and (c) heterogeneous 4-node networks with one FD BS, 2 FD users, and one HD user.**

and FD link SNR values. Throughout the experiments, link SNR values between 0–50 dB are observed.

Dierence in HD and FD Link SNR Values. Fig. 11 shows the measured link SNR dierence as a function of the HD link SNR (i.e., for dierent user locations) in the LOS and NLOS experiments, respectively, with 64QAM-3/4 MCS. For the LOS experiments, the average link SNR dierence is 0.6 dB with a standard deviation of 0.16 dB. For the NLOS experiments, the average link SNR dierence is 0.63 dB with a standard deviation of 0.31 dB. The SNR dierence has a higher variance in the NLOS experiments, due to the complicated environments (e.g., wooden desks and chairs, metal doors and bookshelves, etc.). In both cases, the link SNR dierence is minimal and uncorrelated with user locations, showing the robustness of the FDE-based FD radio.

Impact of Constellations. Fig. 12 shows the measured link SNR dierence and its CDF with varying constellations and 3/4 coding rate. It can be seen that the link SNR dierence has a mean of 0.58 dB and a standard deviation of 0.4 dB, both of which are uncorrelated with the constellations.

FD Link Throughput and Gain. For each user location in the LOS and NLOS experiments, the HD (resp. FD) link throughput is measured as the highest average data rate across all MCSs achieved by the link when both nodes operate in HD (resp. FD) mode . The FD gain is computed as the ratio between FD and HD throughput values. Recall that the maximal HD data rate is 54 Mbps, an FD link data rate of 108 Mbps can be achieved with an FD link PRR of 1.

Fig. 13 shows the average HD and FD link throughput with varying 16QAM-3/4 and 16QAM-3/4 MCSs, where each point represents the average throughput across 1,000 packets. The results show that with sucient link SNR (e.g., 30 dB for 64QAM-3/4 MCS), the FDE-based FD radios achieve an *exact* link throughput gain of 2⇥. In these scenarios, the HD/FD link always achieves a link PRR of 1 which results in the maximum achievable HD/FD link data rate. With medium link SNR values, where the link PRR less than 1, the average FD link throughput gains across dierent MCSs are 1.91⇥ and 1.85⇥ for the LOS and NLOS experiments, respectively. We note that if higher modulation schemes (e.g., 256QAM) are considered and the corresponding link SNR values are high enough for these schemes, the HD/FD throughput can increase (compared to the values in Fig. 13). However, considering such schemes is not required in order to evaluate the FDE-based cancellers and the FD gain.

6.5 Network-Level FD Gain

We now experimentally evaluate the network-level throughput gain introduced by FD-capable BS and users. The users can signicanlty benet from the FDE-based FD radio suitable for hand-held devices. We compare experimental results to the analysis (e.g., [37]) and demonstrate practical FD gain in dierent network settings. Specically, we consider two types of networks as depicted in Fig. 14: (i) *UL-DL networks* with one FD BS and two HD users with inter-user interference (IUI), and (ii) *heterogeneous HD-FD networks* with HD and FD users. Due to software challenge with implementing

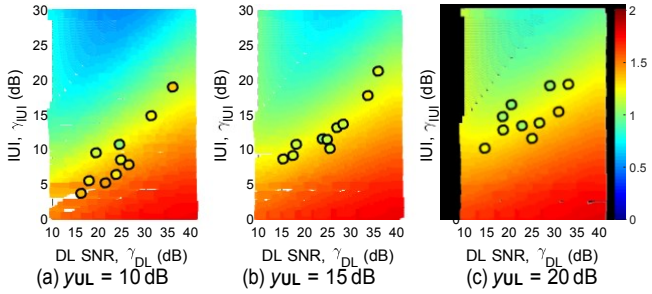


Figure 15: **Analytical (colored surface) and experimental (lled circles) network throughput gain for UL-DL networks consisting of one FD BS and two HD users with varying UL and DL SNR values, and inter-user interference (IUI) levels: (a)** y_{UL} = 10 dB**, (b)** y_{UL} = 15 dB**, and (c)** y_{UL} = 20 dB**. The baseline is the network throughput when the BS is HD.**

a real-time MAC layer using a USRP, we apply a TDMA setting where each (HD or FD) user takes turn to be activated for the same period of time.

6.5.1 UL-DL Networks with IUI. We rst consider UL-DL networks consisting of one FD BS and two HD users (indexed 1 and 2). Without loss of generality, in this setting, user 1 transmits on the UL to the BS, and the BS transmits to user 2 on the DL (see Fig. 14(a)).

Analytical FD gain. We use Shannon's capacity formula $r(y) = B \cdot \log_2(1+y)$ to compute the *analytical throughput* of a link under bandwidth B and link SNR y. If the BS is only HD-capable, the network throughput in a UL-DL network when the UL and DL share the channel in a TDMA manner with equal fraction of time is given by

$$r^{HD}_{UL\text{-}DL} = \frac{B}{2}\log_2(1+y_{UL}) + \frac{B}{2}\log_2(1+y_{DL}), \quad (6)$$

where y_{UL} and y_{DL} are the UL and DL SNRs, respectively. If the BS is FD-capable, the UL and DL can be simultaneously activated with an analytical network throughput of

$$r^{FD}_{UL\text{-}DL} = B\log_2\left(1+\frac{y_{UL}}{1+y_{Self}}\right) + B\log_2\left(1+\frac{y_{DL}}{1+y_{IUI}}\right), \quad (7)$$

where: (i) $\frac{y_{DL}}{1+y_{IUI}}$ is the signal-to-interference-plus-noise ratio (SINR) at the DL HD user, and (ii) y_{Self} is the residual self-interference-to-noise ratio (XINR) at the FD BS. We set y_{Self} = 1 when computing the analytical throughput. Namely, the residual SI power is no higher than the RX noise oor (which can be achieved by the FDE-based FD radio, see Section 6.2). The *analytical FD gain* is then dened as the ratio $r^{FD}_{UL\text{-}DL}/r^{HD}_{UL\text{-}DL}$. Note that the FD gain depends on the coupling between y_{UL}, y_{DL}, and y_{IUI}, which depend on the BS/user locations, their TX power, etc.

Experimental FD gain. The experimental setup is depicted in Fig. 14(a), where the TX power levels of the BS and user 1 are set to be 10 dBm and -10 dBm, respectively. We x the location of the BS and consider dierent UL SNR values of y_{UL} = 10/15/20 dB by placing user 1 at three dierent locations. For each value of y_{UL}, user 2 is placed at 10 dierent locations, resulting in varying y_{DL} and y_{IUI} values.

Table 3: **Average FD Gain in UL-DL Networks with IUI.**

UL SNR, y_{UL}	Analytical FD Gain	Experimental FD Gain
10 dB	1.30	1.25
15 dB	1.23	1.16
20 dB	1.22	1.14

Fig. 15 shows the analytical (colored surface) and experimental (lled circles) FD gain, where the analytical gain is extracted using (6) and (7), and the experimental gain is computed using the measured UL and DL throughput. It can be seen that smaller values of y_{UL} and lower ratios between y_{DL} and y_{IUI} lead to higher throughput gains in both analysis and experiments. The average analytical and experimental FD gains are summarized in Table 3. Due to practical reasons such as the link SNR dierence and its impact on link PRR (see Section 6.3), the experimental FD gain is 7% lower than the analytical FD gain. The results conrm the analy- sis in [37] and demonstrate the practical FD gain achieved in wideband UL-DL networks without any changes in the current network stack (i.e., only bringing FD capability to the BS). Moreover, performance improvements are expected through advanced power control and scheduling schemes.

6.5.2 Heterogeneous 3-Node Networks. We consider heterogeneous HD-FD networks with 3 nodes: one FD BS and two users that can operate in either HD or FD mode (see an example experimental setup in Figs. 1(c) and 14(b)). All 3 nodes have the same 0 dBm TX power so that each user has symmetric UL and DL SNR values of y_i (i = 1, 2). We place user 1 at 5 dierent locations and place user 2 at 10 dierent locations for each location of user 1, resulting in a total number of 50 pairs of (y_1, y_2).

Analytical FD gain. We set the users to share the channel in a TDMA manner. The analytical network throughput in a 3-node network when zero, one, and two users are FD-capable is respectively given by

$$r^{HD} = \frac{B}{2}\log_2(1+y_1) + \frac{B}{2}\log_2(1+y_2), \quad (8)$$

$$r^{HD\text{-}FD}_{\text{User } i \text{ FD}} = B\log_2\left(1+\frac{y_i}{1+y_{Self}}\right) + \frac{B}{2}\log\frac{1+y_{\bar{i}}}{2}, \quad (9)$$

$$r^{FD} = B\log_2\left(1+\frac{y_1}{1+y_{Self}}\right) + B\log_2\left(1+\frac{y_2}{1+y_{Self}}\right), \quad (10)$$

where y_{Self} = 1 is set (similar to Section 6.5.1). We consider both FD gains of $r^{HD\text{-}FD}_{\text{User } i \text{ FD}}/r^{HD}$ (i.e., user i is FD and user $\bar{i}$, i is HD), and r^{FD}/r^{HD} (i.e., both users are FD).

Experimental FD gain. For each pair of (y_1, y_2), experimental FD gain is measured in three cases: (i) only user 1 is FD, (ii) only user 2 is FD, and (iii) both users are FD. Fig. 16 shows

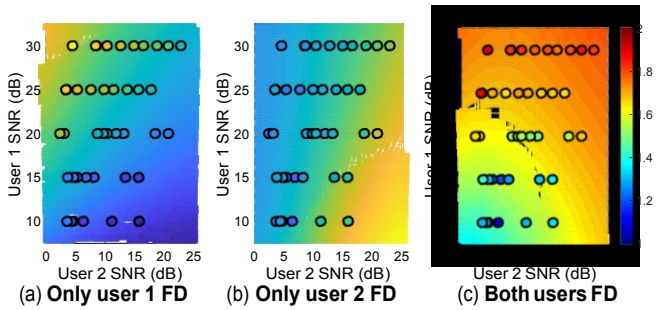


Figure 16: **Analytical (colored surface) and experimental (lled circles) network throughput gain for 3-node networks consisting of one FD BS and two users with varying link SNR values: (a) only user 1 is FD, (b) only user 2 is FD, and (c) both users are FD. The baseline is the network throughput when both users are HD.**

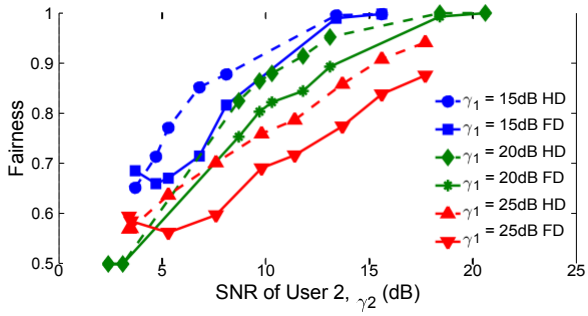


Figure 17: **Measured Jain's fairness index (JFI) in 3-node networks when both users are HD and FD with varying** (y_1, y_2)**.**

the analytical (colored surface) and experimental (lled circles) FD gain for each case. We exclude the results with y_i < 3 dB since the packets cannot be decoded, resulting in a throughput of zero (see Fig. 9).

The results show that with small link SNR values, the experimental FD gain is lower than the analytical value due to the inability to decode the packets. On the other hand, with sucient link SNR values, the experimental FD gain exceeds the analytical FD gain. This is because setting y_{Self} = 1 in (9) and (10) results in a 3 dB SNR loss in the analytical FD link SNR, and thereby in a lower throughput. However, in practice, the packets can be decoded with a link PRR of 1 with sucient link SNRs, resulting in exact twice number of packets being successfully sent over an FD link. Moreover, the FD gain is more signicant when enabling FD capability for users with higher link SNR values.

Another important metric we consider is the fairness between users, which is measured by the Jain's fairness index (JFI). In the considered 3-node networks, the JFI ranges between 1/2 (worst case) and 1 (best case). Fig. 17 shows the measured JFI when both users operate in HD or FD mode. The results show that introducing FD capability results in an average degradation in the network JFI of only 5.6%/4.4%/7.4% for y_1 = 15/20/25 dB, while the average network FD gains

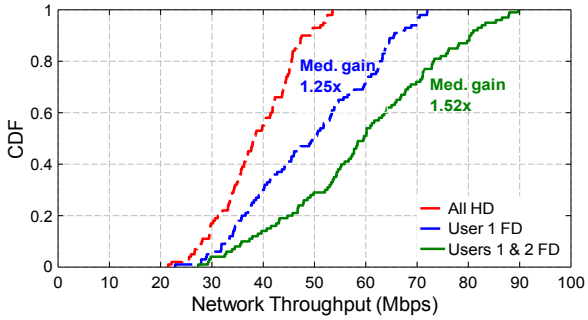


Figure 18: **Experimental network throughput gain for 4-node networks when zero, one, or two users are FD-capable, with** 10 dBm **TX power and varying user locations.**

are 1.32→/1.58→/1.73→, respectively. In addition, the JFI increases with higher and more balanced user SNR values, which is as expected.

6.5.3 Heterogeneous 4-Node Networks. We experimentally study 4-node networks consisting of an FD BS and three users with 10 dBm TX power (see an example experimental setup in Fig. 14(c)). The experimental setup is similar to that described in Section 6.5.2. 100 experiments are conducts where the 3 users are placed at dierent locations with dierent user SNR values. For each experiment, the network throughput is measured in three cases where: (i) zero, (ii) one, and (iii) two users are FD-capable.

Fig. 18 shows the CDF of the network throughput of the three cases, where the measured link SNR varies between 5–45 dB. Overall, median network FD gains of 1.25→ and 1.52→ are achieved in cases with one and two FD users, respectively. The trend shows that in a real-world environment, the total network throughput increases as more users become FD-capable, and the improvement is more signicant with higher user SNR values. Note that we only apply a TDMA scheme and a more advanced MAC layer (e.g., [33]) has the potential to improve the FD gain in these networks.

7 NUMERICAL EVALUATION

In this section, we numerically evaluate and compare the performance of the FDE-based RFIC [49] and PCB cancellers *based on measurements and validated models*. We conrm that the PCB canceller emulates its RFIC counterpart and show that the optimized canceller conguration scheme can signicantly improve the performance of the RFIC canceller. We also evaluate the performance of FDE-based cancellers with respect to the number of FDE taps, M, and desired RF SIC bandwidth, B, and discuss various design tradeos.

7.1 Setup

We use a real, practical antenna interface response, $H_{\text{SI}}(f_k)$, measured in the same setting as described in Section 6.1, and consider M 2 {1, 2, 3, 4} and B 2 {20, 40, 80} MHz. We only

report the RF SIC performance with up to 4 FDE taps since, as we will show, this case can achieve sucient RF SIC up to 80 MHz bandwidth.[14]

We use (2) to both model and evaluate the RFIC canceller with conguration parameters $\{A^{\mathrm{I}}, \phi^{\mathrm{I}}, f_{\mathrm{c},i}, Q_i\}$, since it is shown that a 2nd-order BPF can accurately model the FDE N-path lter [27, 49]. Similar to (P2) (see Section 4.3), the optimized RFIC canceller conguration can be obtained by solving (P3) with $H^{\mathrm{I}}(f_k)$ given by (2).

$$\text{(P3)} \ \min: \sum_{k=1}^{K} \left| H^{\mathrm{I}}_{\mathrm{res}}(f_k) \right|^2 = \sum_{k=1}^{K} \left| H_{\mathrm{SI}}(f_k) - H^{\mathrm{I}}(f_k) \right|^2$$
$$\text{s.t.:} \ A^{\mathrm{I}}_i \in [A^{\mathrm{I}}_{\min}, A^{\mathrm{I}}_{\max}], \ \phi^{\mathrm{I}}_i \in [-n, n],$$
$$f_{\mathrm{c},i} \in [f_{\mathrm{c,min}}, f_{\mathrm{c,max}}], \ Q_i \in [Q_{\min}, Q_{\max}], \ \forall i.$$

Note that in [49], there is no optimization of the RFIC canceller conguration, and the canceller is congured based on a heuristic approach. As we will show, the optimized can- celler scheme outperforms the heuristic approach by an order of magnitude in terms of the amount of RF SIC achieved.

The implemented PCB canceller includes only $M = 2$ FDE taps due to its design (see Section 4). However, it is practically feasible to include more parallel FDE taps. For numerical evaluation purposes, we model the PCB canceller with $M > 2$ FDE taps by extending the validated model (5) with symmetric FDE taps (i.e., all BPFs in the FDE taps behave identically). Although the canceller conguration scheme has a computational complexity of 4^M (i.e., four DoF per FDE tap), we will show that $M = 4$ taps can achieve sucient amount of RF SIC in realistic scenarios.

In practice, the canceller conguration parameters cannot be arbitrarily selected from a continuous range as described in (P2) and (P3). Instead, they are often restricted to discrete values given the resolution of the corresponding hardware components. To address this problem, we evaluate the canceller models in both the *ideal* case and the case *with practical quantization constraints*. The canceller conguration with quantization constraints are obtained by rounding the con- guration parameters returned by solving (P2) or (P3) to their closest quantized values.

In particular, the RFIC canceller has the following constraints: $\forall i$, $A^{\mathrm{I}}_i \in [-40, -10]$ dB, $\phi^{\mathrm{I}}_i \in [-n, n]$, $f_{\mathrm{c},i} \in [875, 925]$ MHz, and $Q_i \in [1, 50]$. When adding practical quantization constraints, we assume that the amplitude A^{I}_i has a 0.25 dB resolution within its range. For ϕ^{I}_i, $f_{\mathrm{c},i}$, and Q_i, an 8-bit resolution constraint is introduced, which is equivalent to $2^8 = 256$ discrete values spaced equally in the given range. These constraints are practically selected and can be easily realized in an IC implementation. The PCB canceller model has following constraints: $\forall i$, $A^{\mathrm{P}}_i \in [-15.5, 0]$ dB, $\phi^{\mathrm{P}}_i \in [-n, n]$, $C_{\mathrm{F},i} \in [0.6, 2.4]$ pF, and $C_{\mathrm{Q},i} \in [2, 14]$ pF. When adding the quantization constraints, we consider 0.5 dB, 0.12 pF, and 0.39 pF resolution to A^{P}_i, $C_{\mathrm{F},i}$, and $C_{\mathrm{Q},i}$, respectively. For ϕ^{P}_i, an 8-bit resolution is introduced. These numbers are consistent with our implementation and experiments (see Sections 4.1 and 6).

[14] We select typical values of 20/40/80 MHz as the desired RF SIC bandwidth, since the circulator has a frequency range of 100 MHz.

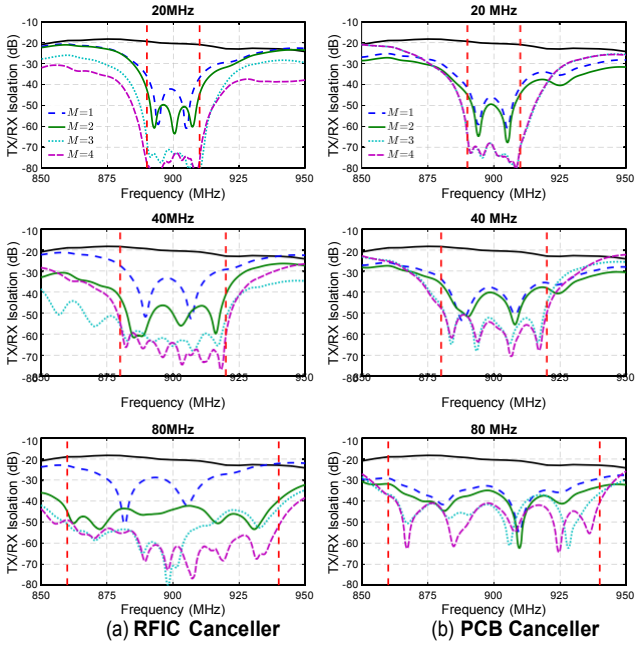
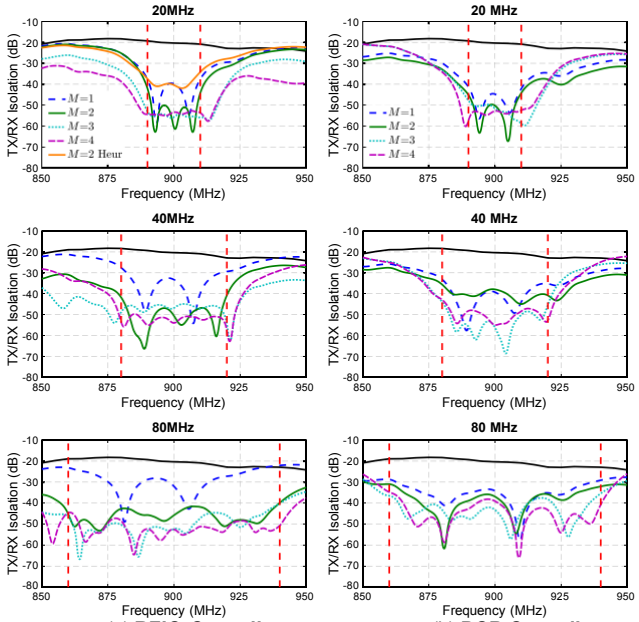


Figure 19: **TX/RX isolation of the antenna interface (black curve) and with the RFIC and PCB cancellers with varying number of FDE taps, $M \in \{1, 2, 3, 4\}$, and desired RF SIC bandwidth, $B \in \{20, 40, 80\}$ MHz, in the ideal case.**

7.2 Performance Evaluation and Comparison between the RFIC and PCB Cancellers

Fig. 19 shows the TX/RX isolation achieved by the RFIC and PCB cancellers with optimized canceller conguration, with varying M and B in the ideal case (i.e., without quantization constraints). It can be seen that: (i) under a given value of B, a larger number of FDE taps results in higher average RF SIC, and (ii) for a larger value of B, more FDE taps are required to achieve sucient RF SIC. For example, the ideal RFIC and PCB cancellers with 2 FDE taps can achieve an average 50/46/42 dB and 50/42/35 dB RF SIC across 20/40/80 MHz bandwidth, respectively.

Fig. 20 shows the TX/RX isolation achieved by the RFIC and PCB cancellers with optimized canceller congura- tion under practical quantization constraints. Comparing to Fig. 19, the results show a performance degradation due to limited hardware resolutions, which is more signicant as M increases. This is because a larger value of M introduces a higher number of DoF with more canceller parameters



(a) **RFIC Canceller** (b) **PCB Canceller**

Figure 20: **TX/RX isolation of the antenna interface (black curve) and with the RFIC and PCB cancellers with varying number of FDE taps,** $M \in \{1, 2, 3, 4\}$**, and desired RF SIC bandwidth,** $B \in \{20, 40, 80\}$ MHz**, under practical quantization constraints.**

that can be exibly controlled. As a result, the RF SIC performance is more sensitive to the coupling between individual FDE tap responses after quantization. The results show that under practical constraints, the RFIC and PCB cancellers with 4 FDE taps can still achieve an average 54/50/45 dB and 52/45/39 dB RF SIC across 20/40/80 MHz bandwidth, respectively. Fig. 20 also shows that the RFIC canceller under the optimized conguration scheme achieves a 10 dB higher RF SIC compared with that achieved by the heuristic approach described in [49] (labeled "Heur").

It is interesting to observe that the RF SIC prole of the PCB canceller with 2 FDE taps is very similar to our experimental results (see Fig. 7 in Section 6.2). It is also worth noting that, in practice, adding more FDE taps cannot improve the amount of RF SIC in some scenarios (e.g., with 20 MHz bandwidth), which is limited by the quantization constraints. However, performance improvement is expected by relaxing these constraints (e.g., through using components with higher resolutions and/or wider tuning ranges).

Table 4 shows the comparison between our implemented PCB canceller and the RFIC canceller presented in [49]. To summarize, we numerically show that the performance of the RFIC and PCB cancellers is similar. The results based on measurements and validated canceller models conrm that the PCB canceller accurately emulates its RFIC counterpart, and that the FDE-based approach is valid and suitable for achieving wideband RF SIC in small-form-factor devices.

Table 4: **Comparison between the PCB and RFIC cancellers.**

	PCB (this work)	RFIC [49]
Center Frequency	900 MHz	1.37 GHz
# of FDE Taps	2	2
Antenna Interface	A single antenna and a circulator	A TX/RX antenna pair
Antenna Isolation	20 dB	35 dB
Canceller SIC (20 MHz)	32 dB	20 dB
Canceller Conguration	Optimization (P2)	Heuristic
Digital SIC	43 dB	N/A
Evaluation	Node/Link/Network	Node

8 CONCLUSION

We designed and implemented a PCB canceller using the FDE technique, which was shown to achieve wideband RF SIC in compact nodes. We presented a PCB canceller model and a scheme for optimizing the canceller conguration. We experimentally evaluated the performance of the FDE-based FD radio at the node, link, and network levels using an SDR testbed. We also compared the RFIC and PCB implementa- tions and discussed various design tradeos of the FDE-based canceller. Future directions include: (i) better design and implementation of FDE-based canceller to support higher TX power handling and RF SIC bandwidth, (ii) extension of the FDE technique to multi-antenna systems, (iii) integration in open-access testbeds, and (iv) development and experimental evaluation of resource allocation and scheduling algorithms tailored for FDE-based FD radios.

ACKNOWLEDGMENTS

This work was supported in part by NSF grants ECCS-1547406, CNS-1650685, and CNS-1827923. We thank Jackson Welles for his contributions to the assembly and testing of the PCB cancellers.

A APPENDIX: THE PCB BPF MODEL

We use transmission (ABCD) matrix to derive $H_i^{\mathrm{B}}(f)$, given by (3). From Fig. 4 and $Y_{\mathrm{F}}(f_k)$ and $Y_{\mathrm{Q}}(f_k)$ in (4),

$$\begin{bmatrix} V_{\text{in}} \\ I_{\text{in}} \end{bmatrix} = \begin{bmatrix} 1 & 0 \\ Y_{\mathrm{Q}}(f_k) & 1 \end{bmatrix} \mathrm{M}^{\mathrm{TL}} \begin{bmatrix} 1 & 0 \\ Y_{\mathrm{F}}(f_k) & 1 \end{bmatrix} \mathrm{M}^{\mathrm{TL}} \begin{bmatrix} 1 & 0 \\ Y_{\mathrm{Q}}(f_k) & 1 \end{bmatrix} \begin{bmatrix} V_{\text{out}} \\ I_{\text{out}} \end{bmatrix}$$
$$:= \begin{bmatrix} M_A^{\mathrm{BPF}}(f_k) & M_B^{\mathrm{BPF}}(f_k) \\ M_C^{\mathrm{BPF}}(f_k) & M_D^{\mathrm{BPF}}(f_k) \end{bmatrix} \begin{bmatrix} V_{\text{out}} \\ I_{\text{out}} \end{bmatrix}, \tag{11}$$

where M^{TL} is the ABCD matrix of a T-Line with wavenumber $f3$, characteristic impedance Z_0, and length l, i.e.,

$$\mathrm{M}^{\mathrm{TL}} = \begin{bmatrix} \cos(f3l) & jZ_0 \sin(f3l) \\ j \sin(f3l)/Z_0 & \cos(f3l) \end{bmatrix}. \tag{12}$$

With the parameters described in Section 4.1, the frequency response of the implemented PCB BPF, $H_i^{\mathrm{B}}(f_k)$, is given by

$$H_i^{\mathrm{B}}(f_k) = \frac{V_{\text{out}}(f_k)}{V_{\text{in}}(f_k)} = \frac{1}{R_{\mathrm{S}}} \cdot \frac{V_{\text{out}}(f_k)}{I_{\text{in}}(f_k)} = \frac{1}{R_{\mathrm{S}}} \cdot \frac{1}{M_C^{\mathrm{BPF}}(f_k)}.$$

Plugging (4) and (12) into (11) yields the model $H_i^{\mathrm{B}}(f)$.

REFERENCES

[1] 2003. Open-access research testbed for next-generation wireless networks (ORBIT). http://www.orbit-lab.org.

[2] 2017. Tutorial: Full-duplex wireless in the ORBIT testbed. http://www.orbit-lab.org/wiki/Tutorials/k0SDR/Tutorial25.

[3] 2018. Cloud enhanced open software dened mobile wireless testbed for city-scale deployment (COSMOS). http://cosmos-lab.org.

[4] 2018. FlexICoN: open-access full-duplex wireless. https://exicon.ee.columbia.edu/gen-2-open-access.

[5] Elsayed Ahmed, Ahmed M Eltawil, and Ashutosh Sabharwal. 2013. Rate gain region and design tradeos for full-duplex wireless communications. *IEEE Trans. Wireless Commun.* 12, 7 (2013), 3556–3565.

[6] Ehsan Aryafar and Alireza Keshavarz-Haddad. 2015. FD2: A directional full duplex communication system for indoor wireless networks. In *Proc. IEEE INFOCOM'15*.

[7] Ehsan Aryafar and Alireza Keshavarz-Haddad. 2018. PAFD: Phased Array Full-Duplex. In *Proc. IEEE INFOCOM'18*.

[8] Ehsan Aryafar, Mohammad Amir Khojastepour, Karthikeyan Sundaresan, Sampath Rangarajan, and Mung Chiang. 2012. MIDU: Enabling MIMO full duplex. In *Proc. ACM MobiCom'12*.

[9] Jingwen Bai and Ashutosh Sabharwal. 2013. Distributed full-duplex via wireless side-channels: Bounds and protocols. *IEEE Trans. Wireless Commun.* 12, 8 (2013), 4162–4173.

[10] Dinesh Bharadia and Sachin Katti. 2014. Full duplex MIMO radios. In *Proc. USENIX NSDI'14*.

[11] Dinesh Bharadia and Sachin Katti. 2015. Fastforward: Fast and constructive full duplex relays. *ACM SIGCOMM CCR* 44, 4 (2015), 199–210.

[12] Dinesh Bharadia, Emily McMilin, and Sachin Katti. 2013. Full duplex radios. In *Proc. ACM SIGCOMM'13*.

[13] Bo Chen, Yue Qiao, Ouyang Zhang, and Kannan Srinivasan. 2015. AirExpress: Enabling seamless in-band wireless multi-hop transmission. In *Proc. ACM MobiCom'15*.

[14] Bo Chen, Vivek Yenamandra, and Kannan Srinivasan. 2015. FlexRadio: Fully Flexible Radios and Networks. In *Proc. USENIX NSDI'15*.

[15] Lu Chen, Fei Wu, Jiaqi Xu, Kannan Srinivasan, and Ness Shro. 2017. BiPass: Enabling end-to-end full duplex. In *Proc. ACM MobiCom'17*.

[16] Shih-Ying Chen, Ting-Feng Huang, Kate Ching-Ju Lin, Y-W Peter Hong, and Ashutosh Sabharwal. 2017. Probabilistic medium access control for full-duplex networks with half-duplex clients. *IEEE Trans. Wireless Commun.* 16, 4 (2017), 2627–2640.

[17] Tingjun Chen, Mahmood Baraani Dastjerdi, Jin Zhou, Harish Krishnaswamy, and Gil Zussman. 2018. Open-access full-duplex wireless in the ORBIT testbed. *arXiv preprint arXiv:1801.03069* (2018).

[18] Tingjun Chen, Jelena Diakonikolas, Javad Ghaderi, and Gil Zussman. 2018. Hybrid scheduling in heterogeneous half- and full-duplex wireless networks. In *Proc. IEEE INFOCOM'18*.

[19] Tingjun Chen, Jin Zhou, Mahmood Baraani Dastjerdi, Jelena Diakonikolas, Harish Krishnaswamy, and Gil Zussman. 2017. Demo abstract: Full-duplex with a compact frequency domain equalization-based RF canceller. In *Proc. IEEE INFOCOM'17*.

[20] Jung Il Choi, Mayank Jain, Kannan Srinivasan, Phil Levis, and Sachin Katti. 2010. Achieving single channel, full duplex wireless communication. In *Proc. ACM MobiCom'10*.

[21] Wooyeol Choi, Hyuk Lim, and Ashutosh Sabharwal. 2015. Power-controlled medium access control protocol for full-duplex WiFi networks. *IEEE Trans. Wireless Commun.* 14, 7 (2015), 3601–3613.

[22] MinKeun Chung, Min Soo Sim, Dongku Kim, and Chan-Byoung Chae. 2017. Compact full duplex MIMO radios in D2D underlaid cellular networks: From system design to prototype results. *IEEE Access* 5 (2017), 16601–16617.

[23] Min Keun Chung, Min Soo Sim, Jaeweon Kim, Dong Ku Kim, and Chan-Byoung Chae. 2015. Prototyping real-time full duplex radios. *IEEE Commun. Mag.* 53, 9 (2015), 56–63.

[24] Jelena Diakonikolas and Gil Zussman. 2018. On the rate regions of single-channel and multi-channel full-duplex links. *IEEE/ACM Trans. Netw.* 26, 1 (2018), 47–60.

[25] Melissa Duarte and Ashutosh Sabharwal. 2010. Full-duplex wireless communications using o-the-shelf radios: Feasibility and rst results. In *Proc. Asilomar Conference on Signals, Systems, and Computers*.

[26] Evan Everett, Clayton Shepard, Lin Zhong, and Ashutosh Sabharwal. 2016. Softnull: Many-antenna full-duplex wireless via digital beamforming. *IEEE Trans. Wireless Commun.* 15, 12 (2016), 8077–8092.

[27] Amir Ghaari, Eric AM Klumperink, Michiel CM Soer, and Bram Nauta. 2011. Tunable high-Q N-path band-pass lters: Modeling and verication. *IEEE J. Solid-State Circuits* 46, 5 (2011), 998–1010.

[28] Sanjay Goyal, Pei Liu, Shivendra S Panwar, Robert A Difazio, Rui Yang, and Erdem Bala. 2015. Full duplex cellular systems: Will doubling interference prevent doubling capacity? *IEEE Commun. Mag.* 53, 5 (2015), 121–127.

[29] Kai-Cheng Hsu, Kate Ching-Ju Lin, and Hung-Yu Wei. 2016. Full-duplex delay-and-forward relaying. In *Proc. ACM MobiHoc'16*.

[30] Kai-Cheng Hsu, Kate Ching-Ju Lin, and Hung-Yu Wei. 2017. Inter-client interference cancellation for full-duplex networks. In *Proc. IEEE INFOCOM'17*.

[31] Mayank Jain, Jung Il Choi, Taemin Kim, Dinesh Bharadia, Siddharth Seth, Kannan Srinivasan, Philip Levis, Sachin Katti, and Prasun Sinha. 2011. Practical, real-time, full duplex wireless. In *Proc. ACM MobiCom'11*.

[32] Mohammad A Khojastepour, Karthik Sundaresan, Sampath Rangarajan, Xinyu Zhang, and Sanaz Barghi. 2011. The case for antenna cancellation for scalable full-duplex wireless communications. In *Proc. ACM HotNets'11*.

[33] Jae Young Kim, Omid Mashayekhi, Hang Qu, Maria Kazandjieva, and Philip Levis. 2013. Janus: A novel MAC protocol for full duplex radio. *CSTR* 2, 7 (2013), 23.

[34] Dani Korpi, Joose Tamminen, Matias Turunen, Timo Huusari, Yang-Seok Choi, Lauri Anttila, Shilpa Talwar, and Mikko Valkama. 2016. Full-duplex mobile device: Pushing the limits. *IEEE Commun, Mag.* 54, 9 (2016), 80–87.

[35] Harish Krishnaswamy and Gil Zussman. 2016. 1 Chip 2x the bandwidth. *IEEE Spectrum* 53, 7 (2016), 38–54.

[36] David López-Pérez, Ming Ding, Holger Claussen, and Amir H Jafari. 2015. Towards 1 Gbps/UE in cellular systems: Understanding ultra-dense small cell deployments. *IEEE Commun. Surv. Tut.* 17, 4 (2015), 2078–2101.

[37] Jelena Marasevic, Jin Zhou, Harish Krishnaswamy, Yuan Zhong, and Gil Zussman. 2017. Resource allocation and rate gains in practical full-duplex systems. *IEEE/ACM Trans. Netw.* 25, 1 (2017), 292–305.

[38] Zhenzhi Qian, Fei Wu, Zizhan Zheng, Kannan Srinivasan, and Ness B Shro. 2017. Concurrent channel probing and data transmission in full-duplex MIMO systems. In *Proc. ACM MobiHoc'17*.

[39] Bozidar Radunovic, Dinan Gunawardena, Peter Key, Alexandre Proutiere, Nikhil Singh, Vlad Balan, and Gerald Dejean. 2010. Rethinking indoor wireless mesh design: Low power, low frequency, full-duplex. In *Proc. IEEE WIMESH'10*.

[40] Negar Reiskarimian, Jin Zhou, Tsung-Hao Chuang, and Harish Krishnaswamy. 2016. Analysis and design of two-port N-path bandpass lters with embedded phase shifting. *IEEE Trans. Circuits Syst. II, Exp. Briefs* 63, 8 (2016), 728–732.

[41] Ashutosh Sabharwal, Philip Schniter, Dongning Guo, Daniel W Bliss, Sampath Rangarajan, and Risto Wichman. 2014. In-band full-duplex wireless: Challenges and opportunities. *IEEE J. Sel. Areas Commun.* 32,

9 (2014), 1637–1652.

[42] Shu Wang, Vignesh Venkateswaran, and Xinyu Zhang. 2017. Fundamental analysis of full-duplex gains in wireless networks. *IEEE/ACM Trans. Netw.* 25, 3 (2017), 1401–1416.

[43] Xiufeng Xie and Xinyu Zhang. 2014. Does full-duplex double the capacity of wireless networks?. In *Proc. IEEE INFOCOM'14*.

[44] Dong Yang, Hazal Yuksel, and Alyosha Molnar. 2015. A wideband highly integrated and widely tunable transceiver for in-band full-duplex communication. *IEEE J. Solid-State Circuits* 50, 5 (2015), 1189–1202.

[45] Yang Yang, Bo Chen, Kannan Srinivasan, and Ness B Shro. 2014. Characterizing the achievable throughput in wireless networks with two active RF chains. In *Proc. IEEE INFOCOM'14*.

[46] Jiakai Yu, Tingjun Chen, Craig Gutterman, Shengxiang Zhu, Gil Zussman, Ivan Seskar, and Dan Kilper. 2019. COSMOS: Optical architecture and prototyping. In *Proc. OSA OFC'19 (to appear)*.

[47] Gan Zheng. 2015. Joint beamforming optimization and power control for full-duplex MIMO two-way relay channel. *IEEE Trans. Signal Process.* 63, 3 (2015).

[48] Jin Zhou, Anandaroop Chakrabarti, Peter Kinget, and Harish Krishnaswamy. 2014. Low-Noise Active Cancellation of Transmitter Leakage and Transmitter Noise in Broadband Wireless Receivers for FDD/Co-Existence. *IEEE J. Solid-State Circuits* 49, 12 (2014), 1–17.

[49] Jin Zhou, Tsung-Hao Chuang, Tolga Dinc, and Harish Krishnaswamy. 2015. Integrated wideband self-interference cancellation in the RF domain for FDD and full-duplex wireless. *IEEE J. Solid-State Circuits* 50, 12 (2015), 3015–3031.

[50] Jin Zhou, Negar Reiskarimian, Jelena Diakonikolas, Tolga Dinc, Tingjun Chen, Gil Zussman, and Harish Krishnaswamy. 2017. Integrated full duplex radios. *IEEE Commun. Mag.* 55, 4 (2017), 142–151.

[51] Wenjie Zhou, Tanmoy Das, Lu Chen, Kannan Srinivasan, and Prasun Sinha. 2016. BASIC: Backbone-assisted successive interference cancellation. In *Proc. ACM MobiCom'16*.