AQuRate: MRAM-based Stochastic Oscillator for Adaptive Quantization Rate Sampling of Sparse Signals

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ABSTRACT

Recently, the promising aspects of compressive sensing have inspired new circuit-level approaches for their efficient realization within the literature. However, most of these recent advances involving novel sampling techniques have been proposed without considering hardware and signal constraints. Additionally, traditional hardware designs for generating non-uniform sampling clock incur large area overhead and power dissipation. Herein, we propose a novel non-uniform clock generator called Adaptive Quantization Rate (AQR) generator using Magnetic Random Access Memory (MRAM)-based stochastic oscillator devices. Our proposed AQR generator provides orders of magnitude reduction in area while offering 6-fold reduced power dissipation, on average, compared to the state-of-the-art non-uniform clock generators.

CCS CONCEPTS

• **Hardware → Data conversion**; **Spintronics and magnetic technologies**; **Emerging architectures**;

KEYWORDS

Analog to Digital Converter, Adaptive Sampling Rate, Non-uniform Clock Generator, MRAM-based Stochastic Oscillator, Compressive Sensing

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1 INTRODUCTION

Recently, non-uniform sampling approaches such as Compressive Sensing (CS) have been proposed to reduce the energy consumption of sampling operation by reducing number of samples in each frame, reduce required storage to save the sampled data, and reduce the data transmission due to lower number of samples taken [15, 18, 19]. Additionally, event-driven sampling, such as level-crossing sampling, has been widely adopted as a promising CS technique to maximize the performance of sampling operation while reducing energy consumption [17]. Furthermore, CS techniques are utilized to sample spectrally sparse wide-band signals close to their information rate rather than their Nyquist rate, which can be a challenge using conventional uniform sampling techniques due to the high cost of the hardware that is capable of performing the sampling operation at a high Nyquist rate.

Despite all the benefits that CS techniques offer, they are typically realized oblivious to the hardware limitations such as energy, bandwidth, and battery capacity. Additionally, signal-dependent constraints such as sparsity and noise level are ignored while studying the quantization rate and resolution trade-off. The aforementioned hardware-dependent and signal-dependent constraints alter during the sampling operation. Thus, an adaptive quantization rate and resolution optimization circuitry is required to maximize sampling performance while minimizing the number of samples to reduce energy consumption, data transmission, and storage. Adaptive quantization rate and resolution sampling might be readily achieved from the algorithm perspective, however it requires a hardware platform that is capable of real-time adaptation according to certain signal behavior such as sparsity rate. Recently, an adaptive optimization of the quantization rate and resolution during signal acquisition has been investigated in [14].

Previous works on adaptive quantization rate and resolution ADCs have been implemented using Complementary Metal Oxide

Semiconductor (CMOS) technology and considering a low-pass signal model [3, 17]. Herein, we propose an spin-based Adaptive quantization rate (AQR) generator circuit that considers the signal dependent constraint as well as hardware limitations. The proposed AQR generator circuit utilized Magnetic Random Access Memory (MRAM)-based stochastic oscillator devices, which offer miniaturization and significant energy savings [6].

2 BACKGROUND AND RELATED WORK

Recently researchers have achieved significant performance improvements using sparse signal recovery techniques. Spectrally sparse signals are utilized in many applications such as frequency hopping communications, musical audio signals, cognitive radio networks, and radar/sonar imaging systems [14]. Additionally, a major challenge in spectrum sensing is that in most cases, the sparse components of the signal are spread over a wide-band spectrum and need to be acquired without prior knowledge of their frequencies. Moreover, spectrum-aware communication networks require Radio Frequency and mixed-signal hardware architectures that can achieve very wide-band but energy-efficient spectrum sensing [14].

The cornerstone to achieving CS approaches and non-uniform sampling techniques is the utilization of an asynchronous pseudo-random clock generator, usually referred to as non-uniform clock generator, which is consisted of a Linear Feedback Shift Register (LFSR) that selects a clock signal at random from a series of ring oscillators with different frequency and phases [3, 4, 10, 11, 13]. In most cases, these circuits require a large number of CMOS transistors and incur significant area overhead and power dissipation. Recently, a novel approach for generating the non-uniform clock using VCMA-MTJ devices is proposed in [11] and the authors have shown that their proposed design can achieve significant area and power dissipation reduction compared to the previous CMOS-based pseudo-random clock generators. However, the authors in [11] considered the frequency of the signal in order to generate the sampling clock, which limits the bandwidth and in case of spectrally sparse signals, where no prior knowledge of frequency is available, their proposed approach will face challenges. Herein, we consider the sparsity rate of the signal to generate the sampling clock. This will minimize the number of samples and results in more energy savings. Furthermore, our proposed design has reduced complexity compared to other designs proposed in the literature due to significant reduction in the CMOS circuit elements.

3 ADAPTIVE QUANTIZATION RATE GENERATOR

3.1 MRAM-based Stochastic Device as a Building Block for AQR generator

In this section, we show that a recently proposed building block with embedded MRAM technology can enable the hardware realization of an AQR generator. The structure of the MRAM-based stochastic device is shown in Fig. 1, which includes a magnetic tunnel junction (MTJ) that is a 2-terminal device with two different resistive levels depending on the orientation of its ferromagnetic (FM) layers, called *fixed layer* and *free layer*. The fixed layer is designed

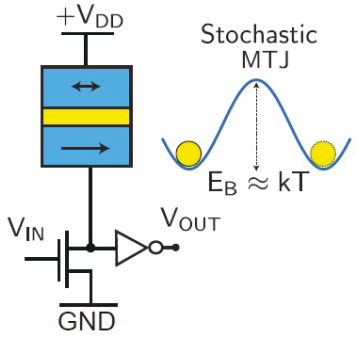

Figure 1: The building block of the proposed spin-based AQR generator [6].

to have a fixed magnetic orientation, while the magnetization orientation of the free layer can be switched. In MRAM-based memory devices, a thermally-stable nanomagnet with a large energy barrier with respect to the thermal energy (kT) is utilized for free layer so that the fixed layer can function as a non-volatile memory. In recent years the use of superparamagnetic MTJs that are not thermally stable have been experimentally and theoretically investigated in search of functional spintronic devices [5, 7–9, 12, 16, 20, 21].

In this paper, we use an MRAM device with a low energy-barrier nanomagnet ($E_B \ll 40kT$), which is thermally unstable [6]. The resistance of an MTJ with such a low energy barrier nanomagnet randomly fluctuates between high (R_{AP}) and low resistance states (R_P). This creates a fluctuating output voltage at the drain of the NMOS transistor, which can be amplified by an inverter circuit to produce a stochastic output that can be modulated by the input voltage. In particular, the output voltage at the drain of the NMOS transistor can be shorted to the ground by reducing its drain-source resistance (r_{ds}) through increasing the input voltage (V_{IN}), or it can be near V_{DD} by increasing the r_{ds} through decreasing V_{IN}. The device operation can be comprehended by considering the MTJ conductance [6]:

$$G_{MTJ} = G_0 \left[1 + m_z \frac{TMR}{(2 + TMR)}\right] \tag{1}$$

where m_z is the free layer magnetization that is stochastically fluctuating due to the thermal noise, G_0 is the average MTJ conductance, $(G_P + G_{AP})/2$, and TMR is the tunneling magnetoresistance ratio. The drain voltage can be expressed as:

$$V_{DRAIN}/V_{DD} = \frac{(2 + TMR) + TMR\, m_z}{(2 + TMR)(1 + \alpha) + TMR\, m_z} \tag{2}$$

where α is the ratio of the transistor conductance (G_T) to the average MTJ conductance (G_0). The maximum fluctuations at the drain occurs when $\alpha \approx 1$, thus the MTJ resistance is approximately equal to the NMOS resistance when $V_{IN} = 0.5V_{DD}$. Since the drain voltage fluctuations are in the order of hundreds of mV for typical TMR values, an additional inverter is used to amplify the noise to produce output voltages ranging from 0 to V_{DD}.

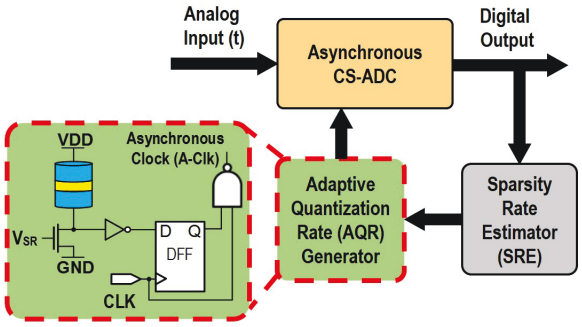

Figure 2: Integration of AQR generator circuit within the Compressive Sensing ADC (CS-ADC) system design.

3.2 AQR Generator Circuit

To realize an effective hybrid emerging device and CMOS circuit, one useful approach can be to consider stochastic and deterministic attributes separately. For instance, Fig. 2 depicts the proposed AQR generator circuit wherein a 2-terminal MTJ realizes stochastic behavior to provide the non-uniform clock generation capability.

The quantized Sparsity Rate Estimator (SRE) module shown in Fig. 2 estimates the sparsity rate of the digital output bit-stream by estimating the sparse spectral components of the digital output using an iterative algorithm. Recently, rapid and optimized sparse component estimation method is proposed in [14]. In the approach proposed in [14] in order to minimize the computational complexity of the sparse component estimation, an sliding window approach is utilized and the algorithm operates only one iteration on each frame of the input by utilizing the previous estimate as an initial value. This will result in gradual convergence of the sparse components to the actual values across iterations. These algorithms can be employed to find the sparsity rate of the signal. In most cases, sparsity rate of analog signals, which can be described as the number of non-zero elements in divided by the total number of elements the sparse representation of the signal, is between 5% to 15% in many applications including those targeted herein.

When the SRE module estimates the sparsity rate of the signal based on the digital output of the previous frame, it will then generate a voltage level according to that sparsity rate of the input analog signal. This voltage, referred to as V_{SR}, will be applied to the gate of the NMOS transistor shown in Fig. 2 and results in an stochastic bit-stream generated by the MRAM-based stochastic oscillator device. The stochastic bit-stream output generated by the MRAM-based stochastic oscillator device will be forwarded to the D-Flip-Flop (D-FF) as shown in Fig. 2 and the result of the 2-input NAND gate between the output of the D-FF and the actual clock of the circuit will generate the required quantization rate to be used for the following frame of the signal acquisition, referred to as Asynchronous Clock (A-Clk) in Fig. 2. Additionally, the SRE module can also used by the recovery algorithms to efficiently recover the sampled signal [14]. Additionally, the A-Clk will be forwarded to the sparse recovery algorithm to provide necessary information about the samples taken from the signal to assist with the signal reconstruction.

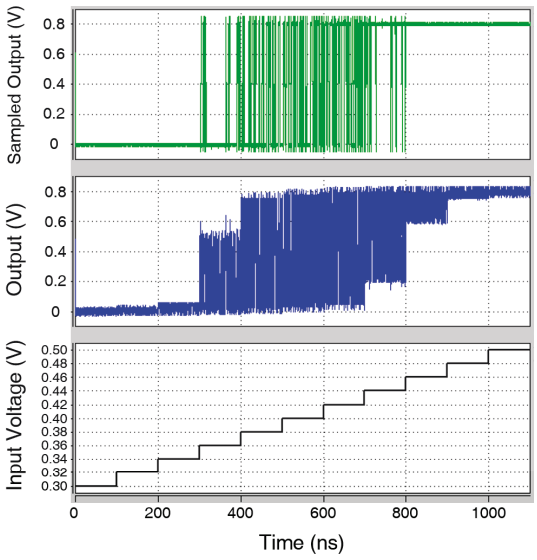

Figure 3: The sampled output of the stochastic MRAM-based building block for AQR generator for various input voltages.

To obtain the relation between the output probability of the stochastic MRAM-based AQR generator and its input voltage, we have applied an input pulse that its amplitude starts from *GND* and is increased by 200mV every 100ns until it reaches V_{DD}. The output of the building block is sampled with a 1GHz clock frequency using a D-FF circuit, as shown in Fig. 3.

4 SIMULATION RESULTS

In order to evaluate and validate the behavior and functionality of the proposed AQR generator circuit, SPICE and MATLAB simulations were performed. We have utilized the 14nm High Performance FinFET Predictive Technology Model (PTM) [2] as well as the MRAM-based stochastic oscillator device model and parameters represented in [6] to implement and evaluate the proposed AQR generator circuit.

According to our simulation results, power dissipation of the proposed AQR generator circuit is 22.64μW on average. Furthermore, the area estimate of the proposed AQR generator circuit in the 14nm technology node according to the transistor count is less than 0.4μm^2. A comparison with other non-uniform clock generators presented in the literature is provided in Table 1. Our results demonstrate that the proposed AQR circuit offers significant area and power dissipation reduction. According to our results, AQR provides significant power dissipation and area reductions compared to the state-of-the-art non-uniform clock generators as shown in Table 1.

As described in Section 3.2, sparsity rate of analog signals is usually within the range of 5%−15%. Fig. 4 depicts an example output of the AQR generator for sampling of a sparse signal with 5% sparsity rate. Moreover, we have embedded our proposed AQR generator within CS recovery algorithms called Orthogonal Matching Pursuit (OMP) and Compressive Sampling Matching Pursuit (CoSaMP)

Table 1: Comparison with recently proposed non-uniform clock generator designs

Design	Tech. ($V_{nominal}$)	Power(μW)	Area(μm^2)
[11]	65nm (1.1V)	26.7	10.6
[13]	65nm (1.1V)	89.7	222.6
[4]	90nm (1.2V)	115.74	1053.7
[3]	28nm (1.0V)	650	N/A
This Work	14nm (0.8V)	22.64	< 0.4

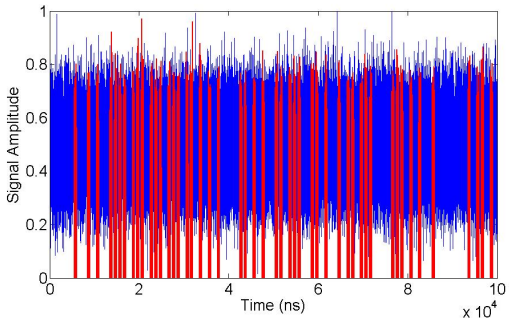

Figure 4: AQR generator output for sampling an analog signal with sparsity rate of 5%. The blue color is the signal and the red color is the sample of the signal using the AQR generator.

[1] in order to evaluate the architectural simulation results and in order to recover the signal from the samples taken using the AQR generator. According to the results, the mean normalized errors of the reconstruction of the signals with 5%, 10%, and 15% sparsity rates using OMP are 0.0504, 0.0446, and 0.0252, respectively. Moreoever, the mean normalized errors of the reconstruction of the signals with 5%, 10%, and 15% sparsity rates using CoSaMP are 0.0487, 0.0304, and 0.0245, respectively.

5 CONCLUSIONS

We have devised a novel non-uniform clock generator called Adaptive quantization rate (AQR) generator using MRAM-based stochastic oscillator devices. Our proposed AQR generator considers signal constraints, such as sparsity rate, as well as hardware constraints, such as area and power dissipation, in order to generate the non-uniform clock for the asynchronous CS-ADC. According to our simulation result, AQR generator provides significant area improvement while achieving power dissipation reduction of 6-fold, on average, compared to similar non-uniform clock generators presented in the literature.

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