MRAM-based Stochastic Oscillators for Adaptive Non-Uniform Sampling of Sparse Signals in IoT Applications

Soheil Salehi[1], Alireza Zaeemzadeh[2], Adrian Tatulian[3], Nazanin Rahnavard[4], and Ronald F. DeMara[5]
Department of Electrical and Computer Engineering
University of Central Florida
Orlando, FL, 32816-2362, USA
{[1]soheil.salehi,[3]jcmaxwell}@knights.ucf.edu, {[2]zaeemzadeh,[4]nazanin}@eecs.ucf.edu, [5]ronald.demara@ucf.edu

Abstract— Recent advances to hardware integration and realization of highly-efficient Compressive Sensing (CS) approaches have inspired novel circuit and architectural-level approaches. These embrace the challenge to design more optimal non-uniform CS solutions that consider device-level constraints for IoT applications wherein lifetime energy, device area, and manufacturing costs are highly-constrained, but meanwhile the sensing environment is rapidly changing. In this manuscript, we develop a novel adaptive hardware-based approach for non-uniform compressive sampling of sparse and time-varying signals. The proposed *Adaptive Sampling of Sparse IoT signals via STochastic-oscillators (ASSIST)* approach intelligently generates the CS measurement matrix by distributing the sensing energy among coefficients by considering the signal characteristics such as sparsity rate and noise level obtained in the previous time step. In our proposed approach, Magnetic Random Access Memory (MRAM)-based stochastic oscillators are utilized to generate the random bitstreams used in the CS measurement matrix. SPICE and MATLAB circuit-algorithm simulation results indicate that ASSIST efficiently achieves the desired non-uniform recovery of the original signals with varying sparsity rates and noise levels.

Index Terms— Adaptive Compressive Sensing, Non-Uniform Compressive Sensing, MRAM-based Stochastic Oscillator.

I. INTRODUCTION

Researchers have recently expanded their efforts to maximize the signal sensing and reconstruction performance while reducing energy consumption for Internet of Things (IoT) applications such as sensors and mobile devices [1], [2]. Recently, Compressive Sensing (CS) has been proposed as a sampling technique aimed at reducing the number of samples taken per frame to decrease energy, storage, and data transmission overheads. CS can be used to sample spectrally-sparse wide-band signals close to the information rate rather than the Nyquist rate, which can alleviate the high cost of hardware performing sampling at high Nyquist rates [3]–[6].

Implementing non-uniform CS in hardware requires a random number generator (RNG) since CS theory assumes random sampling of data [4]. RNGs can be divided into two classes: true RNGs (TRNGs) and pseudo-RNGs (PRNGs). PRNGs include Linear Feedback Shift Registers (LFSR), which begin with a seed value and then continuously update this value by means of a linear function in order to create the illusion of randomness; such designs can suffer from limited quality in the randomness of the output as well as high

energy and area [7]. TRNGs, on the other hand, rely on truly random events such as thermal noise, oscillator jitter, and metastability; TRNG designs can be challenged by limited generation speed as well as post-processing requirements which impose area and power overheads [8].

Previous attempts at TRNG design using spintronics have included use of bistable superparamagnetic tunnel junctions [7], application of sub-threshold voltages for stochastic switching in magnetic tunnel junctions (MTJs) [8] [9], use of MTJ stack arrangements for precessional switching [10], and by means of the voltage-controlled magnetic anisotropy (VCMA) effect [11]. While these designs have been effective in their quality of randomness, they have also involved relatively complex hardware resulting in power and area overhead. Thus, a spin-based TRNG is sought to minimize the power dissipation and area. Furthermore, previous works on non-uniform compressive sensing have been implemented using Complementary Metal Oxide Semiconductor (CMOS) technology [12], [13].

Herein, we propose a spin-based non-uniform compressive sensing circuit-algorithm solution that considers the signal-dependent constraint as well as hardware limitations called *Adaptive Sampling of Sparse IoT signals via STochastic-oscillators (ASSIST)*. The proposed ASSIST approach utilizes Magnetic Random Access Memory (MRAM)-based Stochastic Oscillator (MSO) devices as the main element in TRNGs, which offer miniaturization and significant energy savings [2], [14]. Additionally, MRAM-based Non-Volatile Memory (NVM) is used to store the output of TRNGs, which are the elements of the CS measurement matrix.

The remainder of this paper is organized as follows. Background and related work is provided in Section II. In Section III-A, a detailed description of the MRAM-based Non-Volatile Memory (NVM) devices is given. Then, in Section III-B MRAM-based stochastic bitstream generators used to develop the proposed ASSIST circuit are described. Finally, the proposed ASSIST circuit and architecture are elaborated in Section III-C. Section IV provides the simulation results and comparisons. Finally, Section V concludes this paper while demonstrating the cooperating benefits of emerging and spintronic devices within signal processing applications for IoT.

II. BACKGROUND AND RELATED WORK

Compressive sensing (CS) is a technique for reconstructing a sparse signal of length N using M measurements, with $M \ll N$. The signal is said to be k-sparse if it has at most k non-zero entries in a given basis; the sparsity rate of the signal is defined as $\frac{K}{N}$. The measurement vector $\mathbf{y} \in \mathbb{R}^M$ is related to the signal vector $\mathbf{x} \in \mathbb{R}^N$ by the measurement matrix $\boldsymbol{\Phi} \in \mathbb{R}^{M \times N}$ through the relation $\mathbf{y} = \boldsymbol{\Phi}\mathbf{x}$. While this is an undetermined system with infinitely many solutions, it has been shown that the signal $\mathbf{x}$ can still be recovered from the M measurements by solving the basis pursuit problem:

$$\hat{\mathbf{x}} = \arg\min \|\mathbf{x}\|_1 \text{ s.t. } \mathbf{y} = \boldsymbol{\Phi}\mathbf{x} \qquad (1)$$

where $\|\mathbf{x}\|_1 = \sum_i |\mathbf{x}|$. It has been shown that $\hat{\mathbf{x}}$ reconstructs the original signal vector if $\boldsymbol{\Phi}$ satisfies a special condition known as the Restricted Isometry Property (RIP). An $M \times N$ matrix $\boldsymbol{\Phi}$ satisfies RIP(p) if for any k-sparse vector $\mathbf{x}$:

$$\|\mathbf{x}\|_p (1 - \delta) \le \|\boldsymbol{\Phi}\mathbf{x}\|_p \le \|\mathbf{x}\|_p (1 + \delta), \quad 0 < \delta < 1 \qquad (2)$$

In real-world applications, signals may contain special Regions of Interest (RoI), i.e., subsections of the signal which are more critical to accurately reconstruct than the rest of the signal [5], [6]. Moreover, the sparsity of the signal may be non-uniform. Use of a non-uniform measurement matrix allows RoI and parts of the signal with higher sparsity rates to be sampled with higher frequency (i.e., sampled with a sub-matrix containing a higher density of ones). It has been verified that non-uniform measurement matrices satisfy the RIP condition and therefore may be used for sparse signal sampling [5], [6].

Prior work on sparse measurement matrices includes Gilbert and Indyk [15] who described several CS recovery algorithms using sparse measurement matrices and Jafarpour *et al.* [16] who introduced an efficient and low-complexity sparse recovery algorithm. In addition, Kung *et al.* [17] introduced the concept of *neighbor-weighted decoding* as a means of partitioned compressive sensing, i.e. partitioning a signal into blocks which can then be decoded in parallel [18]. Gan [19] proposed to have blocks in the measurement matrix correspond to independent parts of the signal. While [17] and [19] do not take signal non-uniformity into account, Yu *et al.* [20] proposed saliency-based compressive sensing for image processing, where pixels are divided into blocks and the number of measurements applied to a block depends on the saliency of the pixels in that block. Different schemes for non-uniform measurement matrix design have also been reported in [21] and [22].

Recently researchers have achieved significant performance improvements using sparse signal recovery techniques. Spectrally sparse signals are utilized in many applications such as frequency hopping communications, musical audio signals, cognitive radio networks, and radar/sonar imaging systems [1], [23]. The cornerstone to achieving high-accuracy and efficient CS recovery approaches and non-uniform sampling techniques is the utilization of an adaptive
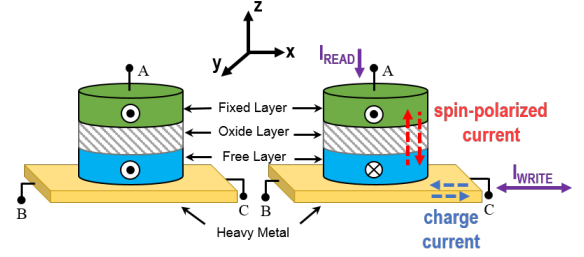

Fig. 1: 3-terminal SHE-MTJ structure, Right: Anti-parallel (high resistance), Left: Parallel (low resistance).

measurement matrix that changes according to the signal characteristics extracted from previous time frames [5], [6]. In most cases, hardware used to implement non-uniform CS sampling and recovery requires a large number of CMOS transistors and incurs significant area overhead and power dissipation [12], [13]. Herein, we propose a low-complexity hardware design to achieve significant power dissipation and area reduction compared to other designs proposed in the literature.

III. ADAPTIVE SAMPLING OF SPARSE IoT SIGNALS VIA STochastic-oscillators (ASSIST)

A. MRAM-based NVM for Storing CS Measurement Matrix

Researchers have focused on exploring the use of Spin-Hall Effect Magnetic Random Access Memory (SHE-MRAM) due to its high reliability and reduced delay for write operation [24]. SHE-MRAM devices consist of Magnetic Tunnel Junctions (MTJs) that are constructed of two ferromagnetic layers, called free layer and fixed layer, and a thin oxide layer, as well as a Heavy Metal (HM) strip as shown in Fig. 1 [25]. A bidirectional charge current through terminals of the HM, B and C, will generate a spin current that passes through the MTJ device in order to modify the polarization of the free layer to represent: 1) high resistance or Anti-Parallel (**AP**) state, and 2) low resistance or Parallel (**P**) state, as depicted in Fig. 1. The states of the MTJ are determined according to the angle, θ, between the magnetization orientation of the ferromagnetic layers. The resistance values of the MTJs in the **P** and **AP** states are obtained using (3) and (4) [25]:

$$R(\theta) = \begin{cases} R_P = R_{MTJ}, & \theta = 0 \\ R_{AP} = R_{MTJ}(1 + TMR), & \theta = \pi \end{cases} \qquad (3)$$

$$TMR(T, V_b) = \frac{2P^2(1 - \alpha_{sp}T^{3/2})^2}{1 - P^2(1 - \alpha_{sp}T^{3/2})^2} \cdot \frac{1}{1 + (\frac{V_b}{V_0})^2} \qquad (4)$$

where $R_{MTJ} = RA/Area$, V_b is the bias voltage, V_0 is a fitting parameter, and α_{sp} is a material-dependent constant.

SHE-MRAM provides separate read and write paths, which increases the reliability due to a reduction in errors caused by read disturbance, while consuming significantly less energy [25]. The critical spin current required for switching the free layer magnetization orientation is expressed by (5) [24]:

$$I_{S,critical} = 2q\alpha M_S V_{MTJ} (H_k + 2\pi M_S) / \overline{h} \qquad (5)$$

TABLE I: Parameters of the 3-terminal SHE-MTJ device.

Parameter	Description	Value
MTJ_{Area}	$l_{MTJ} \times w_{MTJ} \times \pi/4$	$60nm \times 30nm \times \pi/4$
HM_{Volume}	$l_{HM} \times w_{HM} \times t_{HM}$	$100nm \times 60nm \times 3nm$
t_f	Free Layer thickness	1.3 nm
RA	MTJ resistance-area product	$9\ \Omega \cdot \mu m^2$
T	Temperature	358 K
α	Gilbert Damping factor	0.007
P	Spin Polarization	0.52
θ_{SHE}	Spin Hall Angle	0.4
ρ_{HM}	HM Resistivity	$200\mu\Omega.cm$
λ_{sf}	Spin Flip Length	$1.5nm$

TABLE II: Modeling and Simulation Parameters [14].

Parameters	Value
Saturation magnetization (CoFeB) (M_s)	$1100emu/cc$
Free Layer diameter, thickness	$22nm$, $2nm$
Polarization	0.59
TMR	110%
MTJ RA-product	$9\Omega - \mu m^2$
Damping coefficient	0.01
Temperature	$26.85°C$
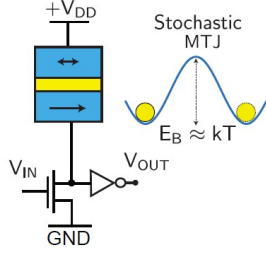
Fig. 2: The building block of the proposed MRAM-based Stochastic Oscillator (MSO) [14].

where V_{MTJ} is the MTJ free layer volume. The relation between SHE-MTJ switching time and the voltage applied to the HM terminals is shown in (6), in which the critical voltage, v_c, is given by (7) [24].

$$\tau_{SHE} = \frac{\tau_0 ln\left(\pi/2\theta_0\right)}{\left(\frac{v}{v_c}\right) - 1} \quad (6)$$

$$v_c = \frac{8\rho I_c}{\theta_{SHE}\left[1 - sech\left(\frac{HM_{thick}}{\lambda_{sf}}\right)\right]\pi HM_{length}} \quad (7)$$

$$\theta_0 = \sqrt{\left(\frac{k_B}{2E_b}\right)} \quad (8)$$

where, θ_0 is the effect of stochastic variation, E_b is the thermal barrier of the magnet of volume V, HM_{length} is the length of the HM, and I_C is the critical charge current for spin-torque induced switching. In order to model the SHE-MTJ, the HM resistance is also required, which is expressed by (9), where ρ_{HM} is the electrical resistivity of HM.

$$R_{HM} = \left(\rho_{HM}.HM_{length}\right)/HM_{width} \times HM_{thick} \quad (9)$$

B. MRAM-based Stochastic Bitstream Generator

Recently, researchers have studied theoretically and experimentally the utilization of thermally unstable superparamagnetic MTJs to realize a variety of functional spintronic devices [14], [26], [27]. Herein, we intend to demonstrate that a recently proposed building block with embedded MRAM technology can enable the hardware realization of a stochastic bitstream generator. The structure of the MRAM-based Stochastic Oscillator (MSO) is depicted in Fig. 2.

Due to the low energy-barrier (i.e. $E_B \ll 40kT$), the MTJ's resistance level fluctuates between the two resistance states of R_{AP} and R_P, which results in the non-uniform stochastic output at the drain of the NMOS transistor shown

in Fig. 2. We can amplify the NMOS drain output to provide full-swing signal, i.e. $[0.0 \to 0.8]$V, using a single inverter circuit. The probability of the output being '1' can be controlled using the input signal connected to the gate of the NMOS transistor. Thus, by increasing the gate voltage of the NMOS transistor, V_{IN}, its drain-source resistance, r_{ds}, will decrease, which will result in the drain voltage to be closer to the GND. On the other hand, by decreasing the gate voltage of the NMOS transistor, V_{IN}, its drain-source resistance, r_{ds}, will increase, which will result in the drain voltage to be closer to the VDD. Considering the MTJ conductance of the MSO, we can observe the behavior of the circuit shown in Fig. 2 [14]:

$$G_{MTJ} = G_0 \left[1 + m_z \frac{TMR}{(2+TMR)}\right] \quad (10)$$

where m_z is the free layer magnetization, G_0 is the average MTJ conductance, $(G_P + G_{AP})/2$, and TMR is the tunneling magnetoresistance ratio. The drain voltage of the NMOS transistor shown in Fig. 2 can be expressed as:

$$V_{DRAIN}/V_{DD} = \frac{(2+TMR) + TMR\ m_z}{(2+TMR)(1+\alpha) + TMR\ m_z} \quad (11)$$

where α is the ratio of the transistor conductance, G_T, to the average MTJ conductance, G_0. When $\alpha \approx 1$ maximum fluctuations can be achieved. This means, when $V_{IN} = V_{DD}/2$, the MTJ resistance is approximately equal to r_{ds}. In this paper, we use a circular nanomagnet with near-zero energy barrier without shape anisotropy. Such magnets have been fabricated and characterized in [28]. We use the embedded MRAM-based model developed in [14] to perform SPICE circuit simulations using the parameters listed in Table II and the nominal voltage of $V_{DD} = 0.8$. The relation between the probability of output being '1' and V_{IN} is depicted in Fig. 3(a), where $V_{IN} = V_{DD}/2 = 400$mV generates an output probability of 50%, as shown in Fig. 3(b).

C. ASSIST Circuit-Architecture Solution

The proposed MRAM-based stochastic bitstream generator circuit is depicted in Fig. 4(a), wherein a 2-terminal low energy-barrier thermally unstable MTJ is utilized. As shown in Fig. 4(a), the output of the MSO is connected to a D-Flip-Flip (D-FF) which is controlled by a Power-Gated Clock (PG-CLK). This will provide control over the number of stochastic outputs provided by the MSO. In other words, by setting the duration of PG-CLK to run for M clock cycles, we would have a stochastic bitstream output, V_M, with the length of M bits, as shown in Fig. 4(a). Additionally, having
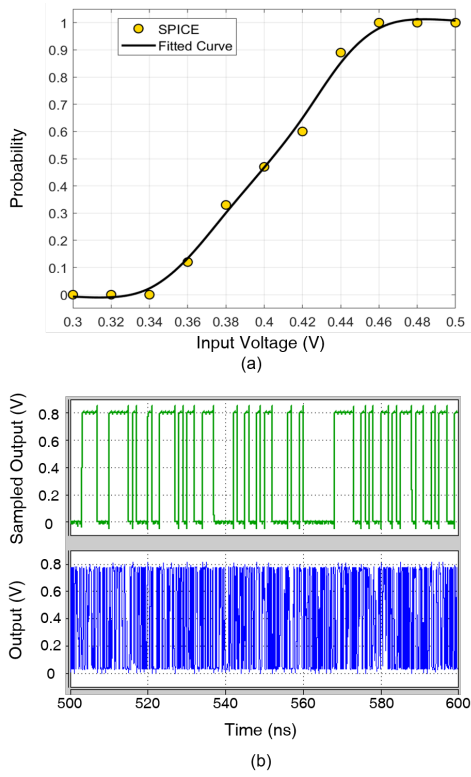
Fig. 3: (a) Output probability of MSO building block for ASSIST versus its input voltage, (b) The output and sampled output voltages for $V_{IN} = 0.5V_{DD} = 400$mV.

control over V_N enables us to adaptively adjust the number of '1's that appear in the output bitstream, V_M. As shown in Fig. 4(c), we have utilized a complementary SHE-MRAM array to store the elements of the measurement matrix and for each column of the measurement matrix we have used an MRAM-based stochastic bitstream generator. Thus, in order to adaptively change the number of rows in the measurement matrix to account for increased sparsity rate, we can adjust V_M accordingly to increase the number of measurements. Furthermore, in order to increase accuracy of the signal recovery, we can increase V_N of the MRAM-based stochastic bitstream generators located in the columns corresponding to the RoI to maintain more '1's in the measurement matrix. It is worth noting that in order to use the MRAM-based stochastic bitstream generator output to write into the SHE-MRAM bit-cells, the PG-CLK clock cycle should be long enough for the write current to flow through the HM of the SHE-MTJs.

As mentioned earlier, we utilize the non-volatile complementary SHE-MRAM array, which will result in a wide read margin and increases reliability of the read operation [25]. Additionally, using a non-volatile complementary SHE-MRAM array enables a clockless read operation that is rapid, reliable, and energy-efficient. In order to use the MSO to write into the SHE-MRAM bit-cells, we utilize the circuit shown in Fig. 4(b). Every column of the SHE-MRAM array shown in Fig. 4(c) is populated using a separate MSO shown in Fig. 4(a).

In order to write into each memory cell, **WWL** should be asserted to enable the write Transmission Gates (TGs), **TGW**. Then by setting Bit Line, **BL**, and Source Line, **SL**, we can write complementary data values in **MTJ** and $\overline{\textbf{MTJ}}$. Additionally, in order to use the MSO to write into the SHE-MTJ devices, the output of the D-FF is connected to the write NMOS transistor, **NW**. Thus, if the output of the D-FF is '1', then **NW** is turned on and will result in a current passing through the SHE-MTJs. On the other hand, if the output of the D-FF is '0', then **NW** won't turn on and the contents of the SHE-MTJs will remain untouched. To read the data stored in the SHE-MTJs, **RWL** is asserted, which turns on the read TG, **TGR**. Additionally, the read transistors, **PR** and **NR**, are enabled. Thus, by applying **VDD** at **BL** and **GND** at **SL**, a read path from **VDD** to **GND** is formed. This will lead to a voltage divider circuit and by connecting the node between the complementary SHE-MTJs, $\textbf{D}_{out}$, to two inverter logic gates, the output voltage will be amplified and presented at the output node, **OUT**.

IV. SIMULATION RESULTS

In order to evaluate and validate the behavior and functionality of the proposed ASSIST approach, SPICE and MATLAB simulations were performed. We have utilized the with 14nm HP-FinFET Predictive Technology Model (PTM) library as well as the MSO device model and parameters represented in [14] along with other circuit parameters and constants listed in Table I and Table II in our simulations to implement and evaluate the proposed ASSIST approach.

According to our simulation results, power dissipation of the stochastic bitstream generator circuit is 23μW on average over a period of $100ns$ for generating a 100-bit bitstream composed of equal likelihood for '0's and '1's. Furthermore, the area estimate of each stochastic bitstream generator circuit in the 14nm technology node according to the transistor count is 0.4μm^2. For a more equitable comparison in terms of area and energy consumption per bit, we have derived (12) and (13) considering general scaling method [29] to normalize the energy consumption per bit and area of the designs listed in Table III. Based on the general scaling method, voltage and area scale at different rates of U and S, respectively. Thus, the energy consumption is scaled with respect to $1/SU^2$ and area per device is scaled according to $1/S^2$ [29].

$$
\begin{aligned}
Energy_{norm} &= \frac{Energy_x}{Energy_{MSO}} \times (\frac{1}{S}) \times (\frac{1}{U})^2 \\
&= \frac{Energy_x}{Energy_{MSO}} \times (\frac{14nm}{Technology}) \times (\frac{0.8V}{V_{DD}})^2
\end{aligned}
\tag{12}
$$

$$
\begin{aligned}
Area_{norm} &= \frac{Area_x}{Area_{MSO}} \times (\frac{1}{S})^2 \\
&= \frac{Area_x}{Area_{MSO}} \times (\frac{14nm}{Technology})^2
\end{aligned}
\tag{13}
$$

where, V_{DD} is the nominal voltage of the technology model, $Technology$ refers to the technology node in nanometers, and subscript x refers to the design that we want to scale its power dissipation and area according to the technology
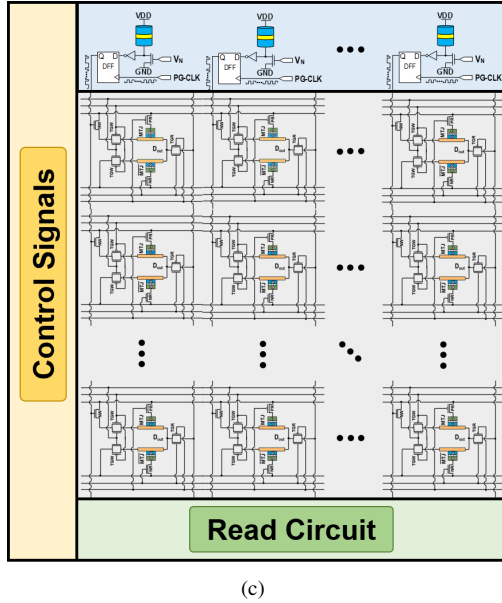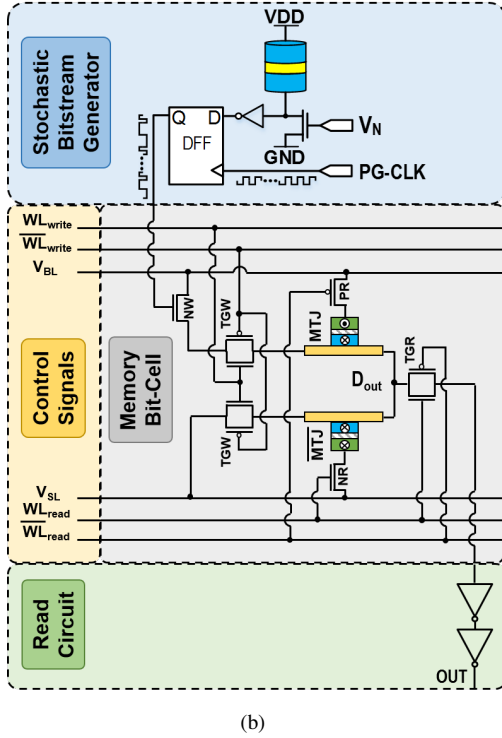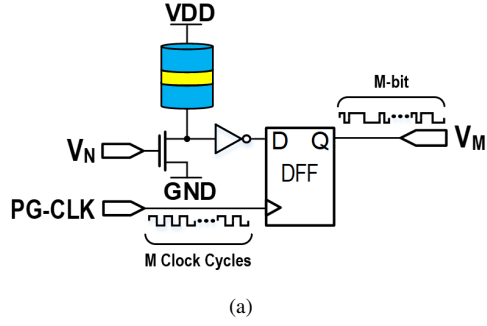
(a)

(b)

(c)

Fig. 4: The proposed ASSIST approach, where (a) depicts the stochastic bitstream generator circuit, (b) shows a complementary MTJ memory bit-cell connected to the stochastic bitstream generator, and (c) illustrates the architecture view.

TABLE III: Comparison with recent TRNG designs

Design	Technology (V_{DD})	Energy$_{norm}$	Area$_{norm}$
[7]	28nm (1.0V)	0.3X	1.25X
[8]	28nm (1.0V)	8.9X	4.8X
[9]	28nm (1.0V)	17.4X	3.7X
This Work	14nm (0.8V)	1X	1X

models. According to (12) and (13), MSO reduces energy consumption per bit by $\sim$ 9-fold on average compared to the state-of-the-art TRNGs as listed in Table III. Additionally, MSO offers up to $\sim$ 3-fold area reduction on average compared to the TRNG designs provided in Table III using the scaling comparison trends accepted in the literature.

Furthermore, transient output of a single complementary SHE-MRAM NVM bit-cell shown in Fig. 4(b) is provided in Fig. 5. According to our simulation results, writing in a NVM bit-cell requires 155.2fJ on average while reading the content of a NVM bit-cell requires 21.9fJ on average. Additionally, based on our simulation results, the standby energy consumption is 36.4aJ. Moreover, in Fig. 6 we use the sampling and recovery algorithm discussed in [5], [23] to evaluate the performance of ASSIST for different values of undersampling ratios, $\frac{M}{N}$, for a signal with sparsity level of $\frac{k}{N} = 0.1$ considering $N = 200$ and with RoI that occupies 10% of the entire signal. This experiment shows that the proposed ASSIST is able to decrease the Time-Averaged Normalized Mean Squared Error (TNMSE) of RoI coefficients up to 2dB for various undersampling ratios. This benefit comes at the cost of reduced performance on total recovery error. It is worth noting that for smaller undersampling ratios, ASSIST incurs no additional performance degradation compared to uniform CS for non-RoI entries.

V. CONCLUSIONS

We have devised a spin-based non-uniform compressive sensing circuit-algorithm solution that considers the signal dependent constraint as well as hardware limitations called Adaptive Sampling of Sparse IoT signals via STochastic-oscillators (ASSIST). High payoff considerations to leverage for device hardware optimization which are advanced herein include the signal sparsity and noise levels. According to our simulation result, the MRAM-based Stochastic Oscillator (MSO) used as a TRNG provides significant area improvement of $\sim$ 3-fold while achieving energy consumption per bit reduction of $\sim$ 9-fold, on average, compared to similar TRNGs presented in the literature. Additionally, our circuit-algorithm simulation results indicate that ASSIST efficiently achieves the desired non-uniform recovery of the original signals with varying sparsity rates and noise levels.
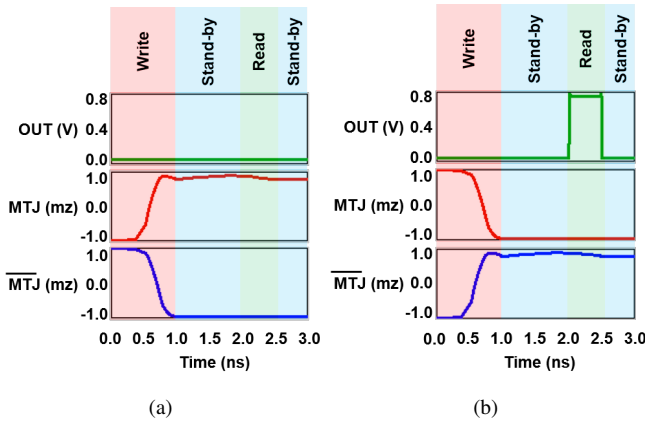
ACKNOWLEDGEMENT

Fig. 5: Transient output for SHE-MRAM NVM array: writing and reading a (a) '0' bit, and (b) '1' bit.
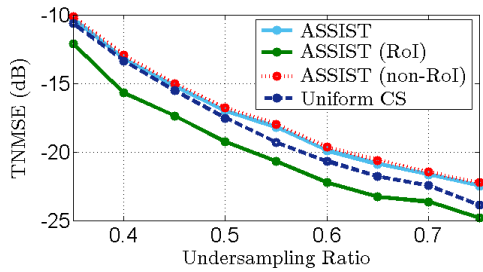

Fig. 6: TNMSE vs. Undersampling Ratio, $\frac{M}{N}$, for a signal with $\frac{k}{N} = 0.1$, $N = 200$, and RoI occupying 10% of N.

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