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Multi-Functional Optical-to-Optical (O/O) Logics with Transistor Laser Integrated Photonic Circuits

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Abstract - *The transistor laser is a four-port, integrated optoelectronic device with two inputs (current and voltage), and two outputs (electrical and optical). Based on its operation principles, an all transistor laser-based, O/O (optical-to-optical) NOR gate was proposed. In this work we apply microwave modeling technique to first simulate the transistor laser device-level operation, then the circuit-level logic operation, and finally propose several new O/O logic circuits for different functionalities and maximize the transistor laser's versatility as a four-port integrated device.*

Keywords: Transistor laser, Optical Logic, Integrated Photonics

Introduction

Optical computing has gained increasing interest at a time when the conventional electronics performance scaling is slowly approaching physical limitation and the beyond-Moore alternative technologies are being actively explored. The electron-photon conversion realized through the electron-hole recombination in semiconductor has enabled fast and efficient data transmission in the optical domain, but challenges remain in achieving logic operations using optical signals in an integrated fashion. The transistor laser (TL), invented in 2005 by Feng and Holonyak [1-2], integrates the E/O (electrical-to-optical) and O/E (optical-to-electrical) conversion functions within a transistor, and bridges the gap between electronics and photonics (Fig. 1). The TL benefits from the inherent electron-photon coupling and the simultaneous electrical-optical dual outputs, making it a promising device to realize optical logic while still being able to interface electronically [3-5].

The TL is a four-port, integrated optoelectronic device with two inputs (current and voltage), and two outputs (electrical and optical): the current input allows the carrier-injection modulation similar to diode lasers, and the voltage input modulates the laser output through intra-cavity photon-assisted tunneling (ICPAT) [6-7], which is an efficient way of controlling the laser cavity loss. Based on its operation principles, an all TL-based, optical-to-optical (O/O) NOR gate was proposed. In this work we apply microwave modeling technique to first simulate the TL device-level operation, then the circuit-level logic operation, and finally propose several new O/O logic circuits for different functionalities and maximize the TL's versatility as a four-port integrated device. The results can be referenced for future device and circuit designs for optimization purpose.

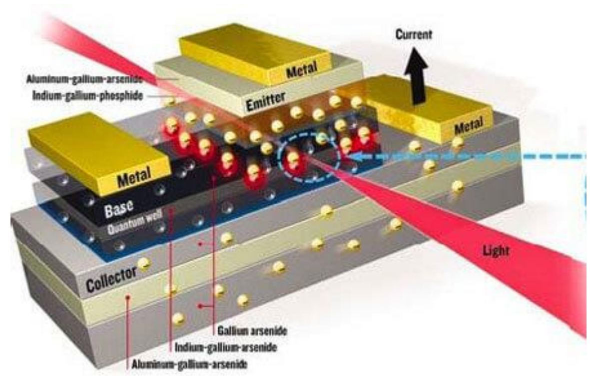

Figure 1: Cross-section schematic of a transistor laser showing the edge-emitting coherent light output [2]

Transistor Laser Operation and Modeling

The TL operates under the control of two inputs: the current input to the transistor base port for carrier-recombination and photon injection in the base quantum-wells (base modulation), and the voltage input on the collector junction for photon absorption under the effect of ICPAT (collector tunneling modulation). The base modulation follows conventional carrier-photon dynamic governed by the Statz-DeMars laser rate equation [8] and can be modeled by treating photon generation as equivalent current components. The tunneling modulation, however, requires a modification to the original carrier-photon rate equation to be able to account for the photon absorption and the associated charge rebalance with the presence of ICPAT (Fig. 2).

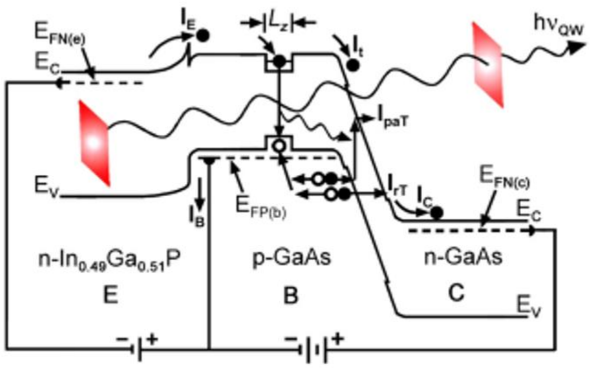

Figure 2: TL band diagram showing the photon absorption and the carrier flow in response to ICPAT in the collector junction [7].

The TL operation and modeling principles have been established previously [9]. The microwave equivalent-circuit model for TL base modulation is plotted in Fig. 3, with RC delay components to model the delay due to the base quantum-well carrier recombination lifetime as well as the laser cavity photon lifetime (escape time). The circuit model was then modified to include the photon/current loss due to ICPAT. Physically ICPAT is a strong function of the junction electric field (base-collector bias) [5], and for modeling purpose we extract the voltage-dependence based on measurement data and incorporate the empirical model in the equivalent-circuit model.

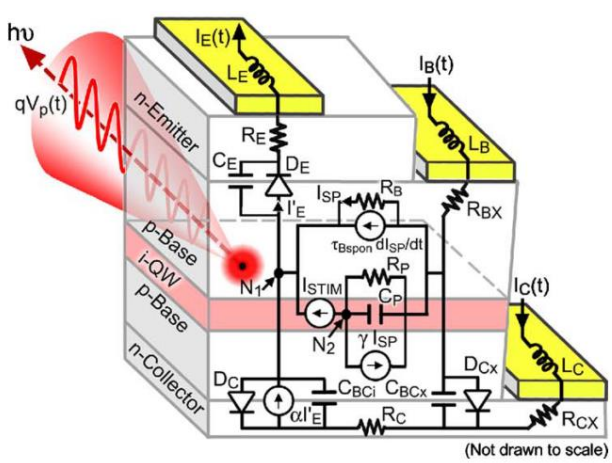

Figure 3: TL microwave equivalent-circuit model for base modulation; the photon generation is modeled as an equivalent current component [9].

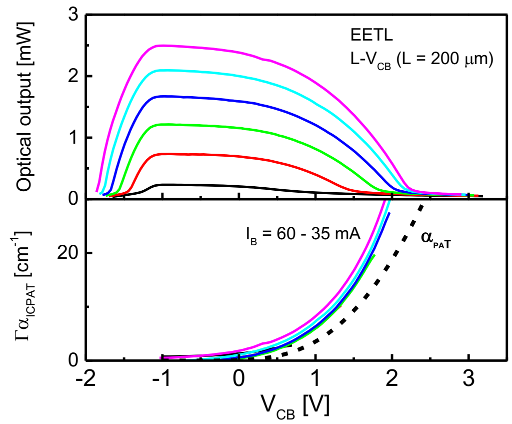

Figure 4: (Top) measured optical output family curves on a 200um long edge-emitting TL (EETL) and (Bottom) the extracted ICPAT absorption coefficient as a function of the junction electric field.

Table 1: TL device parameters used in modeling with scaled junction capacitances

Resistances [Ω]	Capacitances [pF]	Lifetimes [ps]	Misc.
$R_E = 3.6$	$C_E = 0.2$	$\tau_B = 37$	$\beta = 0.1$
$R_C = 0.5$	$C_{BC} = 0.2$	$\tau_{ph} = 2.7$	$I_{th} = 5\ mA$
$R_B = 0.7$			

The TL device parameters such as terminal resistances and junction capacitances can be obtained by fitting the simulated DC and S-parameter to the measurement data. Table 1 summarizes the parameters obtained, but with the junction capacitances scaled down to 200 fF in order to reflected the device scaling and the device performance projection in the near future. The simulated TL bandwidth under both base modulation and tunneling modulation are plotted in Fig. 5 for comparison. At a bias of 10 *mA* ($I/I_{th} = 2$) the tunneling shows a higher bandwidth than conventional base modulation, due to the fact that physically the base modulation is limited by the carrier recombination lifetime in the picosecond range while the tunneling modulation is ultimately limited by the electron tunneling time, which is in the femtosecond range. The simulated eye-diagram of the TL optical output under tunneling modulation at a speed of 40 *Gb/s* (NRZ-OOK, PRBS7) is also shown in Fig. 6.

Transistor Laser-based Logic

With the TL device-level modeling ready, we start building optical logic circuits with TLs. We reference the CMOS active pixel sensor structure

[10], which consists of a photodetector as the pull-down current source and a MOSFET source-follower as the amplifying/output stage. Thus on the source stage we use TL-based P-i-N photodetector as either pull-up or pull-down source (Fig. 7).

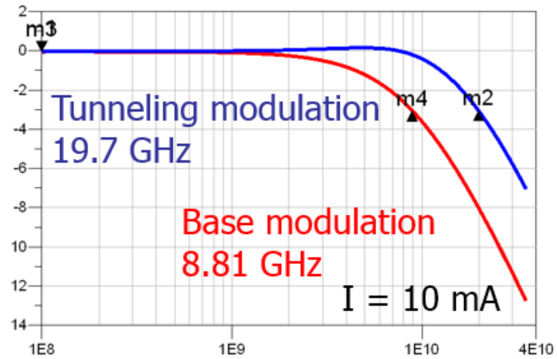

Figure 5: Simulated TL small-signal modulation bandwidth under base modulation (red) vs. tunneling modulation (blue), assuming a bias of 10 mA (I/I_{th} = 2).

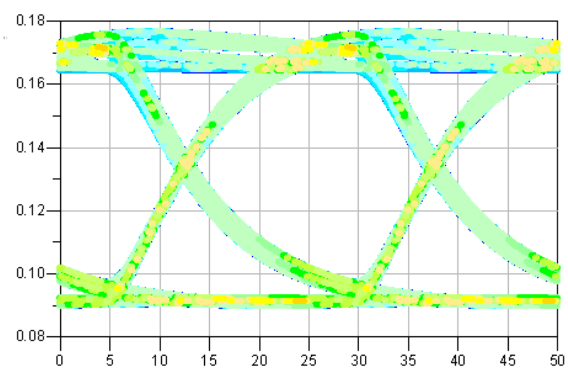

Figure 6: Simulated TL optical output eye-diagram under tunneling modulation at 40 Gb/s showing the open eye; horizontal scale is nanoseconds; vertical scale is arbitrary unit.

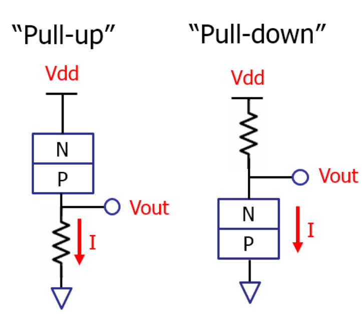

Figure 7: TL-based P-i-N photodetector as pull-up or pull-down source.

Note that since the TL can operate with either base modulation, which is non-inverting (higher base current, higher optical output), and tunneling modulation, which is inverting (higher collector bias, lower optical output), we thus have an additional degree of freedom. Figure 8 shows two possible configurations for TL-based O/O inverter gate.

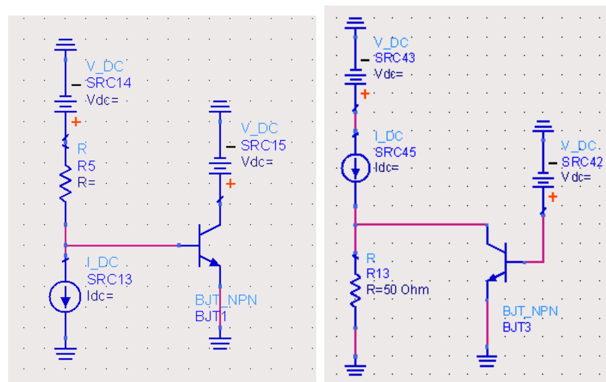

Figure 8: Circuit diagram of two possible configuration for TL-based O/O inverter gate.

In order to explore the performance limit of TL-based logic gates, we assume the extreme scaling scenario with the TL laser threshold as low as 0.1 *mA* and the operating current level at 0.2 *mA*; the power supply needed at this bias level is 1.3 *V* at the base and 0.6 *V* at the collector. Table 2 summarizes the simulated TL-based inverter performance at a data rate of 50 *Gb/s*. The corresponding 50 *Gb/s* eye-diagram of the gate logic operation is simulated and shown in Fig. 9; while deterministic jitter starts to dominate, the simulated eye-diagram shows possibility to pass the data rate.

Table 2: TL-based inverter gate specifications assuming a scaled TL threshold of 0.1 mA

Delay [ps]	1.53
Rise/fall time [ps]	10.77 / 9.75
Jitter RMS [ps]	0.752
Data rate [Gb/s]	50
Power consumption [mW]	0.934

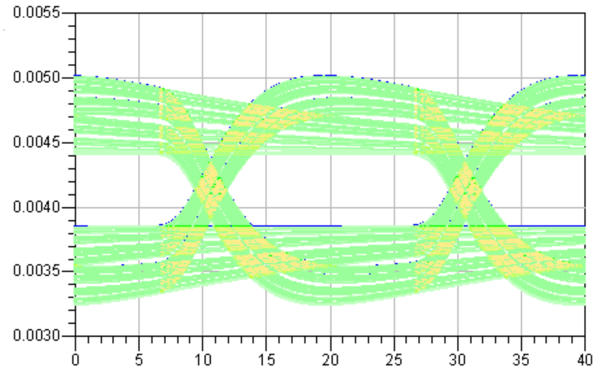

Figure 9: Simulated TL-based inverter logic operation eye-diagram assuming extreme scaling.

Conclusion

In conclusion, based on the integrated functionalities of the transistor laser we complete the device-level equivalent-circuit model, and use the model to construct and simulate the performance of TL-based optical-to-optical logic gates. The simulation results suggest the TL-based logic can potentially achieve very high speed, but further optimizations are needed to fully utilize the entire transistor laser logic family. The model and simulator we build will benefit future design iterations.

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