A Comparison of 100 kW SiC DC-DC Converters for Electric Vehicles

Ze Ni, Yanchao Li, Chengkun Liu, Mengxuan Wei, and Dong Cao
Electrical and Computer Engineering Dept., North Dakota State University
ze.ni@ndsu.edu

Abstract - **This paper compares three different dc-dc topologies, i.e. boost converter, three-level flying capacitor multilevel converter (FCMC) and one-cell switching tank converter (STC) for a 100 kW electric vehicle power electronic system. This bidirectional dc-dc converter targets 300 V - 600 V voltage conversion. Total semiconductor loss index (TSLI) has been proposed to evaluate topologies and device technologies. The boost converter and one-cell STC have been fairly compared by utilizing this index. The simulation results of a 100 kW one-cell STC working at zero current switching (ZCS) mode have been provided. A 100 kW hardware prototype using 1200 V 600 A SiC power module has been built. The estimated efficiency is about 99.2% at 30 kW, 99.13% at half load, and 98.64% at full load. The power density of the main circuits is about 42 kW/L.**

I. INTRODUCTION

In electric vehicle systems, a high DC bus voltage is needed to be interfaced with a three-phase inverter to drive the electric motors or generators [1]–[3]. To step up the relatively low battery voltage to this higher DC busbar voltage, a dc-dc converter is often applied. Typical voltage ratings are 300 V input battery and 650 V DC bus [4]. This dc-dc converter not only regulates the bus voltage, but also protects the battery from over/under voltage, excessive charge/discharge currents [4]–[6]. A recent report from U.S. Department of Energy [7] estimates that by 2025, the power density of the electric traction drive system is supposed to exceed 100 kW/L based on 100 kW power level. This indicates the importance of a proper topology and optimized device and passive component design.

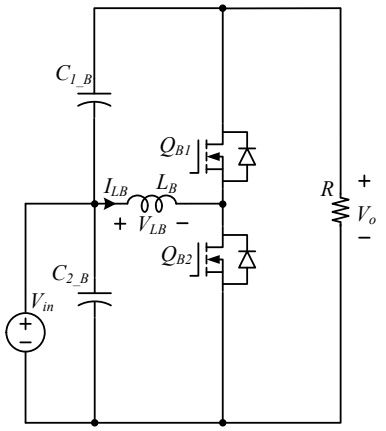
Traditional boost converter is a widely studied solution for this application. A 40 kW bidirectional dc-dc converter based on boost topology is designed in [8] with 6 kW/L power density working at 20 kHz switching frequency. However, it suffers from low efficiency and bulky reactive components. Also based on boost converter, a 3-phase interleaved converter with discrete inductors achieves a power density of 30.8 kW/L and 97.9% efficiency [9]. But the total inductor core volume is as bulky as about 1.3 Liters. To overcome this issue, constant frequency quasi square wave zero voltage switching (ZVS) converter is studied [10]. But it is inefficient at light load. Variable-frequency boundary mode quasi square wave ZVS control is applied in a 200 kW Si IGBT based prototype [4] to further increase the peak efficiency to 98%. However, the power density is only 6 kW/L. A 150 kW, 8.6 L interleaved boost dc-dc converter is designed with multiple DC sources [11]. But the power density is 17.44 kW/L, which is still low considering the above presented U.S. Department of Energy 2025 goal. Another commonly investigated topology for this application is flying capacitor multilevel converter (FCMC) [1][12]–[16]. Over 97% efficiency at 30 kW continuous operation is claimed in [1] by using FCMC with around 8.612 kW/L power density. However, it is difficult to realize a compact design considering the separate locations of the DC-side resonant inductor and AC-side resonant capacitor. SiC MOSFET power modules have shown better performance compared with Si counterparts in high-power, high-frequency applications [17]–[20]. 1200 V 100 A SiC MOSFET power modules from Cree have been applied in a 60 kW dc-dc converter, which can achieve 20 kW/L power density [21]. But 75 kHz hard-switching operation doesn't fully utilize their advantages, which degrades overall 98.7% peak efficiency. These days, resonant switched capacitor converters are investigated for their modularity, high power density and high efficiency [15][22]–[25]. But the high-power applications of this group of topologies are not so well investigated, which needs to be compared fairly with other topologies.

Since different topologies use various voltage rating devices, it is challenging to compare the semiconductor die area usage among topologies. Dr. B. Jayant Baliga proposed a device-level index called figure of merit in [26], but it fails to evaluate the total device power loss among different topologies by using only on-resistance and the total gate charge. Total switching device power is defined in [27] using the product of switch voltage and current stresses as the evaluation method. But it is not able to indicate the optimized die area for different topologies. Relative total semiconductor chip area is proposed in [28], but it does not consider the relationship between total die area and the total device power loss.

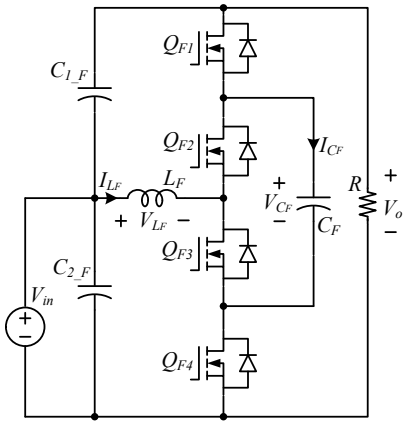
This paper will compare three dc-dc converter topologies and possible device candidates for this high-power electric vehicle application by using the proposed total semiconductor loss index. By utilizing SiC MOSFET power modules, a 100 kW 300 V – 600 V one-cell STC prototype is built with ZCS achieved. The topology comparison, simulation and theoretical results, the designed prototype will be presented.

II. TOPOLOGY COMPARISON

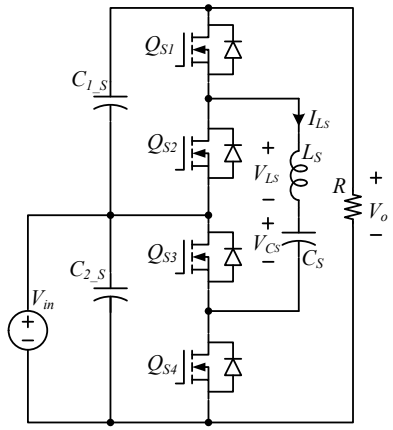
Fig. 1 shows the investigated three topologies, i.e. conventional boost converter, three-level flying capacitor multilevel converter (3-level FCMC) and one-cell switched tank converter (STC) with resonant inductor on the AC side. To evaluate the inductor and capacitor design differences, the corresponding resonant inductor current and voltage



(a) Boost converter



(b) Three-level flying capacitor multi-level converter



(c) One-cell switched tank converter

Fig. 1: Three investigated dc-dc converters

waveforms are shown in Fig. 2. The resonant capacitor voltage and current waveforms are presented in Fig. 3.

Multiple topologies such as boost converter, FCMC could achieve relatively high efficiency by selecting specific semiconductor die areas at the same power rating. But different from the boost converter, the FCMC and STC topologies utilize the devices with lower voltage rating. Thus, how to evaluate these topologies needs to be deliberated. To evaluate device technologies on converter topologies and relate the device power loss with the total die area usage so that minimal device

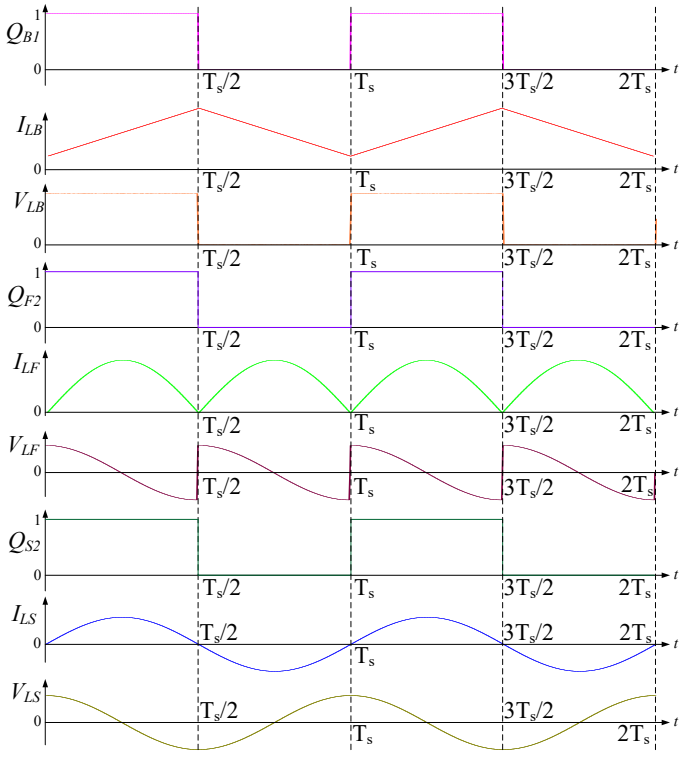


Fig. 2: Comparison of inductor current and voltage

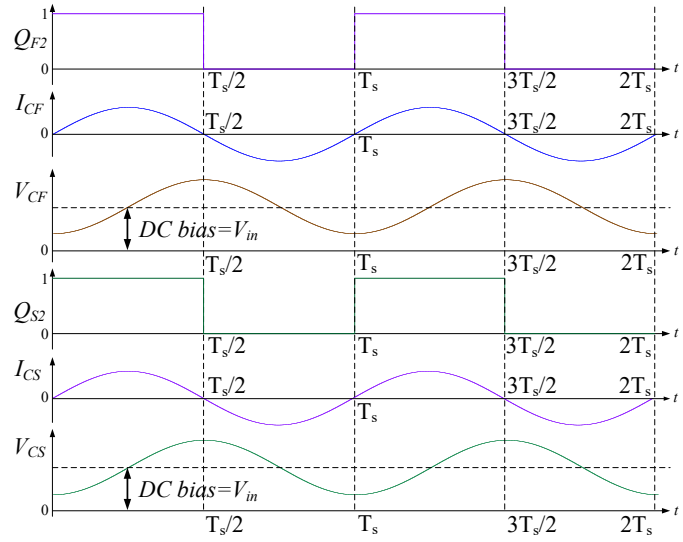


Fig. 3: Comparison of capacitor current and voltage

power loss with an optimized die area can be achieved, the total semiconductor loss index (TSLI) is defined in Eq. (1).

$$\begin{aligned} TSLI &= \frac{1}{P_o}\left(P_{cond}(A_{die\_total}) + P_{sw}(A_{die\_total})\right) \\ &= P^*_{cond}(A_{die\_total}) + P^*_{sw}(A_{die\_total}) \\ &= P^*_{cond}(A_{die\_total}) + P^*_{Gate\_charge}(A_{die\_total}) \\ &+ P^*_{turn\_on}(A_{die\_total}) + P^*_{turn\_off}(A_{die\_total}) \end{aligned} \quad (1)$$

Where, P_{cond}, P_{sw} are total device conduction and switching loss. A_{die_total} is total die area of the converter devices. P_{cond}, P_{sw}

are the functions of total die area. P_{cond}^*, P_{sw}^* are the corresponding loss normalized by output power P_o. Normalized switching loss is further categorized into gate charge induced switching loss $P_{Gate\_charge}^*$, turn-on and turn-off switching loss $P_{turn\_on}^*$, $P_{turn\_off}^*$.

In the ZCS operation, the switching loss could be estimated by the Coss discharged induced turn-on loss. So, the TSLI can be further shown in Eq. (2).

$$TSLI = P_{cond}^*(A_{die\_total}) + P_{Gate\_charge}^*(A_{die\_total}) + P_{C_{oss}}^*(A_{die\_total}) \tag{2}$$

From Eq.(6.211) in [26], the device conduction loss is negatively proportional to the active die area. Hence, the device conduction loss can be expressed as Eq. (3) shows.

$$\begin{aligned} &P_{cond}^*(A_{die\_total}) \\ &= \frac{1}{P_o}\sum_{i=1}^{N}\left[I_{RMS\_S(i)}^2 \cdot \left(R_{ds(on)}\right)_{(i)}\right] \\ &= \frac{1}{P_o}\sum_{i=1}^{N}\left(I_{RMS\_S(i)}^2 \cdot \frac{\alpha_i(\xi_i, V_{B(i)})}{\kappa_i A_{die\_total}}\right) \end{aligned} \tag{3}$$

Where, N is the number of active switches, $I_{RMS\_S(i)}$ is the switch RMS current, $R_{ds(on)}$ is the switch on-resistance. $\alpha_i(\xi_i, V_{B(i)})$ is the product of on-resistance and die area, determined by the device technology dependent coefficient ξ_i and the voltage rating $V_{B(i)}$. κ_i is the die cutting factor ranging from 0 to 1, reflecting different cutting strategies for the dies used by specific switches. The sum of each κ_i equals to 1.

According to Eq.(6.211) in [26], when the die area is enlarged, the input capacitance increases, which means larger gate current is needed to charge the input capacitor and thus increases the gate charge induced switching loss, which is presented in Eq. (4).

$$\begin{aligned} P_{Gate\_charge}^* &= \frac{1}{P_o}\sum_{i=1}^{N}\left[\left(Q_g\right)_{(i)} \cdot V_{gs(i)} \cdot f_{s(i)}\right] \\ &= \frac{1}{P_o}\sum_{i=1}^{N}\left(\beta_i \cdot \kappa_i A_{die\_total} \cdot V_{gs(i)} \cdot f_{s(i)}\right) \end{aligned} \tag{4}$$

Where, f_s is the switching frequency. Q_g is the total gate charge. V_{gs} is the difference of the maximum and minimum gate-source voltages. β_i is the total gate charge per die area, dependent on the device technology. Besides, turn-on and turn-off switching losses are explained in Eq. (5) and (6), respectively. The turn-on energy E_{on} and turn-off energy E_{off} are functions of turn-on and turn-off drain current.

$$P_{turn\_on}^* = \frac{1}{P_o}\sum_{i=1}^{N}\left[\left(E_{on}\right)_{(i)} \cdot f_{s(i)}\right] \tag{5}$$

$$P_{turn\_off}^* = \frac{1}{P_o}\sum_{i=1}^{N}\left[\left(E_{off}\right)_{(i)} \cdot f_{s(i)}\right] \tag{6}$$

The output capacitance C_{oss} discharge induced turn-on switching loss is part of the total turn-on switching loss. From Page 409 in [26], the gate-drain capacitance C_{gd} increases with the die area. From Eq.(6.174), (6.175), (6.178) in [26], the drain-source capacitance C_{ds} is positively proportional to the junction area. Thus, C_{oss} (equal to $C_{gd} + C_{ds}$) discharge induced turn-on switching loss is positively related to the die area. The C_{oss} induced turn-on switching loss is shown in Eq. (7).

$$\begin{aligned} P_{C_{oss}}^* &= \frac{1}{P_o}\sum_{i=1}^{N}\left[C_{oss(i)} \cdot \left(V_{ds(i)}\right)^2 \cdot f_{s(i)}\right] \\ &= \frac{1}{P_o}\sum_{i=1}^{N}\left[\gamma_i \cdot \kappa_i A_{die\_total} \cdot \left(V_{ds(i)}\right)^2 \cdot f_{s(i)}\right] \end{aligned} \tag{7}$$

Where, V_{ds} is drain-source voltage. γ_i is the device output capacitance per die area, which is dependent on the device technologies as well. For a specific circuit topology, when the output power and switching frequency are fixed, theoretically it is possible to derive an optimum die area for each switch to achieve the minimized total device power loss. In other words, when the total device power loss is the same between two topologies under specific conditions, the one with smaller total die area can achieve more efficient die utilization. These two different evaluation perspectives based on the above SLI parameter can provide more comprehensive understandings between the total device power loss and semiconductor die area.

In this comparison, the boost converter is assumed to operate at continuous conduction mode and the inductor current ripple is 30% of its average current. Thus, the device turn-on and turn-off losses are considered. 3-level FCMC and one-cell STC are designed to operate at ZCS mode and the device power loss of these two is the same. Coss losses are included in the switching losses of the switches in the one-cell STC.

Since the voltage rating of the switches in the boost converter is twice the voltage stress (2×600 V), only the dies with 1200 V voltage rating are considered, which are S4103 and CPM2-1200-0025B. The turn-on and turn-off power loss of S4103 are derived from the switching energy vs. drain current curve in the datasheet of Rohm 1200 V SCT3022KL SiC MOSFET since it shares the same on-resistance and current rating information with the S4103 die. While the turn-on and turn-off power loss of CPM2-1200-0025B are derived from the switching energy vs. drain current curve in the datasheet of Cree 1200 V C2M0025120D SiC MOSFET since it shares the similar on-resistance and current rating information with the CPM2-1200-0025B die.

Total semiconductor power loss is compared in Fig. 4. With

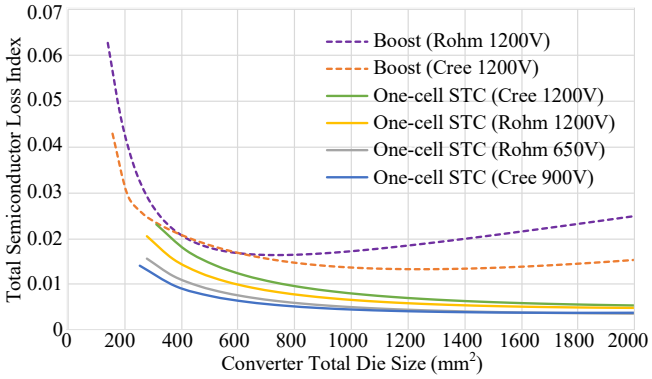
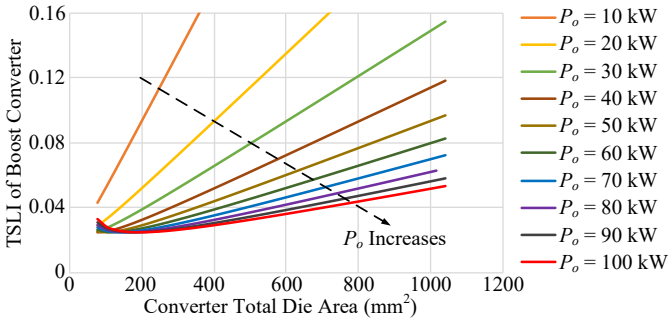


Fig. 4: TLSI comparison between one-cell STC and boost converter with different SiC dies

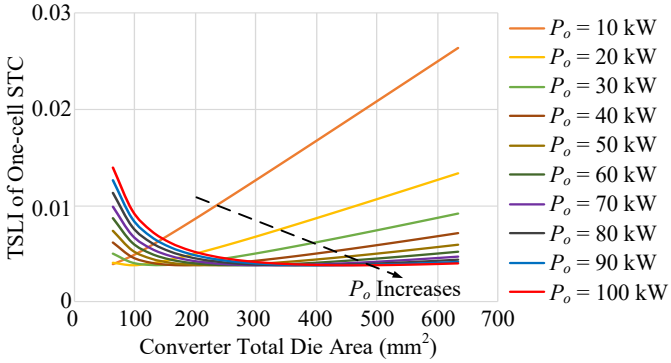
the same total die area, one-cell STC achieves lower total semiconductor power loss compared with boost converter due to higher switching loss of the boost converter.

Compared with 3-level FCMC, one-cell STC can achieve better device clamping and allow the converter to be designed in a more compact way because the inductor is on the AC side. Thus, one-cell STC is selected in this paper.

TSLI can also reflect the relationship between the total device power loss and the output power. Fig. 5(a) and (b) show the TSLI vs. the total converter die area with different output power of boost converter and one-cell STC, respectively, at 100 kHz switching frequency. Based on the TSLI comparison results in Fig. 4, the Cree 1200 V CPM2-1200-0025B SiC die performs best in boost converter and the Cree 900 V CPM3-0900-0010A SiC die works most effectively in the one-cell STC topology. Thus, in the below evaluation, these two SiC dies are selected for the corresponding topologies. In different output power, the boost converter inductor current ripple is maintained as 30% the average current [29]. As the output power increases, the TSLI of both the two topologies decreases, which indicates smaller total device loss at the same converter die area usage.



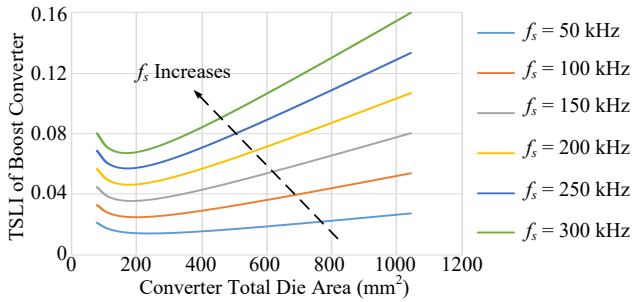
(a) Boost converter TSLI vs. die area with different P_o



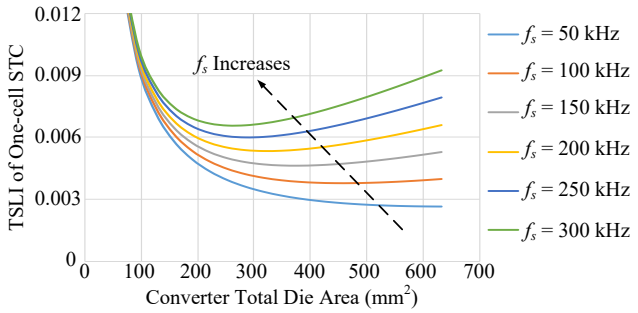
(b) One-cell STC TSLI vs. die area with different P_o

Fig. 5: TSLI vs. die area with different output power

Besides, the proposed TSLI can be also used to present the impact of the switching frequency on the total device power loss. Fig. 6(a) and (b) illustrate the TSLI vs. the total converter die area with different switching frequency of boost converter and one-cell STC, respectively, at 100 kW output power. When the switching frequency increases, the TSLI of both the two topologies increases as well, which indicates larger total device power loss at the same converter die area usage.



(a) Boost converter TSLI vs. die area with different f_s

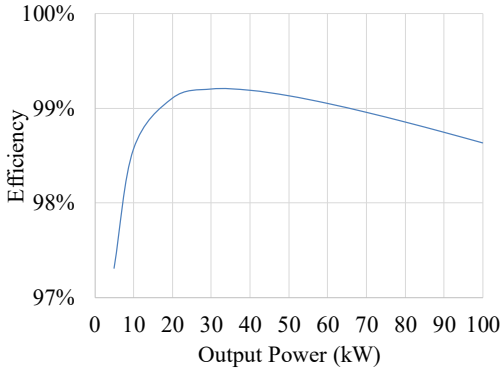


(b) One-cell STC TSLI vs. die area with different f_s

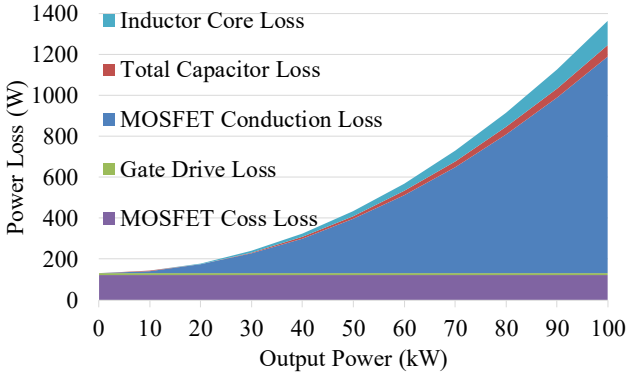
Fig. 6: TSLI vs. die area with different switching frequency

III. Theoretical Analysis and Simulation

The theoretical efficiency and power loss breakdown are estimated in Fig. 7. The conduction loss has been calculated



(a) Estimated efficiency vs. output power

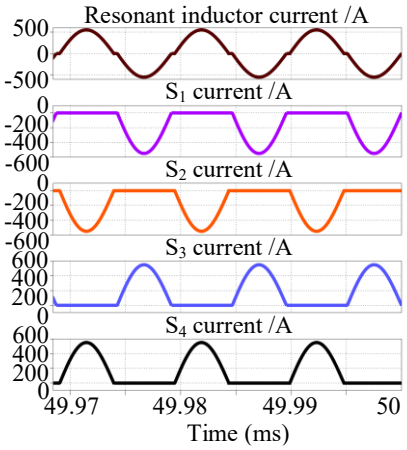


(b) Theoretical power loss breakdown

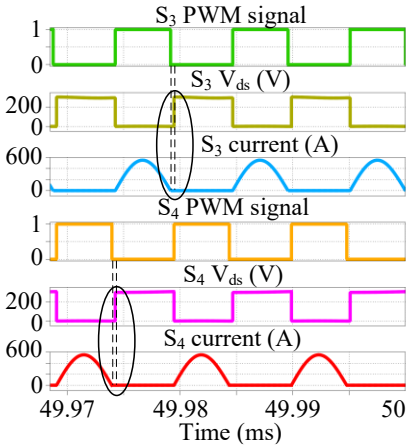
Fig. 7: Theoretical efficiency and power loss breakdown

considering two additional aspects. One is the fact that on-resistance increase with the temperature rise. The other is the deadtime induced switch RMS current increase.

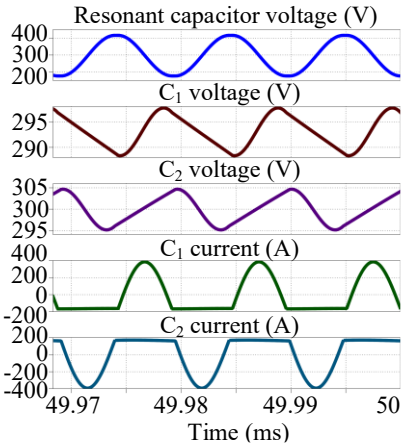
A 300 V 600 V 100 kW one-cell STC operated at ZCS is simulated in PLECS. The simulation results are shown in Fig. 8 with the switching frequency tuned to 96 kHz and the deadtime set as 300 ns. From Fig. 8(b), the switch current I_d decreases to zero before the drain-source voltage V_{ds} starts to rise. Thus, ZCS turn off has been achieved.



(a) Simulated inductor and switch current



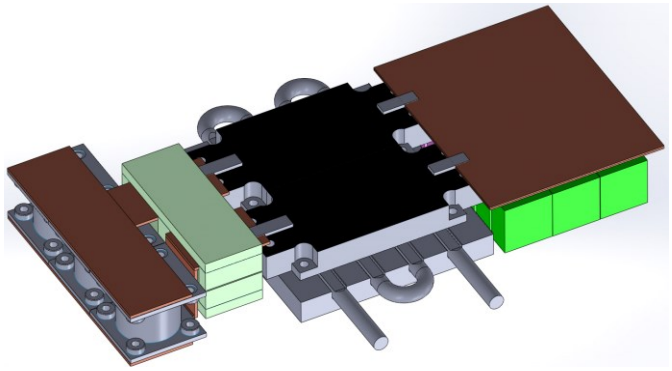
(b) Simulated switch voltage and current to show ZCS



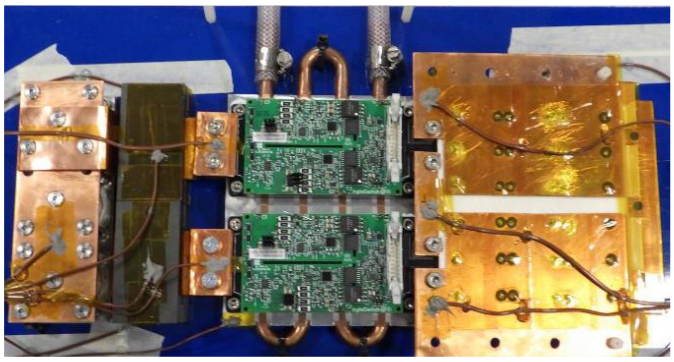
(c) Simulated resonant, input and output capacitor voltage and current waveforms

Fig. 8: Simulation results of one-cell STC at ZCS operation

A prototype has been built as shown in Fig. 9. Fig. 9(a) shows the 3-D layout model designed in Solidworks. The resonant tank is on the left-hand side, which is composed of three polypropylene film resonant capacitors, one soft-ferrite core inductor with one-turn copper foil winding. The SiC power module is mounted on a water-cooling heatsink. The right-hand side presents the DC capacitors and the 2-layer DC busbar, which includes V_{in}, V_o and ground DC busbars. An assembled 100 kW prototype is shown in Fig. 9(b). The power density has been measured as around 42 kW/L.



(a) 3-D prototype model built in Solidworks



(b) Assembled 100 kW prototype

Fig. 9: 3-D and assembled real prototypes

IV. Conclusion and Future Work

This paper utilizes a resonant switched capacitor based one-cell switched tank converter in a 300 V – 600 V 100 kW variable voltage converter for the electric vehicle applications. The topology has been proved to be more efficient and compact compared with boost converter and three-level flying capacitor multilevel converter. A new index called total semiconductor loss index has been proposed to evaluate topologies and device technologies at customized output power and switching frequency. The one-cell STC can achieve lower device power loss with the same die area usage compared with boost converter. In other words, the one-cell STC utilizes smaller die area with lower device manufacturing costs at the same device power loss. The theoretical efficiency and power loss breakdown analysis has been conducted. The simulation results

at the ZCS operation are presented. The estimated efficiency is about 99.2% at 30 kW, 99.13% at half load, and 98.64% at full load. Both the 3-D and real protypes have been presented, which shows a power density of around 42 kW/L. More design details and test results will be presented in future publications.

ACKNOWLEDGMENT

This work is supported by the Ford Motor Company and NSF Award Number 1810428. The engineering sample support from Rohm and Hitachi is appreciated.

REFERENCES

[1] W. Qian and H. Cha et al., "55-kW variable 3X DC-DC converter for plug-in hybrid electric vehicles," *IEEE Trans. Power Electron.*, vol. 27, no. 4, pp. 1668–1678, Apr. 2012.

[2] T. Kim and S. Baek, "A direct DC bus voltage regulation of the variable voltage converter in the electric traction drive system," in *2017 IEEE Transportation and Electrification Conference and Expo, ITEC 2017*, 2017, pp. 732–736.

[3] L. Chen, "A variable voltage converter with direct bypass for traction drive inverters," in *2013 IEEE Energy Conversion Congress and Exposition, ECCE 2013*, 2013, pp. 2793–2798.

[4] J. Elmes, "High-Density and High-Efficiency Soft Switching Modular Bi-Directional DC-DC Converter for Hybrid Electric Vehicles," Ph.D Thesis, University of Central Florida, 2010.

[5] L. Chen, L. Xu, N. Narayanachar, and S. Zarei, "Development of a drive cycle based evaluation method for Variable Voltage Converter in vehicle electrification applications," in *2011 IEEE Energy Conversion Congress and Exposition*, 2011, pp. 254–259.

[6] L. Chen, "Variable Voltage Converter with Direct Output Voltage Clamping," US 2012/0019231 A1, 2012.

[7] U.S. Department of Energy, "Electrical and Electronics Technical Team Roadmap," *U.S. DRIVE Partnership*, 2017. [Online]. Available: https://www.energy.gov/sites/prod/files/2017/11/f39/EETT Roadmap 10-27-17.pdf.

[8] X. Jia and D. Xu et al., "A High Power Density and Efficiency Bi-Directional DC / DC Converter for Electric Vehicles," in *ECCE Asia, Seoul*, 2015, pp. 874–880.

[9] J. Scoltock, G. Calderon-lopez, and A. J. Forsyth, "Topology and Magnetics Optimisation for a 100-kW Bi-Directional DC-DC Converter," in *2017 IEEE Vehicle Power and Propulsion Conference (VPPC)*, 2017, pp. 1–6.

[10] J. Zhang, J. S. Lai, R. Y. Kim, and W. Yu, "High-power density design of a soft-switching high-power bidirectional dc-dc converter," *IEEE Trans. Power Electron.*, vol. 22, no. 4, pp. 1145–1153, Jul. 2007.

[11] D. Christen, S. Tschannen, and J. Biela, "Highly efficient and compact DC-DC converter for ultra-fast charging of electric vehicles," in *2012 15th International Power Electronics and Motion Control Conference (EPE/PEMC)*, 2012, p. LS5d.3-1 to 3-8.

[12] W. Qian, J. G. Cintrón-Rivera, F. Z. Peng, and D. Cao, "A multilevel DC-DC converter with high voltage gain and reduced component rating and count," in *Conference Proceedings - IEEE Applied Power Electronics Conference and Exposition - APEC*, 2011, pp. 1146–1152.

[13] C. Schaef, J. S. Rentmeister, and J. Stauth, "Multimode Operation of Resonant and Hybrid Switched-Capacitor Topologies," *IEEE Trans. Power Electron.*, pp. 1–1, 2018.

[14] Y. Lei, W.-C. Liu, and R. C. N. Pilawa-Podgurski, "An Analytical Method to Evaluate and Design Hybrid Switched-Capacitor and Multilevel Converters," *IEEE Trans. Power Electron.*, vol. 33, no. 3, pp. 1–1, Mar. 2017.

[15] M. Vasic, D. Serrano, P. Alou, J. A. Oliver, P. Grbovic, and J. A. Cobos, "Comparative analysis of two compact and highly efficient resonant switched capacitor converters," in *Conference Proceedings - IEEE Applied Power Electronics Conference and Exposition - APEC*, 2018, vol. 2018–March, pp. 2168–2174.

[16] J. Itoh, K. Matsuura, and K. Orikawa, "Reduction of a boost inductance using a switched capacitor DC-DC converter," in *8th International Conference on Power Electronics - ECCE Asia*, 2011, pp. 1315–1322.

[17] T. Zhao, J. Wang, A. Q. Huang, and A. Agarwal, "Comparisons of SiC MOSFET and Si IGBT Based Motor Drive Systems," *2007 IEEE Ind. Appl. Annu. Meet.*, pp. 331–335, 2007.

[18] C. Sintamarean, F. Blaabjerg, and H. Wang, "Comprehensive evaluation on efficiency and thermal loading of associated Si and SiC based PV inverter applications," *IECON Proc. (Industrial Electron. Conf.*, pp. 555–560, 2013.

[19] S. Pettersson, S. Kicin, E. Bianda, T. Holm, P. Raisanen, and F. Canales, "Performance evaluation of custom-made 1.2-kV 100-A silicon carbide half-bridge module in three-phase grid connected PWM rectifier," *2015 IEEE Energy Convers. Congr. Expo. ECCE 2015*, pp. 4138–4144, 2015.

[20] A. Elasser and T. P. Chow, "Silicon carbide benefits and advantages for power electronics circuits and systems," *Proc. IEEE*, vol. 90, no. 6, pp. 969–986, 2002.

[21] G. Calderon-Lopez and A. J. Forsyth, "High Power Density DC-DC Converter with SiC MOSFETs for Electric Vehicles," in *IET PEMD*, 2014, p. 1.4.01--1.4.01.

[22] S. Jiang, S. Saggini, and C. Nan et al., "Switched tank converters," *IEEE Trans. Power Electron.*, vol. Sept, pp. 1–1, 2018.

[23] M. Shoyama, F. Deriha, and T. Ninomiya, "Resonant boost switched capacitor converter with high efficiency," in *30th Annual Conference of IEEE Industrial Electronics Society, 2004. IECON 2004*, 2004, vol. 1, pp. 222–226.

[24] K. Sano and H. Fujita, "Performance of a high-efficiency switched-capacitor-based resonant converter with phase-shift control," *IEEE Trans. Power Electron.*, vol. 26, no. 2, pp. 344–354, Feb. 2011.

[25] Y. Li, B. Curuvija, X. Lyu, and D. Cao, "Multilevel modular switched-capacitor resonant converter with voltage regulation," in *Conference Proceedings - IEEE Applied Power Electronics Conference and Exposition - APEC*, 2017, pp. 88–93.

[26] B. J. Baliga, "Power MOSFETs," in *Fundamentals of Power Semiconductor Devices*, 1st ed., Springer US, 2008, pp. 279–506.

[27] M. Shen, A. Joseph, J. Wang, F. Z. Peng, and D. J. Adams, "Comparison of traditional inverters and Z-source inverter for fuel cell vehicles," in *Power Electronics in Transportation (IEEE Cat. No.04TH8756), Novi, MI, USA*, 2004, pp. 125–132.

[28] T. Friedli, M. Hartmann, and J. W. Kolar, "The Essence of Three-Phase PFC Rectifier Systems -- Part II," *IEEE Trans. Power Electron.*, vol. 29, no. 2, pp. 543–560, Feb. 2014.

[29] B. Hauke, "Basic Calculation of a Boost Converter's Power Stage (Rev. C)," *Texas Instruments Application Report*, 2014. [Online]. Available: http://www.ti.com/lit/an/slva372c/slva372c.pdf.