Development of a 100 kW SiC Switched Tank Converter for Automotive Applications

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***Abstract*—A 300 V to 600 V 100 kW SiC MOSFET based one-cell switched tank converter (STC) is developed as a bidirectional dc-dc power transfer stage between the vehicle battery and the DC-link side of the vehicle dc-ac inverter. A continuous half-load 50 kW and short-period full-load 100 kW operation is targeted. Working principles of the proposed topology are analyzed. Design of the key components such as SiC MOSFET power modules, AC resonant capacitor and inductor is presented. A 100 kW prototype has been assembled and tested. An energy-efficient test platform is designed. The power density of the main power processing part is around 41.7 kW/L. The tested peak and full-load efficiencies are about 98.7% and 97.35%, respectively. The thermal performance has also been evaluated. Both the tested electrical and thermal results are consistent with the theoretical design.**

Keywords—switched tank converter, resonant switched capacitor converter, SiC MOSFET, ZCS (zero current switching)

I. Introduction

The powertrains in electric vehicles and hybrid electric vehicles are equipped with a bidirectional dc-dc converter to interface the battery and the DC-link side of 3-phase inverter in the generator/motor system [1]. In a recent report from U.S. Department of Energy [2], by 2025, the electric traction drive system cost is expected to be lower than $2.7/kW, and the power density is supposed to exceed 100 kW/L based on the 100 kW power level. To achieve this goal, a proper topology with optimized device and passive component design should be deliberated and experimentally verified.

Boost converter [3] and its derivatives such as soft switching boost topology [1], multi-phase interleaved versions [4] and isolated composite boost topology [5] have been studied. A 40 kW boost converter is designed with 6 kW/L power density [3]. However, it suffers from low efficiency and bulky reactive components. A 200 kW frequency-variable, soft-switching boost converter [1] is investigated with 98% peak efficiency and 6 kW/L power density. 3-phase boost topology is applied in a 90 kW bidirectional 320 V to 600 V dc-dc converter in hybrid electric vehicles [4]. However, the power density is only 2.7 kW/L and no efficiency is provided. Isolated composite boost topology is applied in a 30 kW 200 V to 650 V converter with 98.7% peak efficiency [5]. But both the inductor and transformer sizes are not optimized. Another group is flying capacitor multilevel converter [6]. A 30 kW converter with 8.612 kW/L power density and 97% efficiency is shown in [6]. However, it is difficult to realize a compact design considering the separate locations of the DC-side resonant inductor and AC-side resonant capacitor.

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Recently, due to their high efficiency, high power density and modularity, resonant switched capacitor converters have been widely investigated [7]–[9]. Besides, SiC MOSFET power modules achieve better performance compared with Si counterparts, especially in high-frequency, high-temperature and high-power operations [10]. A boost based 60 kW dc-dc converter applies Cree 1200 V 100 A SiC MOSFET power modules to realize 20 kW/L power density [10]. But the overall efficiency is sacrificed by hard-switching operation.

By combining the advantages of SiC MOSFET power modules and STC, this paper develops a 100 kW 300 V to 600 V ZCS STC for electric vehicle and hybrid electric vehicle applications. The operation principles, design of the key components, assembled prototype, tested electrical and thermal results will be presented in the following parts.

II. Design of 100 kW One-Cell SiC STC

Fig. 1 shows a one-cell STC topology. Two switches S_1 and S_2 are connected in series to interface the input and output voltages. The other pair of switches S_3 and S_4 forms another half bridge linking the low-voltage input side to the ground. The resonant tank is composed of a resonant inductor L_R and resonant capacitor C_R. The DC bias of C_R equals to V_{in}. While the DC bias of L_R is 0 due to inductor voltage-second balance. Thus, the DC bias of the whole resonant tank is V_{in}. As a result, the output voltage can be 2 times V_{in}. Clamping capacitors C_1 and C_{in} are used to clamp the drain-source voltage of each switch.

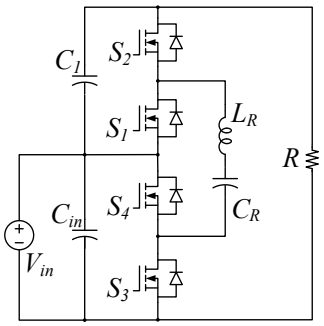
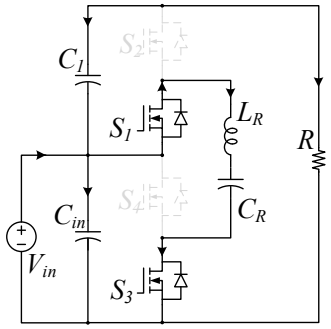


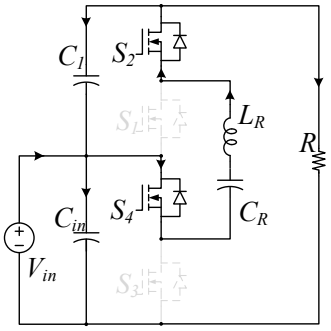
Fig. 1: Proposed one-cell STC topology

The two equivalent circuits are presented in Fig. 2(a) and (b), respectively. In Fig. 2(a), when S_1 and S_3 are ON, the resonant capacitor C_R is charged and resonant inductor L_R stores energy. The current I_{C1} flowing through the C_1 capacitor has the same amplitude with load current I_o. C_1 keeps releasing its energy to the load. While the current I_{Cin} of the input capacitor C_{in} is negative to the reference direction. C_{in} releases the energy most of the time. In Fig. 2(b), when S_2 and S_4 are ON, the resonant capacitor C_R

discharges together with the input voltage source. The resonant inductor L_R releases energy. The resonant inductor current has the same waveform with the switch current flowing through S_2 and S_4. C_1 stores its energy most of the time. C_{in} keeps storing energy. The voltage V_{CR} of the resonant capacitor C_R is a DC voltage with a DC bias equal to V_{in}. A voltage doubler is achieved by applying this simple control into the proposed topology.



(a): Equivalent circuit 1



(b): Equivalent circuit 2

Fig. 2: Two equivalent circuits for the one-cell STC

A. Design of Devices

Among the investigated devices with different voltage ratings, 900 V Cree and 650 V Rohm SiC MOSFET achieve relatively lower power loss. However, the 900 V Cree SiC MOSFET power module is not available during the design period. The current capability of 650 V Rohm SiC MOSFETs are limited. Thus, multiple paralleled devices with TO-247 package are needed, which increases total device volume and induces current imbalance issues [11]. Therefore, Rohm and Cree 1200 V SiC MOSFET modules with comparatively higher current capabilities are studied.

Fig. 3 shows the total SiC MOSFET power loss of five 1200 V SiC MOSFET power modules at different output power ratings with 100 kHz switching frequency. With maximum 100 kW output power, 300 V input, 600 V output, the lowest MOSFET power loss at full power is achieved by Rohm 1200 V 600 A SiC modules.

Higher switching frequency decreases the magnetic component size, but introduces more AC loss. Considering this trade-off and the maximum frequency capability of selected AgileSwitch® EDEM3-EconoDual gate drive boards, 100 kHz switching frequency has been designed.

B. Design of Resonant Capacitor

Both ceramic and film capacitors could be used in the high-frequency and high RMS current applications. The multi-layer ceramic capacitors (MLCC) have higher power

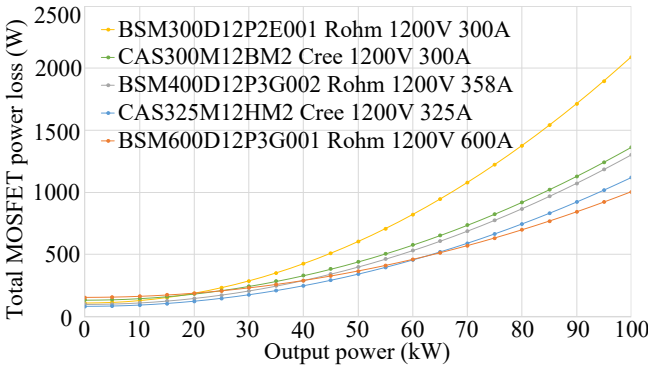


Fig. 3: Total MOSFET power loss comparison among different MOSFETs

density compared to film capacitors. However, because ceramics tend to be weak in tension, a crack is relatively easily formed when excessive board flex is put on the soldered MLCC [12]. So, an electrical conduction between the two electrodes would occur, which further progresses towards a short circuit. Therefore, due to these reliability concerns, MLCCs are not preferred for the automotive power electronic applications. As a result, the film capacitors with good current capability are considered.

Based on a summarization of high power resonant capacitors from different companies [13], the polypropylene film capacitors of Illinois Capacitor® provides specifically designed high-current, high-frequency resonant capacitors. So, all the high-density resonant capacitors from this company are studied, including LC1 ~ LC6, HC1 ~ HC6 and HC3A, HC3B series. In each category, one type with highest capacitance density, satisfying frequency range, full-load peak voltage and current requirements is selected. Fig. 4 shows the capacitance density comparison, from which LC2 and LC3 series achieve higher capacitance density.

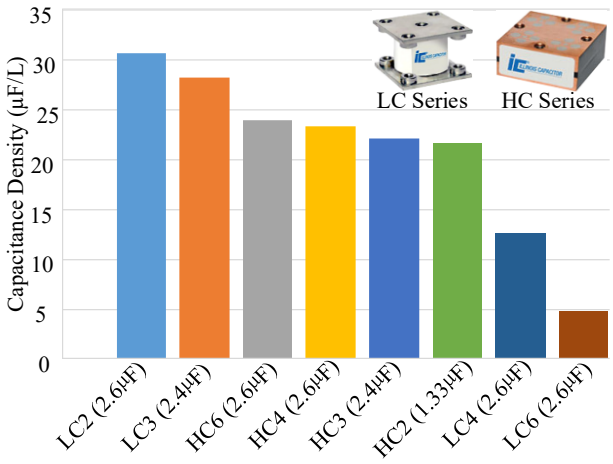
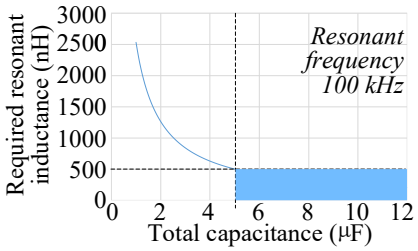


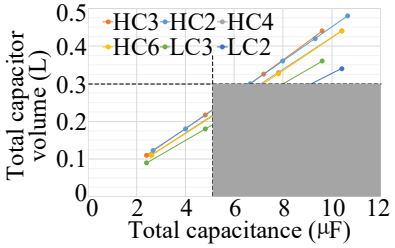
Fig. 4: Capacitance density per unit volume comparison

The volume of the whole resonant tank then needs to be further examined. So, smaller inductance is preferred. Fig. 5(a) shows the relationship between the required inductance and total resonant capacitance. With the practical size as well as the design of core and winding considered, 500 nH maximum inductance is designed. Correspondingly, the minimum resonant capacitance is 5.066 μF. Considering the power module and heatsink layout, the total capacitor volume is designed below 0.3 L. Fig. 5(b) shows the trade-off between the total capacitance and the capacitor volume. The remaining candidates in the shaded area are compared in

Table I, from which three 2.4 µF LC2 and three 2.6 µF LC3 are preferable due to smaller required inductance.



(a): Required resonant inductance versus total capacitance



(b): Total capacitor volume versus total capacitance

Fig. 5: Capacitor evaluation based on required inductance and total volume

TABLE I: COMPARISON AMONG PROSPECTIVE CAPACITORS

Series	Total capacitance (µF)	Total volume (L)	RMS voltage (V)	RMS voltage capability at 100kHz (V)	Required inductance at 100kHz (nH)
HC2	5.32	0.24	319.79	500	476.13
HC4	5.2	0.22	320.69	500	487.12
HC6	5.2	0.22	320.69	600	487.12
LC3	7.2	0.27	310.96	410	351.81
LC2	5.2	0.17	320.69	350	487.12
LC2	7.8	0.26	309.36	350	324.75

Nevertheless, the polypropylene film capacitor voltage rating drops at higher switching frequency, because of the heat generated by high frequency AC loss [14]. Thus, a safe margin is required between the full-load peak voltage and maximum voltage capability after 100 kHz derating. Fig. 6 shows voltage derating with the resonant frequency of selected film capacitors. The margins between the full-load voltage peak and the maximum voltage capability for the LC2 and LC3 series are about 41 V and 100 V, respectively. Therefore, three 2.4 µF LC3 capacitors are finalized.

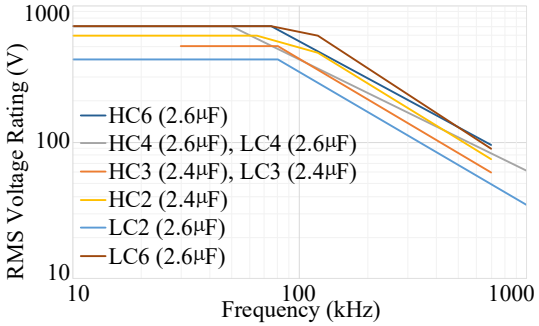


Fig. 6: Voltage derating curves for HC and LC series capacitors

C. Design of Resonant Inductor

With above 7.2 µF resonant capacitance and 100 kHz resonant frequency design, the resonant inductance is 351.81 nH. The winding, core designs are described below.

1) Winding Design

One-turn winding is designed to keep the AC inductor in the similar height with AC capacitors, power module, heatsink, and DC side so that the space is fully used. Multi-layer copper foil AC busbar is utilized for this high-current high-frequency winding. By distributing current through multiple layers, this arrangement reduces AC loss caused by skin effect. Skin depth δ is calculated in Eq. (1) [15][16].

$$\delta = \sqrt{\rho/(\pi f \mu)} \tag{1}$$

Where, f is the AC frequency. The copper resistivity ρ and permeability μ are 1.76×10^{-8} Ω·m, 1.257×10^{-6} H/m, respectively. At 100 kHz, the skin depth for copper is calculated as 0.211 mm. So, the copper foil not thicker than 0.211 mm is selected. To further design the copper cross-section area and number of layers, the current density is evaluated. For the one-turn winding design, current density is recommended as 5.167 A/mm^2 to avoid excessive temperature rise [17]. Because AC RMS current value is 370.24 A and the cross-section area of selected one-layer copper foil is 7.112 mm^2, total number of layers is (370.24/5.167)/(7.112)≈10. Thus, 10-layer copper foil is applied. The total cross-section area of AC busbar A_{AC_Busbar} is 71.12 mm^2. Its assembly is shown in Fig. 7.

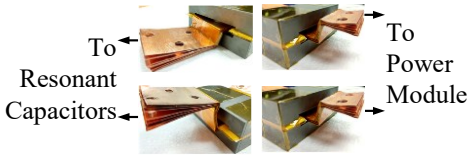


Fig. 7: AC busbar assembly

2) Core Design

To select an appropriate core, a small core loss density is preferred. Powder and ferrite cores from major magnetic manufacturers are investigated. The core loss density equation of CSC cores and Hitachi soft ferrite cores is in Eq. (2) [18][19]. For Hitachi HLM50 amorphous powder core, Magnetics powder, ferrite cores, it is in Eq. (3) [20]–[22].

$$P_V = (K_h \cdot f + K_e \cdot f^{\lambda}) \cdot (B_{PK})^Y \tag{2}$$

$$P_V = a \cdot (B_{PK})^b \cdot (f)^c \tag{3}$$

Where, P_V is core loss density (kW/m^3). f is the frequency (kHz). K_h is the hysteresis loss efficient. K_e is the eddy current loss efficient. Y is an exponent close to 2.

Fig. 8 shows the core loss density comparison at 100 kHz. Hitachi soft ferrite core ML29D is finalized because of smaller core loss density in the 0.1 ~ 1 T flux density range.

E-shaped cores are targeted owing to simpler assembly and more cost-effective solutions compared with pot cores [23]. Fig. 9 shows a typical E-core dimension. Due to the length constraints of the heatsink and SiC module, α_2 is fixed as 152.4 mm. Constrained by the prototype height, β_2 is 15 mm. From a planar E core reference design [15][24], the core height β_2 is the sum of β_1 and α_1.

To achieve desired inductance, core cross-section area A_e and air gap length l_g are restricted by Eq. (4) [25].

$$L = \left(N^2 \cdot A_e\right) / \left[\left(l_g/\mu_0\right) + \left(l_e/\mu_c\right)\right] \tag{4}$$

Where, N is number of turns. μ_0, μ_c are permeability of the free space and core, respectively. l_g is air gap length. l_e is

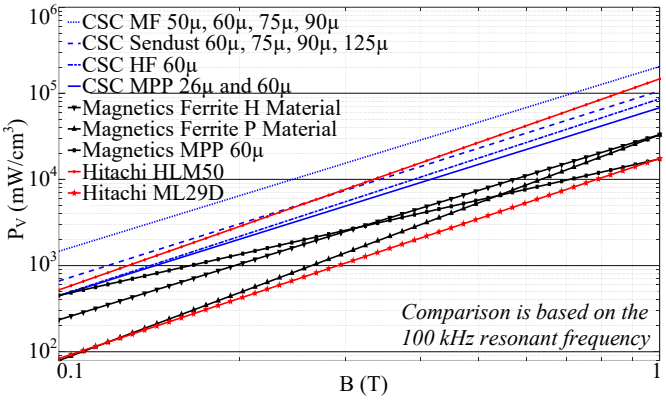


Fig. 8: Core loss density comparison at 100 kHz frequency

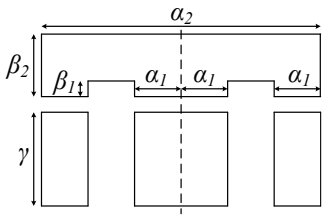


Fig. 9: E core dimensions for the resonant inductor core shape design

the equivalent magnetic path length as shown in Eq. (5) [26].

$$l_e = 2\left(\alpha_2/2 - 2\alpha_1 + 2\beta_1 + l_g\right) + \pi\cdot\alpha_1 \quad (5)$$

Due to winding insulation requirement, the window utilization factor K_u should be less than 0.65 for low voltage foil inductor design [27], as shown in Eq. (6).

$$K_u = A_{AC\_Bus}/A_{window} = 71.12mm^2/A_{window} \le 65\% \quad (6)$$

Based on the core geometry in Fig. 9, the window area A_{window} equals to $2\beta_1\cdot(\alpha_2/2\text{-}2\alpha_1)$. Thus, a constraint for α_1 is derived: $\alpha_1 \le 13.87$ mm. In this project, 13 mm is applied. The magnetics path length l_e can be further calculated once α_1 is fixed. The calculated l_e is 149.24 mm from Eq. (5).

To further determine the core width γ and corresponding core cross-section area A_e, a trade-off between core temperature rise and core volume is made. From Faraday's law, the flux density swing ΔB is derived in Eq. (7).

$$\Delta B = \left|\left[\int_{T_s/4}^{3\cdot T_s/4} L di_L(t)\right]\Big/\left(N\cdot A_e\right)\right| = \left(L\cdot 2I_o\cdot\pi\right)/\left(N\cdot A_e\right) \quad (7)$$

For the AC flux swing in our case, peak flux density B_{PK} is half the flux density swing ΔB [21], as shown in Eq. (8).

$$B_{PK} = \Delta B/2 = \left(L\cdot P_o\cdot\pi\right)/\left(N\cdot A_e\cdot 2V_{in}\right) \quad (8)$$

By combining Eq. (2) and (8) and considering $A_e = 2\alpha_1\cdot\gamma$, the core loss density P_V is derived in Eq. (9). Core volume V is in Eq. (10). Core power loss $P_{core} = P_V\cdot V$. The core temperature rise ΔT_{core} is estimated by Eq. (11) [28].

$$P_V = \left(K_h\cdot f + K_e\cdot f^{\lambda}\right)\cdot\left[\left(L\cdot P_o\cdot\pi\right)/\left(4N\cdot\alpha_1\cdot\gamma\cdot V_{in}\right)\right]^X \quad (9)$$

$$V = 4\cdot\alpha_1\cdot\left(\beta_2 - \alpha_1\right)\cdot\gamma + \alpha_1\cdot\alpha_2\cdot\gamma \quad (10)$$

$$\Delta T_{core} = \left(P_{core}/A_{surface}\right)^{0.833} \quad (11)$$

Based on above analysis, core temperature rise versus core width is plotted in Fig. 10, together with the core volume. Two constraints are considered in the core width design. The core temperature rise is limited below 100 °C to avoid external core cooling. The core volume is designed to be smaller than 0.1 L, considering the dimensions of resonant

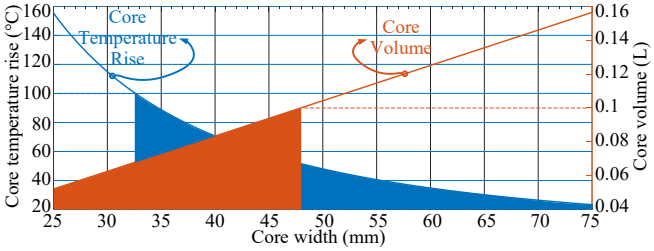


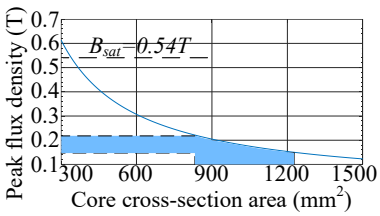
Fig. 10: Core temperature rise and core volume trade-off

capacitors, heatsink and SiC power modules. Hence, a design range can be obtained based on this trade-off. The core width γ range from 32.5 to 48 mm is derived. So, core cross-section area A_e ranges from 845 to 1248 mm^2.

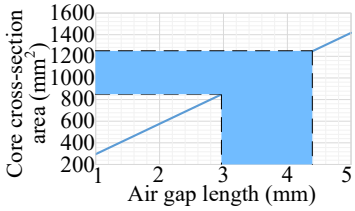
Fig. 11(a) shows the 0.1476 ~ 0.218 T peak flux density range according to Eq. (8). Considering 0.54 T saturation magnetic flux density B_{sat} for ML29D core [29], designed flux density range is below half the saturated flux density.

Fig. 11(b) illustrates the relationship between A_e and l_g based on Eq. (12) and the inductance calculated in Eq. (4). A design range for the air gap length l_g is further derived, ranging from 2.967 to 4.407 mm.

$$A_e = L\cdot\left(l_g/\mu_0 + l_e/\mu_c\right) \quad (12)$$



(a): Relationship between peak flux density and core cross-section area



(b): Relationship between core cross-section area and air gap length

Fig. 11: The plots of (a) peak flux density B_{PK} vs. core cross-section area A_e. (b) core cross-section area A_e vs. air gap length l_g

Considering the above core temperature rise and volume trade-off, a core width of 40 mm is finalized. Therefore, the core cross-section area is calculated as 1040 mm^2. The peak flux density and air gap length are finalized as 0.1771 T and 3.664 mm, respectively. With this designed core shape, the core temperature rise is about 70 °C at 100 kW.

III. Assembled Prototype and Tested Results

Fig. 12 shows the assembled 100 kW prototype. It is mainly composed of four parts. The first part is the control board, gate drive board and interface board. The control is realized through the TI® TMS320F28335 Delfino microcontroller and Xilinx® FPGA Spartan-6 XC6SLX9 IC. The second part is the water-cooling heatsink and SiC power modules. The third part is the AC resonant side including two sets of 10-layer AC copper foil busbars, the resonant capacitors, and resonant inductor core. The fourth part is the two-layer DC busbar including V_{in}, V_o and GND busbars.

The DC busbars are soldered together with the DC capacitors by using a 500 W high-power soldering iron considering that the leaded film capacitors are not suitable for the reflow soldering [30].

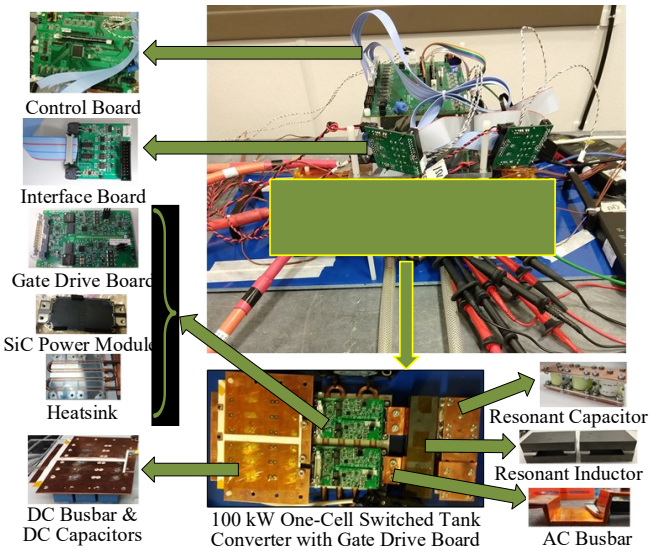


Fig. 12: The designed and assembled 100 kW one-cell STC

The length, width and height of the dc-dc converter itself are 37.8 cm, 15.1 cm and 4.2 cm, respectively. So, the main power processing part volume is about 2.4 L, and the power density is 41.714 kW/L.

The schematic of the test platform is shown in Fig. 13. The power is circulated in a 3-phase motor-generator system. The DC power supply is aimed to compensate the power loss, most of which is consumed by the motors and generators. Therefore, the efficiency is much higher and overall thermal performance is better for this test platform compared to the platform with a high-current resistive load.

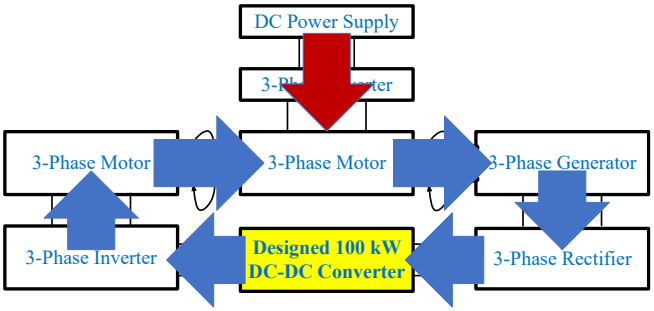
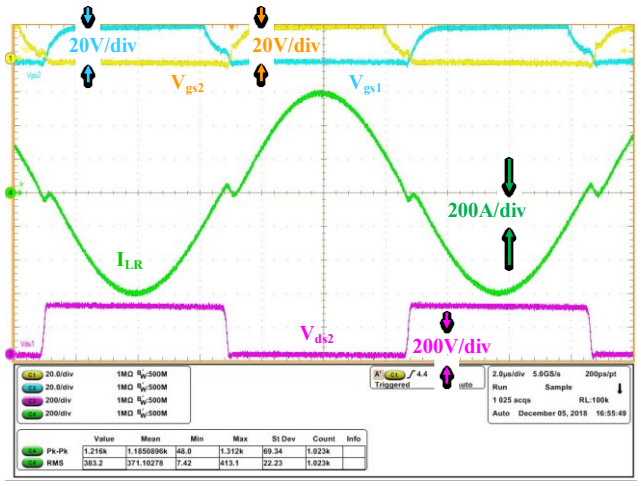


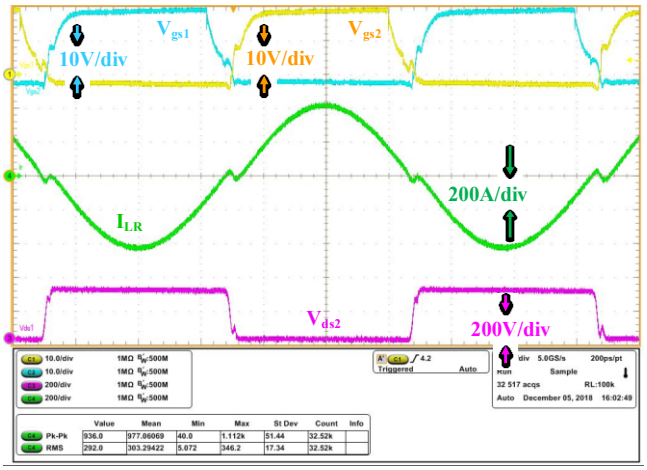
Fig. 13: The test platform schematic

In the test, the switching frequency is fine-tuned around 84.9 kHz which includes the 300 ns deadtime. Actual design resonant frequency is higher than switching frequency and the ZCS for all switches is achieved. Fig. 14(a) shows the test results at 100 kW with 300 V input and 600 V output. The top two waveforms are the gate-source voltage of S_1 and S_2. The green waveform is the resonant current with the tested RMS current around 383.2 A. The theoretical RMS current value is 370.24 A, which matches the tested result well. The bottom trace is the drain-source voltage of S_2.

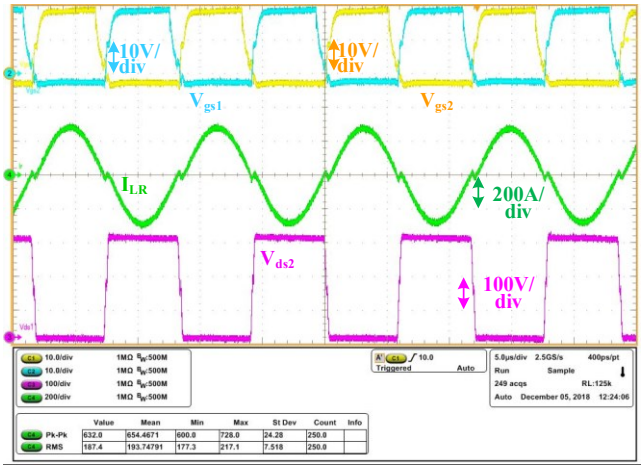
The tested waveforms at 80 kW, 50 kW are presented in Fig. 14(b) and (c), respectively. From the tested current waveforms, the resonant current RMS values at 80 kW, 50 kW are 292 A and 187.4 A, respectively, which also match the theoretical calculated values.



(a): Tested waveforms at 100 kW



(b): Tested waveforms at 80 kW



(c): Tested waveforms at 50 kW

Fig. 14: Test results at (a) 100 kW, (b) 80 kW, and (c) 50 kW

The tested gate-source voltage V_{gs} waveforms of the four SiC MOSFET switches are presented in Fig. 15. The gate drive output high and low voltages are +18 V and −3 V, respectively. The drain-source voltage V_{ds} waveforms are measured at about 300 V input and around 600 V output, as shown in Fig. 16. From the figure, each switch voltage stress is equal to the input voltage.

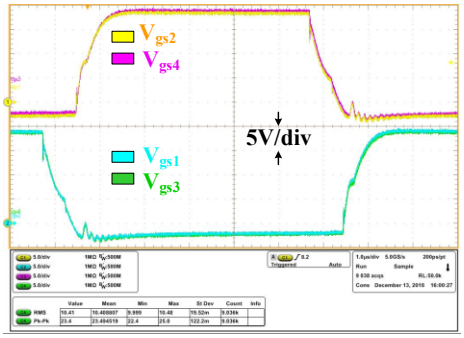


Fig. 15: Gate-source voltage waveforms measured at gate and source pins

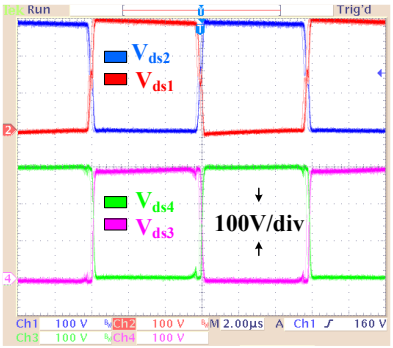


Fig. 16: Drain-source voltage waveforms measured at drain and source pins

All the voltages $V_{gs1} \sim V_{gs4}$, $V_{ds1} \sim V_{ds4}$ are measured directly from the SiC power module pins in Fig. 17(a). It also shows that the resonant current I_{LR} is measured through the middle point of the half bridge. Fig. 17(b) presents the applied Rohm 1200 V 600 A SiC module circuit diagram, which defines each pin and clarifies the measurement.

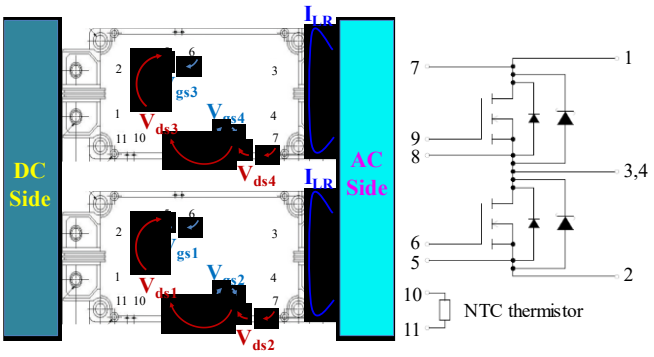


Fig. 17: (a) Voltage, current measurement. (b) SiC module circuit diagram

Fig. 18 illustrates the detailed tested thermal performance at 50 kW continuous operation. It is based on the measurement from thermal couples. According to Fig. 18, AC busbar and the V_{in} DC busbar experience the highest temperature, which are 56.5 °C and 59 °C, respectively. At 50 kW steady state, the heatsink temperature is constant and close to the room temperature 25 °C, which justifies the design of the water cooling heatsink. The inductor core temperature comes to stable at around 42.5 °C. Thus, the resonant inductor core temperature rise is 17.5 °C. The two DC capacitors C_1 and C_{in} show temperature of 37 °C and 24 °C, respectively. Thus, the maximum temperature rise for the DC capacitor is about 12 °C. Finally, the stabilized V_o and GND DC busbars stay at the 46 °C and 54 °C, respectively.

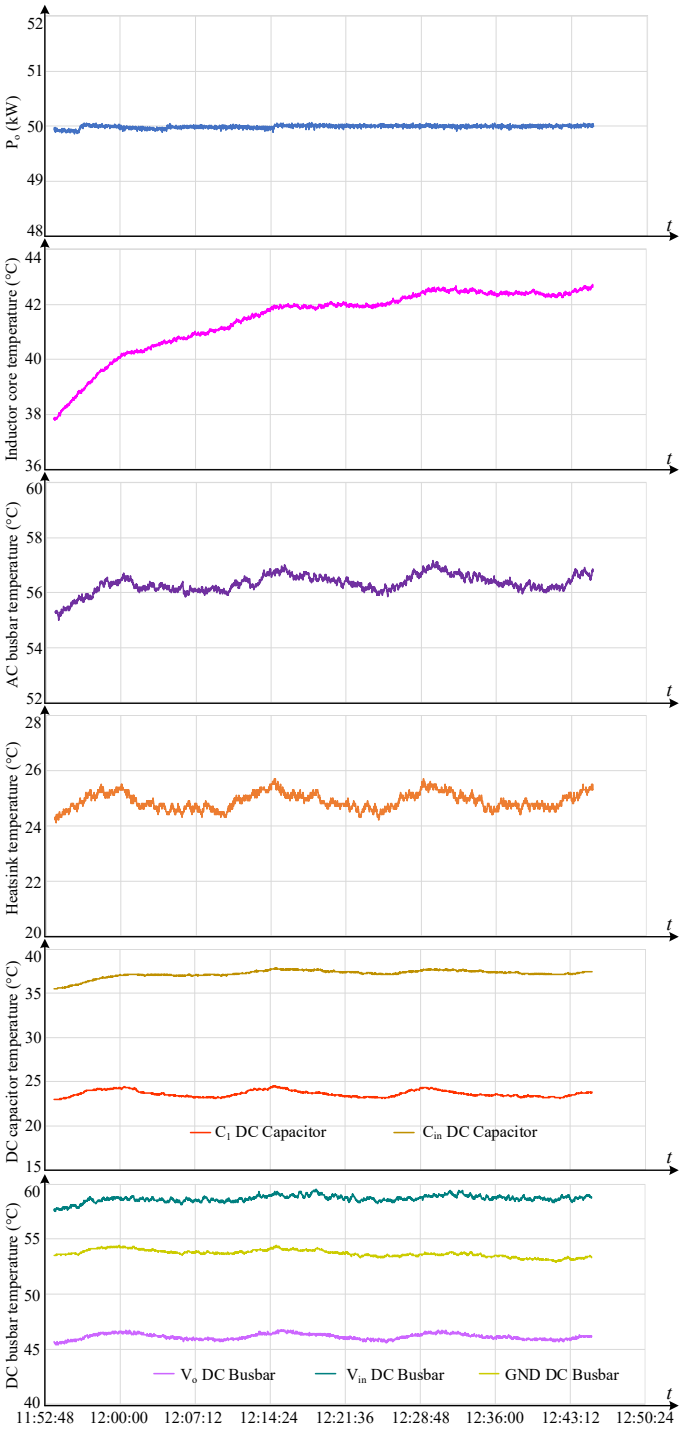


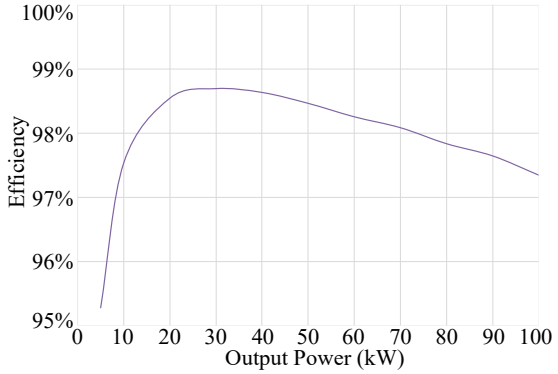
Fig. 18: Tested thermal performance at 50 kW continuous operation

From the above thermal analysis, high DC busbar and AC busbar power losses are indicated, which could be optimized by future finite element analysis. More theoretical thermal calculation and the consistency with these tested thermal results will be presented in future publications.

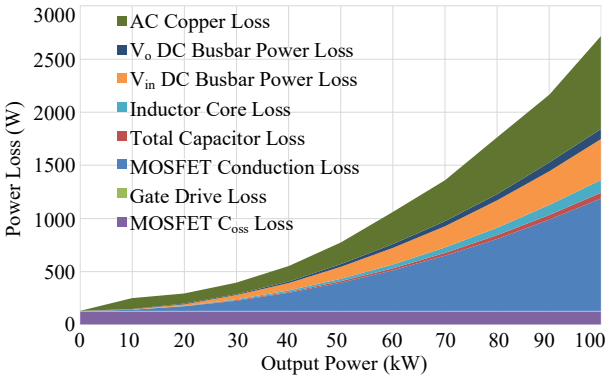
Fig. 19(a) presents the tested efficiency based on the measured voltage, current and power data from Yokogawa® WT1800 power analyzer. The tested peak efficiency reaches to about 98.7% at around 30 kW. The tested 100 kW and 50 kW efficiency is about 97.35% and 98.47%, respectively.

Fig. 19(b) illustrates the power loss breakdown conducted with different output power. From the figure, the MOSFET conduction loss is a major contribution at full load.

Because the on-resistance increases with the junction temperature and the device current RMS increases with the deadtime, the estimated conduction loss is higher than ideal case. Besides, the V_{in} DC busbar loss and AC copper loss are significant in the total power loss. The V_{in} and V_o DC busbar power losses are calculated based on the measured voltage drops between two ends on the V_{in} DC busbar and V_o DC busbar, respectively.



(a): Tested efficiency versus the output power



(b): Tested power loss breakdown versus output power

Fig. 19: (a) Tested efficiency. (b) Tested power loss breakdown

IV. Conclusion and Future Work

This paper has presented the design and development of a 300 V to 600 V, 100 kW SiC MOSFET based dc-dc one-cell switched tank converter for the automotive applications. The operation principles have been analyzed. The SiC MOSFET power module with optimized power loss and high current capability has been selected. A compact resonant tank with one single-turn soft-ferrite-core inductor and three low-volume high-current high-frequency polypropylene film capacitors has been designed. A complete prototype has been assembled and tested in an optimally designed test platform. From the experimental results, the gate-source and drain-source voltages, resonant currents are consistent with the theoretical analysis. Besides, the thermal performance at 50 kW continuous operation has been verified. The assembled prototype main power circuit power density is about 41.7 kW/L. The tested peak efficiency is around 98.7% at 30 kW. The tested 50 kW and 100 kW efficiency is about 98.47% and 97.35%, respectively. Further power density and efficiency improvement could be done in the following areas. A more energy-efficient power module with 900 V voltage rating is helpful to further decrease the device power loss. What should be noted is that the future design could utilize the high-current Litz wire to replace the AC copper busbars, which would make the optimized multi-turn winding scheme more practicable to decrease the AC copper loss and increase the power density. The DC and AC busbar design would be optimized by using the finite element analysis and simulation.

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