

On Multiterminal Communication over MIMO Channels with One-bit ADCs at the Receivers

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Abstract—The fundamental limits of communication over multiple-input multiple-output (MIMO) networks are considered when a limited number of one-bit analog to digital converters (ADC) are used at the receiver terminals. Prior works have mainly focused on point-to-point communications, where receiver architectures consisting of a concatenation of an analog processing module, a limited number of one-bit ADCs with non-adaptive thresholds, and a digital processing module are considered. In this work, a new receiver architecture is proposed which utilizes adaptive threshold one-bit ADCs — where the ADC thresholds at each channel-use are dependent on the channel outputs in the previous channel-uses — to mitigate the quantization rate-loss. Coding schemes are proposed for communication over the point-to-point and broadcast channels, and achievable rate regions are derived. In the high SNR regime, it is shown that using the proposed architectures and coding schemes leads to the largest achievable rate regions among all receiver architectures with the same number of one-bit ADCs.

I. INTRODUCTION

Next generation cellular networks will utilize hundreds of antennas at the base station and in excess of ten antennas at the user terminals [1]. A major obstacle in implementation and adoption of massive multiple-input multiple-output (MIMO) systems and millimeter wave (mmWave) technologies is the high energy consumption resulting from the large number of antennas in the transmitter and receiver terminals [2], [3].

In traditional fully digital receivers, each antenna is connected to a distinct high resolution analog to digital converter (ADC). While ADCs are an essential component of wireless communication systems, they are a major source of power consumption [2]. In conventional ADC design, the power consumption of an n_q -bit ADC grows exponentially in n_q [4]. Consequently, the power requirements for n_q one-bit ADCs — which grows linearly in n_q — is significantly less than that of a single n_q -bit ADC. As a result, the use of several one-bit ADCs instead of a single high resolution ADC has been proposed to limit the power consumption at MIMO receiver terminals [5]–[10]. However, the receiver architectures studied in the literature lead to a rate-loss, in the sense that when n_q one-bit ADCs are used, they achieve rates strictly less than n_q bits per channel-use [11].

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There has been a large body of work on characterizing the rate-loss due to low resolution quantization in point-to-point (PtP) MIMO systems [6]–[10]. These works consider a PtP MIMO communication problem, where the receiver is equipped with a limited number of one-bit threshold ADCs. The receiver performs linear analog processing on the received channel output vector and feeds the resulting vector to the one-bit ADCs. The digitized output is stored and blockwise processing is performed to recover the message. In particular, [6] and [8] show that using non-zero thresholds in the ADCs can lead to higher achievable rates.

In a companion paper [11], we studied PtP MIMO communication with n_q one-bit ADCs at the receiver, and proposed a blockwise non-adaptive threshold receiver architecture where the ADC thresholds are fixed over the transmission block. We showed that this architecture, which uses analog delay elements, results in an achievable rate that grows linearly in n_q , the number of ADCs at high SNRs, and achieves the maximum rate for a PtP MIMO system for a given n_q . This is in contrast with prior works, where the increase in capacity is logarithmic in n_q [1], [6]. However, the performance analysis in [11] does not extend naturally to PtP communication in low SNRs and multiterminal communications. In this paper, we consider PtP and multiterminal MIMO communication in the presence of a set of n_q low resolution ADCs at the receiver. While we consider the application of one-bit ADCs, the analysis can be extended in a straightforward manner to the case where a set of b -bit ADCs are used at the receiver, where b is an arbitrary system parameter. We propose a class of adaptive threshold receiver architectures, where the ADC thresholds at each channel-use depend on the channel outputs in the previous channel-uses. The proposed adaptive threshold architecture resembles the class of successive approximation register ADCs [12], and is amiable to analysis for PtP communication in the low SNR regime and multiterminal communications. In addition, in PtP communications, the proposed adaptive threshold architecture achieves the same optimal high SNR rate as the non-adaptive threshold one of [11].

While much of the literature focuses on PtP communication, the use of low resolution ADCs at the receivers in multiterminal communications gives rise to new challenges in interference management and successive decoding schemes.

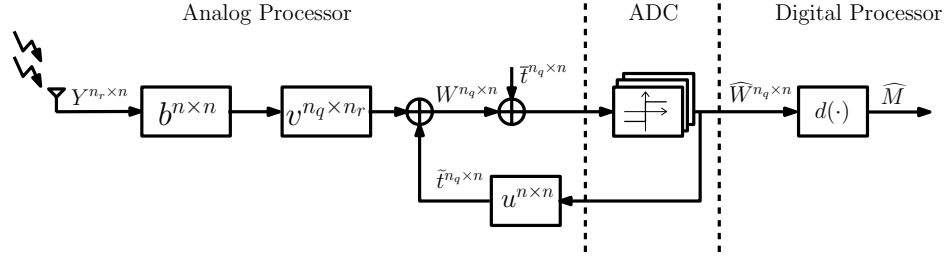


Fig. 1. A PtP-QMIMO system is shown where the linear combiner, temporal processing, and adaptive threshold coefficients are characterized by the matrices $v^{n_q \times n_r}$, $b^{n \times n}$, and $u^{n \times n}$, respectively. Each of the columns of $\tilde{t}^{n_q \times n}$ are equal to the threshold vector t^{n_q} . The ADC module consists of n_q one-bit ADCs.

There have only been few works analyzing efficient and reliable multiterminal receiver architectures and communication strategies in the presence of low resolution ADCs. In [13], communication over the multiple-access channel (MAC) was studied when each transmitter is equipped with a single antenna and the receiver has a single one-bit ADC. It was shown that the optimal input distribution is discrete. Uplink communication over wireless networks modeled as a MAC, was also studied in [14] and practical coding strategies were proposed when coarse quantization is used at the receiver.

Using the adaptive threshold receiver architecture, we propose coding schemes for communication over PtP channels and the broadcast channel (BC), and derive achievable rate or rate regions for arbitrary SNRs. We show that the proposed architecture achieves the optimal rate region in the presence of one-bit ADCs when SNR goes to infinity in all receiver terminals in the sense that the achievable region cannot be expanded by improving the architecture design without the use of additional ADCs. The ideas used in constructing the coding scheme may be used to devise coding strategies for communication over the MAC as well. The MAC achievable region will appear in a longer version of this work.

The rest of the paper is organized as follows: Section II explains the system model. Section III contains the proposed ADC module construction and receiver architectures. In Section IV, we derive achievable regions for various multiterminal communication settings. Section V concludes the paper.

Notation: Sets are denoted by calligraphic letters such as \mathcal{X}, \mathcal{U} . The set of natural numbers and real numbers are denoted by \mathbb{N} and \mathbb{R} , respectively. The set of numbers $\{1, 2, \dots, n\}$, $n \in \mathbb{N}$ is represented by $[n]$. For a given $n \in \mathbb{N}$, the n -length vector (x_1, x_2, \dots, x_n) is written as x^n . The subvector $(x_k, x_{k+1}, \dots, x_n)$ is denoted by x_k^n . We write $\|x^n\|_2$ to denote the L_2 -norm of x^n . An $n \times m$ matrix is written as $h^{n \times m} = [h_{i,j}]_{i \in [n], j \in [m]}$, and I_n is the $n \times n$ identity matrix. The notation $h^m(i)$, $i \in [n]$ is used to represent the i th column of $h^{n \times m}$.

II. SYSTEM MODEL

We first describe the PtP MIMO communication setup when a limited number of one-bit ADCs are available at the receiver which also forms the basis of the BC model. Consider a PtP-MIMO system characterized by $(n_t, n_r, h^{n_r \times n_t})$, where n_t is the number of transmitter antennas, n_r is the number of receiver

antennas, and $h^{n_r \times n_t}$ is the channel gain matrix. The input and output vector pair (X^{n_t}, Y^{n_r}) are related through

$$Y^{n_r} = h^{n_r \times n_t} X^{n_t} + N^{n_r},$$

where N^{n_r} is a vector of independent and identically distributed Gaussian variables with zero mean and unit variance, and the channel input has average power constraint P . The channel gain matrix is assumed to be fixed over the transmission block and is known at the transmitter and receiver. The receiver uses a concatenation of an analog processing module which performs analog signal processing on the received signals, an ADC module consisting of n_q one-bit threshold ADCs to digitize and store the signals, and a digital processing module which performs a digital blockwise decoding operation on the stored bits to recover the message. The communication system is called an $(n_t, n_r, h^{n_r \times n_t}, n_q)$ PtP-QMIMO system.

One-shot Architectures: Prior works have proposed analog processing of the received signals before quantization as a means to mitigate the rate-loss [6]–[10]. In these works, communication is performed in a transmission block of length n . At each channel-use, an analog linear combiner multiplies the channel output vector Y^{n_r} by a spatial analog processing matrix $v^{n_q \times n_r}$ and the output vector is fed to the threshold ADCs, where the threshold vector is denoted by t^{n_q} . The spatial analog processing matrix and threshold vector are assumed to be fixed over the transmission block. The ADC output vector in the i th channel-use is $\hat{W}^{n_q}(i) = Q(v^{n_q \times n_r} Y^{n_r}(i) + t^{n_q})$, $i \in [n]$, where $Y^{n_r}(i)$ is the channel output in that channel-use, and $Q(x^{n_q})$ is the element-wise sign quantization of x^{n_q} . The digital output is stored by the receiver and digital blockwise processing is performed to recover the message. Note that this architecture does not allow for analog temporal processing of the received signals prior to quantization. Consequently, it is called *one-shot* receiver architecture. The one-shot capacity, maximized over all spatial analog processing matrices $v^{n_q \times n_r}$ and threshold vectors t^{n_q} , is denoted by $C_{OS}(h^{n_r \times n_t}, n_q)$.

Adaptive Threshold Architectures: We propose a specific class of adaptive threshold blockwise receiver (AT-Rx) architectures shown in Fig. 1. The matrix $Y^{n_r \times n}$ consists of the received channel output vectors over n channel-uses, where $Y^{n_r}(i)$ is the output in the i th channel-use. The outputs are linearly combined by the temporal analog processing matrix $b^{n \times n}$ and the spatial analog processing matrix $v^{n_q \times n_r}$. These

linear combination operations are implemented using analog linear combiners and delay elements. More precisely, in order to allow for temporal processing, the receiver uses delay elements to store the previously received signals and feeds the stored signals to the analog combiner. The analog combiner produces $v^{n_q \times n_r} Y^{n_r \times n} b^{n \times n}$. As shown in Fig. 1, the ADC thresholds consist of a fixed component and an adaptive component. To elaborate, let $\widehat{W}^{n_q \times n}$ be the matrix of ADC outputs, where $\widehat{W}^{n_q}(i), i \in [n]$ is the vector of ADC outputs after the i th channel-use. The adaptive threshold matrix $\widehat{t}^{n_q \times n}$ is produced by linear processing of $\widehat{W}^{n_q \times n}$ and is equal to $\widehat{W}^{n_q \times n} u^{n \times n}$, where $u^{n \times n}$ is called the adaptive threshold coefficient matrix. The vector $\widehat{t}^{n_q}(i), i \in [n]$ is the adaptive threshold in the i th channel-use. The fixed component of the ADC thresholds is the vector t^{n_q} , and the matrix $\widehat{t}^{n_q \times n}$ consists of n identical copies of t^{n_q} . The adaptive threshold coefficient matrix $u^{n \times n}$ is strictly upper-triangular and the temporal linear combining coefficient matrix $b^{n \times n}$ is an upper-triangular matrix. This ensures that the system can be implemented causally.

We call the architectures described above *adaptive threshold architectures* (AT-Rx). We will provide an example of an adaptive threshold architecture and justify its use in Section III. The AT-Rx architectures are formally defined below.

Definition 1 (AT-Rx). Consider the PtP-QMIMO system characterized by the tuple $(n_t, n_r, h^{n_r \times n_t}, n_q)$. Let $b^{n \times n} \in \mathbb{R}^{n \times n}$ be an upper-triangular matrix, and $u^{n \times n} \in \mathbb{R}^{n \times n}$ be a strictly upper-triangular matrix. A transmission system with adaptive threshold architecture at the receiver (AT-Rx) is characterized by the tuple $(n, \Theta, v^{n_q \times n_r}, t^{n_q}, b^{n \times n}, u^{n \times n})$, the pair of encoding and decoding functions (e, d) are defined in a similar fashion as in PtP-QMIMO systems, where $\widehat{W}^{n_q}(i) = Q(v^{n_q \times n_r} \bar{Y}^{n_r}(i) + \widehat{t}^{n_q}(i) + t^{n_q}), i \in [n]$, $\bar{Y}^{n_r \times n} = Y^{n_r \times n} b^{n \times n}$ is the temporally processed received signal, and $\widehat{t}^{n_q \times n} = \widehat{W}^{n_q \times n} u^{n \times n}$ is the adaptive threshold matrix. The capacity, maximized over all linear combiner matrices $v^{n_q \times n_r}$, threshold vectors t^{n_q} , temporal processing matrix $b^{n \times n}$ and adaptive threshold coefficient matrices $u^{n \times n}$, is denoted by $C_{AT}(h^{n_r \times n_t}, n_q)$.

The BC model considered in this paper is formally defined below. An example is provided in Section IV.

Definition 2 (BC-QMIMO). A two-user MIMO broadcast channel with one-bit ADCs (BC-QMIMO) is characterized by the tuple $(n_t, n_{r,1}, n_{r,2}, h_1^{n_{r,1} \times n_t}, h_2^{n_{r,2} \times n_t}, n_{q,1}, n_{q,2})$, where n_t is the number of transmit antennas, $n_{r,i}$, $h_i^{n_{r,i} \times n_t}$, $n_{q,i}, i \in \{1, 2\}$ are the number of receive antennas, channel gain matrix, and number of one-bit ADCs at the i th receiver. The channel input vector is X^{n_t} and the output at the i th receiver is given by $Y^{n_{r,i}} = h_i^{n_{r,i} \times n_t} X^{n_t} + N^{n_{r,i}}$, $i \in \{1, 2\}$, where $N^{n_{r,i}}$ is a vector of independent, zero-mean and unit-variance Gaussian variables.

III. ADAPTIVE THRESHOLD ARCHITECTURES

It was shown in prior works that one-shot communication over PtP-MIMO systems with a limited number of one-bit ADCs at the receiver inflicts a rate-loss on the transmission system in the sense that the maximum achievable rate is

strictly less than the number of one-bit ADCs even at high SNRs [1], [6], [7]. More precisely, even in the ideal scenario when the SNR is taken to be asymptotically large, the one-shot capacity $C_{OS}(h^{n_r \times n_t}, n_q)$ is strictly less than n_q . The example in Section III.A illustrates how the proposed adaptive threshold architectures eliminate the aforementioned rate-loss. Particularly, Example 1 describes a method for constructing an equivalent scalar quantizer with 2^{n_q} quantization bins from n_q one-bit threshold ADCs. Section III.B builds upon this motivating example to propose a general coding strategy for PtP MIMO communication with AT-Rx architectures and derive an achievable rate region for arbitrary SNRs. Section IV further extends these ideas to communication over BC.

A. Motivating Example

The following example explains the rate-loss due to low resolution quantization in a simple SISO scenario and describes the proposed receiver architecture.

Example 1. One-shot Architecture: consider a PtP SISO communication scenario (i.e. $n_t = n_r = 1$), where the receiver is equipped with two one-bit ADCs (i.e. $n_q = 2$). Fig. 2(a) shows a generic one-shot PtP-QMIMO receiver in which the receiver antenna receives Y_1 , and produces the digitized signal:

$$(\widehat{W}_1, \widehat{W}_2) = \begin{cases} (-1, -1) & \text{if } Y_1 < t_1, \\ (-1, +1) & \text{if } t_1 < Y_1 < t_2, \\ (+1, +1) & \text{if } t_2 < Y_1, \end{cases}$$

where we have assumed that $t_1 < t_2$ without loss of generality. Note that the symbol $(+1, -1)$ is not produced at the receiver. In the high SNR scenario, the communication noise is negligible and rates close to $\log 3$ bits per channel-use are achievable. The rate is strictly less than $n_q = 2$ bits per channel-use.

Adaptive Threshold Architecture: Fig. 2(b) shows the proposed adaptive threshold architecture. The first ADC has zero threshold and outputs the sign of the received signal Y_1 . The threshold of the second ADC is adaptive and is set to be equal to half of the output of the first ADC in the previous channel-use. In the context of Definition 1, we have $n = 2$, $v^{2 \times 1} = \begin{bmatrix} 1 \\ 1 \end{bmatrix}$,

$b^{2 \times 2} = I_2$, and $u^{2 \times 2} = \begin{bmatrix} 0 & -\frac{1}{2} \\ 0 & 0 \end{bmatrix}$. Let $(\widehat{W}_1(i), \widehat{W}_2(i))$ be the output of the two ADCs at the i th channel-use. Then,

$$(\widehat{W}_1(i), \widehat{W}_2(i+1)) = \begin{cases} (-1, -1) & \text{if } Y_1(i) < -\frac{1}{2}, \\ (-1, +1) & \text{if } -\frac{1}{2} < Y_1(i) < 0, \\ (+1, -1) & \text{if } 0 < Y_1(i) < \frac{1}{2}, \\ (+1, +1) & \text{if } \frac{1}{2} < Y_1(i). \end{cases}$$

As a result, the rate of 2 bits per channel-use is achievable at high SNRs. Note that this rate is optimal in the sense that any other receiver architecture and coding scheme cannot achieve higher rates without increasing the number of one-bit ADCs.

B. Achievable PtP Rates

In the following, we consider communication over PtP-QMIMO systems and propose a communication scheme which

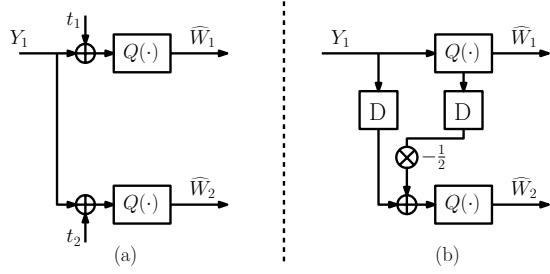


Fig. 2. (a) An OS-Rx system with fixed thresholds. (b) An AT-Rx system where the first ADC has zero threshold and the second ADC has an adaptive threshold which is equal to half of the output of the first ADC.

uses the singular value decomposition (SVD) in the analog domain to transform the communication system into s parallel, non-interfering channels. The i th parallel channel is allocated a number of $n_{q,i}$ one-bit ADCs, where $\sum_{i \in [s]} n_{q,i} = n_q$. The adaptive threshold architecture described in Example 1 is employed to construct an equivalent scalar quantizer with $2^{n_{q,i}}$ quantization bins. We calculate the maximum achievable rate for a given ADC allocation $(n_{q,1}, n_{q,2}, \dots, n_{q,s})$ and power allocation (P_1, P_2, \dots, P_s) for the subchannel subject to the total power constraint. The following theorem describes the set of achievable rates. The proof is provided in [15].

Theorem 1. *For the PtP-QMIMO characterized by $(n_t, n_r, h^{n_r \times n_t}, n_q)$ and average input power constraint P , the rate R is achievable if it satisfies the following inequality:*

$$R \leq \max \sum_{k=1}^s I(\tilde{X}_k; \tilde{Y}_k)$$

where the maximum is taken over $(n_{q,i})_{i \in [s]}, (P_i)_{i \in [s]}$ such that $\sum_{i \in [s]} n_{q,i} = n_q$, $\sum_{i \in [s]} P_i = P$, $\tilde{X}_k = a_k \cdot (2\tilde{X}_k - 1 - 2^{n_{q,k}})$, $\tilde{Y}_k = \sigma_k \tilde{X}_k + N_k$, $a_k = \sqrt{\frac{3P_k}{2^{n_{q,k}} - 1}}$, \tilde{X}_k is uniformly distributed over $[2^{n_{q,k}}]$, N^s is a vector of i.i.d. zero-mean Gaussian variables with unit variance, and σ_k is the k th singular value of $h^{n_r \times n_t}$.

Outline of proof. Let $n_{q,1}, n_{q,2}, \dots, n_{q,s} \in \mathbb{N} \cup \{0\}$ and $P_1, P_2, \dots, P_s \in \mathbb{R}^{\geq 0}$ such that $\sum_{i \in [s]} n_{q,i} = n_q$ and $\sum_{i \in [s]} P_i = P$. Let $h^{n_r \times n_t} = \Phi^{n_r \times n_r} \Sigma^{n_r \times n_t} \Gamma^{n_t \times n_t}$ be the SVD of the channel gain matrix. Let $X^{n_t} = \Gamma^{n_t \times n_t} \tilde{X}^{n_t}$. The transmitter sends \tilde{X}^s , the first s elements of the vector \tilde{X}^{n_t} . The receiver receives Y^{n_r} and computes \tilde{Y}^{n_r} such that $Y^{n_r} = \Phi^{n_r \times n_r} \tilde{Y}^{n_r}$ in the analog combiner module. The resulting parallel channels are $\tilde{Y}_i = \sigma_i \tilde{X}_i + \tilde{N}_i, i \in [s]$, where $\sigma_i, i \in [s]$ is the i th singular value of the channel matrix $h^{n_r \times n_t}$ and the power constraint $\mathbb{E}(\|\tilde{X}^s\|_2^2) \leq P$ must hold. The i th parallel channel is allocated $n_{q,i}$ one-bit ADCs and the average power constraint P_i . The $n_{q,i}$ one-bit ADCs are used to construct a uniform quantizer with $2^{n_{q,i}}$ levels as described in Example 1. The achievable rate is the summation of the rates of each sub-channel. It follows from standard Shannon theoretic arguments that the transmission rate of $I(\tilde{X}_k; \tilde{Y}_k)$ is achievable for the k 'th channel. As a result, the total transmission rate of $\sum_{k \in [s]} I(\tilde{X}_k; \tilde{Y}_k)$ is achievable. ■

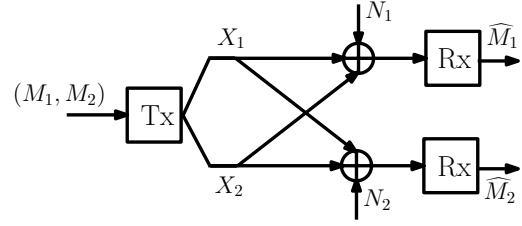


Fig. 3. A two user broadcast channel example.

Note that as $\text{SNR} \rightarrow \infty$, we have

$$I(\tilde{X}_k; \tilde{Y}_k) \xrightarrow{(a)} H(\tilde{X}_k) \xrightarrow{(b)} H(\tilde{X}_k) \xrightarrow{(c)} n_{q,k},$$

where (a) holds since at high SNR we have $h(\tilde{X}_k|\tilde{Y}_k) \approx 0$, (b) follows by the bijectivity of the mapping $\tilde{X}_k = a_k \cdot (2\tilde{X}_k - 1 - 2^{n_{q,k}})$, and (c) holds since \tilde{X}_k is uniformly distributed over $[2^{n_{q,k}}]$. As a result, the total transmission rate approaches n_q . Consequently, the performance converges to optimality as SNR is increased asymptotically since no more than n_q bits per channel-use may be decoded using n_q one-bit ADCs at each channel-use. This is in contrast with [1] and [6], where the achievable rate grows logarithmically in the number of ADCs at high SNRs.

IV. BROADCAST CHANNEL COMMUNICATION STRATEGIES

In this section, we propose BC coding strategies and derive achievable regions for communication over the BC.

A. Motivating Example

The following example describes the key ideas used in the proposed coding strategies.

Example 2. Consider the two-user broadcast channel shown in Fig. 3. The BC-QMIMO system is characterized by $(n_t, n_{r,1}, n_{r,2}, h_1^{n_{r,1} \times n_t}, h_2^{n_{r,2} \times n_t}, n_{q,1}, n_{q,2})$, where $n_t = 2, n_{r,1} = n_{r,2} = n_{q,1} = n_{q,2} = 1$, and $h_1^{n_{r,1} \times n_t} = h_2^{n_{r,2} \times n_t} = \begin{bmatrix} 1 & 1 \end{bmatrix}$. We consider the achievable rate vectors when $\text{SNR} \rightarrow \infty$ when one-shot and adaptive threshold architectures are used at the receiver.

One-shot Architecture with Zero Thresholds: If the receivers are equipped with one-shot architectures and zero-threshold ADCs (i.e. $t_{1,k} = 0, k \in \{1, 2\}$), then the two users' channels are statistically equivalent. As a result, each receiver may decode the other receivers' message. Consequently, by Fano's inequality, $R_1 + R_2 \leq 1$.

One-shot Architecture with Non-zero Thresholds: Consider a one-shot architecture where the first receiver is equipped with a zero-threshold ADC and at the second receiver, the ADC threshold is equal to $0 < \epsilon \ll P$. Let the channel input be equal to $X_1 + X_2 = (-1)^{U_1} \frac{\sqrt{P'}}{2} + (-1)^{U_2} \sqrt{P'}$, where $P' = \frac{4}{5}P$ and U_1 and U_2 correspond to the binary messages sent to receivers one and two, respectively. It is straightforward to verify that $R_1 + R_2 = 1 + C$, where C is the capacity of a binary Z-channel with cross-over probability $\frac{1}{2}$.

Adaptive Threshold Architecture: Let each receiver be equipped with the adaptive threshold architecture, where the

temporal processing matrix is $b^{2 \times 2} = \begin{bmatrix} 1 & 1 \\ 0 & 0 \end{bmatrix}$, $v^{1 \times 1} = 1$, and the adaptive threshold coefficient matrix is $u^{2 \times 2} = \begin{bmatrix} 0 & -\frac{1}{2} \\ 0 & 0 \end{bmatrix}$.

We argue that the symmetric sum-rate of 2 bits per channel-use (1 bit per channel-use for each user) is achievable using this architecture. Assume that the transmitter is to send the message $(U_{i,1}, U_{i,2}, \dots, U_{i,m})$, $i \in \{1, 2\}$ to the i th receiver over $m+1$ channel-uses, where $U_{i,j}$, $j \in [m]$ are independent binary symmetric variables and m is an odd number. The odd (even) channel-uses are used to transmit two bits of information to the first (second) receiver. More precisely, the channel input in the j th channel-use is

$$X_j = X_{1,j} + X_{2,j} = (-1)^{U_{k,j'}} \sqrt{P'} + (-1)^{U_{k,j'+1}} \frac{\sqrt{P'}}{2},$$

where $P' = \frac{4}{5}P$, in the odd channel-uses $k = 1$ and $j' = j$, and in the even channel-uses $k = 2$ and $j' = j - 1$. We explain the decoding process at the first receiver in the first two channel-uses. The decoder receives Y_1 and feeds it to a zero-threshold ADC to recover $U_{1,1}$. It also stores Y_1 using a delay element and in the next channel-use feeds it to the ADC with threshold $\frac{1}{2}U_{1,1}$. The second decoder uses a similar method to recover its corresponding message. Note that the resulting sum-rate approaches 2 bits per channel-use as $m, \text{SNR} \rightarrow \infty$.

We observe that in the adaptive threshold architecture described in Example 2, the transmitter uses a time-sharing method where the odd (even) channel-uses are used for transmission to the first (second) user. However, the one-bit ADCs at both receivers are active at all channel-uses. This leads to optimal performance at high SNRs where the communication bottleneck is the number of one-bit ADCs. In the next section, we build upon the time-sharing strategy to derive an achievable region for the general BC-QMIMO system.

B. Achievable Regions

In this section, we build upon the time-sharing strategy described in Example 2 and the coding strategy used in Theorem 1 to provide achievable rate-regions for the two user BC-QMIMO under quantization resolution constraints when adaptive threshold architectures are used at the receivers. We prove the following theorem in [15].

Theorem 2. Consider the BC-QMIMO system characterized by $(n_t, n_{r,1}, n_{r,2}, h_1^{n_{r,1} \times n_t}, h_2^{n_{r,2} \times n_t}, n_{q,1}, n_{q,2})$. Let \mathcal{R} be the set of rate vectors (R_1, R_2) for which there exists $(n_{q,j,k})_{k \in [s_j], j \in \{1, 2\}}$ and $(P_{j,k})_{k \in [s_j], j \in \{1, 2\}}$ satisfying the following bounds:

$$\sum_{k \in [s_j]} n_{q,j,k} = n_{q,j}, \quad \sum_{k \in [s_j]} P_{j,k} = P,$$

$$R_j \leq \frac{1}{2} \sum_{k \in [s_j]} I(\tilde{X}_{j,k}, \tilde{Y}_{j,k}),$$

where $s_j, j \in \{1, 2\}$ is the number of singular values of $h_j^{n_{r,j} \times n_t}$, $\tilde{X}_{j,k} = a_k (2\tilde{X}_{j,k} - 1 - 2^{2n_{q,j,k}})$, $\tilde{Y}_{j,k} = \sigma_{j,k} \tilde{X}_{j,k} + N_{j,k}$, $k \in [s_j]$, $j \in \{1, 2\}$, $a_{j,k} = \sqrt{\frac{3P_{j,k}}{2^{4n_{q,j,k}} - 1}}$, $\tilde{X}_{j,k}$ is uniformly distributed over $2^{2n_{q,j,k}}$,

and $\sigma_{j,k}$ is the k th singular value of $h_j^{n_{r,j} \times n_t}$. Then $\text{conv}(\mathcal{R})$ is a subset of the optimal achievable rate region, where $\text{conv}(\cdot)$ is the convex hull function.

The rate pair $(n_{q,1}, n_{q,2})$ is achievable at high SNR since $I(\tilde{X}_{j,k}, \tilde{Y}_{j,k}) \rightarrow 2n_{q,j,k}$, $j \in \{1, 2\}, k \in [s_j]$ as shown in Section III. As a result, the coding scheme is optimal at high SNRs in the sense that the rate pair $(n_{q,1}, n_{q,2})$ cannot be improved upon unless the number of one-bit ADCs is increased.

V. CONCLUSION

We have studied multiterminal communication over MIMO channels when a limited number of one-bit ADCs are available at the receiver terminals. We have proposed a receiver architecture which uses adaptive thresholds ADCs to mitigate the rate-loss due to low resolution quantization. We have derived achievable rate regions for communication over point-to-point and the two user broadcast channel. We have shown that the achievable regions are tight as the SNR goes to infinity.

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