Memory and Logic soft error improvement using phase transition material assisted transistors

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***Abstract*— Phase transition Material (PTM) assisted logic and SRAM bitcells have been proposed with improved soft error tolerance. The large insulating resistance of PTM hinders the propagation of glitches to subsequent stages thereby improving the immunity to radiation strikes. Also, the abrupt switching to metallic phase minimizes the delay penalty thereby offering an optimized solution. We present a detailed PTM parameter optimization for optimum soft error performance. We also quantify the improvement in the Soft Error Tolerance of logic and 6T SRAM bit cell configuration.**

***Index Terms*— Phase Transition Material (PTM), Soft Error Tolerance (SET), Critical Charge**

I. Introduction

The reducing feature size and operating voltages of modern day silicon circuits is dramatically increasing their vulnerability to soft errors [1]-[3]. These soft errors are induced through alpha particle strike (emitted by radioactive substance in the IC packaging materials) or neutron particle strike (caused through cosmic ray interaction) onto the semiconductor surface. The alpha particle strike ionizes the silicon substrate generating electron hole pairs. Although neutron interaction does not ionize silicon directly, the elastic/inelastic collisions eventually generates electron hole pairs. The generated electron hole pairs drift under the influence of electric field resulting in current spike at the nearest node thereby inducing soft errors in circuits. Soft errors can cause the data loss of single bit (Single Bit Upset) or multiple bits (Multi Bit Upset) in the logic/memory circuits. Especially, the electronics designed for space applications are highly susceptible to data loss (soft errors) due to the high LET (Linear Energy Transfer) associated with particle strikes.

Traditionally, soft error tolerant approaches utilized redundancy techniques such as TMR [4] (Triple Modular Redundancy), DMR [5] (Dual Modular Redundancy) to enhance their immunity to particle strikes. Various other techniques such as transistor gate sizing have been proposed for radiation hardening. Also, researchers have proposed various SRAM bit cell configurations such as Dual Interlocked Cell (DICE) [6], Quatro cell [7] to reduce the memory Soft Error Rate (SER). However, these approaches incur significant area and performance overhead. Hence, radiation hardened circuit topologies need to be developed minimizing area, power and delay overheads.

In this paper, we propose a novel assist technique to enhance the immunity of the logic and memory circuits to soft errors with a minimal performance penalty and zero area overhead. The key contributions of this paper are:

1. We propose integration of phase transition material onto the baseline CMOS for improved soft error tolerance.
2. We evaluate the soft error performance of PTM assisted 6T SRAM bit cell for single event upset (SEU) radiation strike and compare with other CMOS variants.
3. We present a detailed analysis describing the influence of PTM parameters and the impact of PTM switching time on the soft error tolerance of circuits.
4. We propose PTM assisted logic circuits with enhanced immunity to soft errors.

II. Phase Transition Material

A. Phase Transition Material

Transition metal oxides such as Vanadium dioxide (VO_2) or Niobium dioxide (NbO_2) undergo phase transition under application of external electric field [8-9]. These materials exhibit abrupt insulator to metal phase transition owing to the interaction of various microscopic degrees of freedom such as charge, lattice, orbital and spin. Researchers are exploiting this novel property to realize devices with completely unique electrical characteristics showing promise for transformational circuit topologies such as hyper-FET and selector switch for crossbar arrays [10-11]. In this work, we leverage this novel property of voltage dependent resistance change in PTMs to suppress the radiation strike induced glitch propagation in the logic gates and to avoid bitflips in a SRAM array. The intrinsic switching time of the PTM also helps in filtering out the narrow pulse-width radiation strikes thereby improving the soft error immunity.

B. Phase Transition Material based MIM fabrication

Two terminal MIM structures with Phase Transition Material (VO_2) sandwiched in between metal electrodes have been fabricated and characterized. 100 nm thick VO_2 thin films has been deposited on n++ silicon substrate through thermal evaporation of commercially available VO_2 powder. Fig.1 shows the SEM (Scanning Electron Microscope) image of the deposited thin film. The physical composition of the thin film was verified through X-

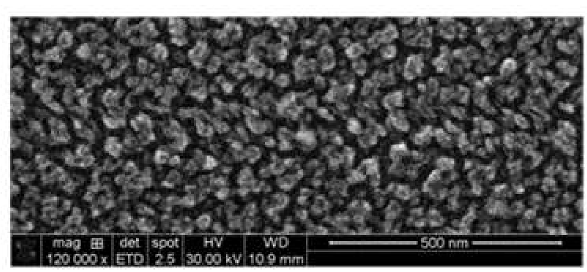

Fig.1 SEM cross section of deposited VO_2 thin film

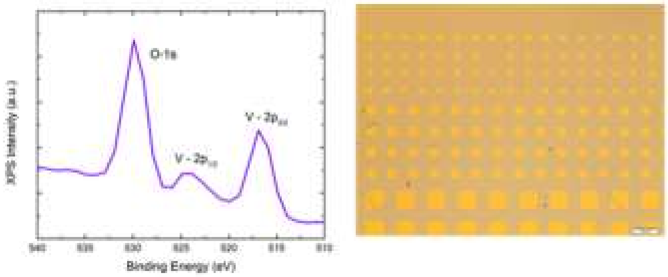

Fig. 2 Measured XPS and top view of fabricated VO₂ M-I-M structures

ray photoelectron spectroscopy (XPS) studies as shown in Fig.2. The n++ silicon substrate served as the bottom electrode. Nickel metal was deposited to serve as top electrode through e-beam evaporation. The deposited nickel was patterned to form vertical isolated MIM structures with dimensions varying from (5 um x 5 um) to (125 um x 125 um). The fabricated MIM structures were characterized and the obtained IV characteristics are shown in Fig.3.

C. Electrical Characteristics

The electrical characteristics of PTM observed in our experiment and other experiments in the literature can be modelled using few parameters. Table.1 highlights those parameters and their respective values [12] used for the purpose of simulation in this work. $\rho_{INS}/_{MET}$ represents the resistivity of the PTM in insulating/metallic phase respectively. $J_{CIMT}/_{CMIT}$ correspond to the current density required to trigger the (insulating to metallic) and (metallic to insulating) phase transitions respectively. L_{PTM} and A_{PTM} represent the length and area of cross section of PTM respectively. Under zero bias condition (V_{DC}=0 V), the PTM is in insulating phase with very high resistance (R_{INS} = ρ_{INS} x L_{PTM}/A_{PTM}). A Current ($I=V_{DC}/R_{INS}$) begins to flow in the circuit on application of voltage bias across its terminals. As the current in circuit reaches insulator-metal transition threshold (I_{IMT} = J_{CIMT} x A_{PTM}), phase transition to metallic phase is triggered. The corresponding voltage bias is referred to as V_{IMT} (V_{IMT} = I_{IMT} x R_{INS} = J_{CIMT} x ρ_{INS} x L_{PTM}) threshold. Although the phase transition is current driven, for easier understanding we use voltage switching thresholds in the circuit description. Also, the PTM requires finite time to completely transit from insulating phase to metallic phase (and vice versa) referred to as intrinsic switching time (T_{PTM}). This intrinsic switching time has been experimentally demonstrated to be in the sub-nanosecond regime [13] and projected to be ~ 50ps for scaled dimensions [14]. In the metallic phase, a large current flows in the circuit ($I=V_{DC}/R_{MET}$) where R_{MET} is the resistance of the PTM in metallic phase ($R_{MET}=\rho_{MET}$ x L_{PTM}/A_{PTM}). The PTM exhibits hysteresis behavior corresponding to the current-voltage characteristics. A reverse phase transition to insulating phase is triggered as the current in the circuit reduces and reaches I_{MIT} (I_{MIT} = J_{CMIT} x A_{PTM}) threshold and the corresponding voltage threshold is V_{MIT} (V_{MIT} = I_{MIT} x R_{MET} = J_{CMIT} x ρ_{MET} x L_{PTM}).

D. Soft-FET

The PTM device when placed in series with the gate of the baseline MOS transistor exhibits soft switching transistor behavior as shown in Fig. 4 referred as "Soft-FET" [15]. The PTM changes the transient behavior resulting in soft and delayed switching of the baseline MOS transistor. However, the DC characteristics of the proposed Soft-FET remain unchanged. When, $V_G=V_{IN}$=0V the PTM is initially in the insulating phase. Hence, the gate capacitor is charged with large associated time constants (R_{INS}*C_G) leading to slow increase in V_G (horizontal portion of staircase waveform). This causes an increasing voltage difference across the PTM (V_{IN}-V_G) triggering phase transition to metallic phase (at V_{IMT} threshold). In the metallic phase the gate capacitor is charged with a small associated R_{MET}*C_G time constant (vertical portion of staircase waveform). This leads to decreasing voltage difference (V_{IN}-V_G) across the PTM and triggers the reverse phase transition (at V_{MIT}). This alternating slow and quick charging cycle continues until $V_G=V_{CC}$ resulting in staircase waveform as shown in Fig.4. The Soft-FET exhibits soft switching staircase behavior only when the T_{PTM} << R_{INS}*C_G else the PTM behaves like passive Series-R (as the phase transition cannot be triggered). Fig.4 highlights the BEOL (Back end of line) integration process steps of PTM. The PTM can be envisioned as 'special gate via' and hence does not incur any active silicon area penalty.

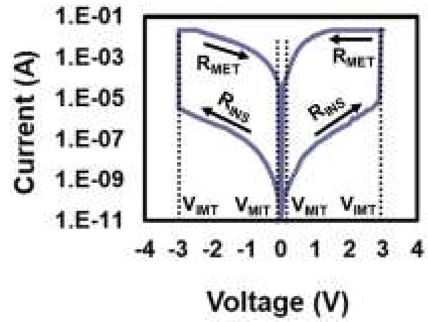

Fig. 3 Measured I-V characteristics: VO₂ M-I-M structures

ρ_{MET}	5×10^{-3} Ω-cm
ρ_{INS}	1 Ω-cm
J_{CMIT}	10^6 A/cm^2
J_{CIMT}	4×10^4 A/cm^2
L_{PTM}	36 nm
A_{PTM}	36 nm x 20 nm

Table.1 PTM parameters

III. Radiation Hardened PTM assisted SRAM bitcell

A. Simulation Setup

The proposed design is evaluated by performing SPICE simulations using commercial 40 nm CMOS process technology. The electrical characteristics of the phase transition material have been emulated using a Verilog-A model [16]. The SEU radiation is modelled as the double exponential current spike [17] as shown in Fig.5. The τ_R and τ_F parameters correspond to the rise and fall time constants of the spike respectively. The SEU radiation strike can have pulse widths ranging from few picoseconds to few hundred picoseconds [18]. The SEU radiation pulse-widths in this study are varied following the earlier study on single event transient cross sections for advanced technology nodes [19]. An SEU radiation strike can deposit sufficient charge at the affected node to induce transitions from (1→0) or (0→1). The weaker PMOS provides the restoring current in the case of radiation strike induced (1→0) transition. This worst-case SEU scenario has been considered for all the subsequent simulations.

B. Radiation Hardened 6T SRAM bitcell

Radiation induced bit flips are highly prevalent in the high-density SRAM bitcells employing minimum geometry transistors. The SEU voltage spike can trigger bitflip (data loss) in the SRAM

Fig.4 Soft-FET schematic, transient response and layout

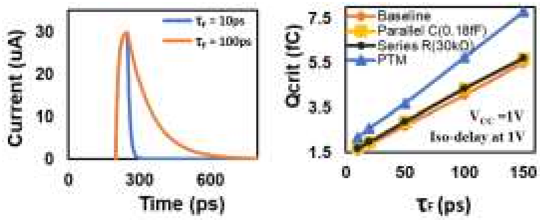

Fig.5 Double exponential current spike and Q_{CRIT} variation with fall time constant, τ_F

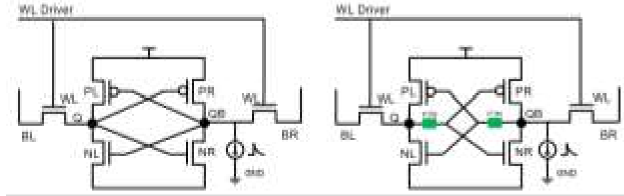

Fig.6 SRAM schematic without and with~~out~~ PTM

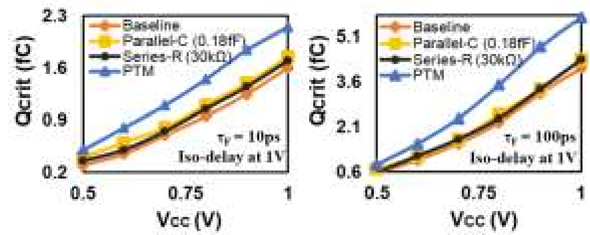

Fig. 7 Q_{CRIT} variation with supply voltage for τ_F=10 ps strike (left) and τ_F=100 ps strike (right)

bitcell owing to the positive feedback loop. We propose the integration of PTM based Soft-FET SRAM bit cell to improve the immunity against radiation strikes. Fig.6 shows the schematic of the PTM assisted 6T SRAM bitcell and the baseline 6T SRAM bitcell with radiation strike positioned at QB storage node (storing logic '1'). The SEU radiation strike at any storage node must traverse through the PTM to disrupt the other storage node. The PTM delays this propagation through two mechanisms,

(1) The PTM with inherently high insulating resistance (R_{INS}) delays the propagation of the spike owing to the large R_{INS}*C_G time constant. Hence, the radiation strikes which cannot deposit sufficient charge to trigger the insulator-metal transition are completely filtered out thereby protecting the nodes. It should be noted that although this delay blocks the small signal transients (such as radiation strikes), the large signal voltages remain unaffected (as they can strongly trigger the insulator-metal transition). Hence, the write-time of the PTM assisted SRAM bitcell is significantly smaller than the equivalent series resistor offering the same soft error tolerance.

(2) The intrinsic switching time of the PTM also plays a crucial role in determining soft error performance. Although the high LET (Linear Energy Transfer) strikes can trigger insulator-metal transition, the PTM requires intrinsic switching time to complete the phase transition. Hence, the radiation strikes with pulse width much smaller than T_{PTM} are compensated by the restoring currents before propagating to other storage node. Further, the presence of two PTMs increases the propagation delay of the positive feedback loop (QB→ Q →QB) thereby improving the soft error tolerance.

In summary, the PTM completely blocks the radiation strikes either with smaller amplitude (irrespective of pulse width) or with smaller pulse widths (irrespective of amplitude). In addition, the PTM also improves the immunity to large LET strikes induced soft errors.

C. Simulation Results

Critical charge (Q_{CRIT}) has been proven as an important metric to evaluate the soft error immunity in the SRAM memory circuits. Hence, we choose Q_{CRIT} to gauge the performance of the proposed design. Q_{CRIT} is calculated as the minimum amount of charge that can induce a bitflip in the SRAM bitcell. Fig.5 shows the variation of the Q_{CRIT} with the fall time constant (τ_F) of the double exponential current waveform. To evaluate the soft error improvement of PTM assisted circuits two other variants (Series Resistor and Parallel Capacitor) have also been compared. The inclusion of Series R (passive resistor replacing PTM in Fig.6) and Parallel C (additional capacitance at Q and QB nodes without PTM) increases the write-time of the SRAM bitcell. We gauge the performance of the proposed design by comparing the Q_{CRIT} of the effective Series-R (30 kΩ) and effective parallel-C (0.18 fF) that produce the same delay penalty as PTM (iso-write-time at 1V). As shown in Fig. 5, the PTM achieves approximately 1.5x improvement in the Q_{CRIT} for large pulse width strikes. Although, the PTM in insulating phase incorporates delay, the PTM in metallic phase compensates for the loss leading to reduced overall delay. In addition, the PTM shows superior soft error performance across the supply voltage (V_{CC}) range as shown in Fig.7. As a representative of neutron strike and alpha particle strike we conduct the study for two values of τ_F (= 10 ps and 100 ps) keeping τ_R constant (=10 ps) as suggested by [17]. The proposed design achieves 1.3x and 1.4x improvement in the Q_{CRIT} for low pulse width (τ_F=10 ps) and high pulse width (τ_F=100 ps) radiation strikes respectively.

D. Design Space Exploration

As explained in the previous section, the insulating phase resistance and intrinsic switching time of the PTM play a crucial role (owing to the two mechanisms) in determining the soft error tolerance. Hence, we conduct PTM parameter sensitivity analysis to the understand the impact of these two parameters on the Q_{CRIT}. The insulating phase resistance (R_{INS}) can be varied by altering the dimensions of the PTM ($R_{INS} = \rho_{INS}$ x L_{PTM}/A_{PTM}). It should be noted that altering the device dimensions also alters the voltage thresholds ($V_{IMT/MIT}=\rho_{INS/MET}$ x $J_{CIMT/CMIT}$ x L_{PTM}) which can affect the soft error performance. Hence, we hold the voltage thresholds constant by not altering L_{PTM} but vary R_{INS} by just changing A_{PTM}. Although altering A_{PTM} does change R_{MET}, it does not significantly affect the soft error performance. The intrinsic switching time on the other hand, is strongly dependent on the growth techniques/fabrication processes of the material. Fig.8 shows the Q_{CRIT} variation as a function of both T_{PTM} and R_{INS} for (τ_F= 10 ps) and (τ_F= 100 ps) radiation strikes. It is evident that the Q_{CRIT} increases with increasing T_{PTM} and R_{INS} in accordance with the two explained mechanisms. It should be noted that for 10 ps case, the SRAM bitcell essentially does not flip for large R_{INS} and

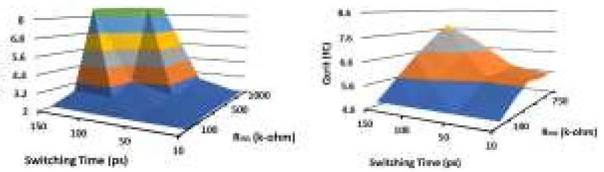

Fig.8 Q_{CRIT} variation with switching time and insulating resistance for (τ_F=10 ps) and (τ_F=100 ps)

T_{PTM} values (large peaks in left Fig. 8 showing Q_{CRIT} above the Y axis maxima). This can be explained by the propagation time being much larger than the strike pulse width. Also, it is evident that the Q_{CRIT} is independent of the T_{PTM} at low R_{INS} values. The low R_{INS}*C_G time constant accelerates the charging thereby not allowing sufficient voltage to build up across the PTM. As the PTM is always in the insulating phase, the Q_{CRIT} is independent of T_{PTM}. Based on the parameter sensitivity analysis, an optimized PTM with high R_{INS}, low V_{IMT} and moderate T_{PTM} can yield improved soft error tolerance with minimal write-time overhead.

IV. Radiation hardened PTM assisted logic

. With technology scaling, the impact of SER on static CMOS logic has been predicted to increase significantly. We propose the integration of PTM based Soft-FET to tackle increasing logic SER. Fig. 9 shows the schematic of the PTM assisted 11-stage ring oscillator. Q_{CRIT} in logic gates is quantified as the minimal SEU induced charge required to generate 50% of V_{CC} transition at the logic gate output node. PTM assisted logic gate shows improved Q_{CRIT} compared to the baseline design. The PTM assisted logic effectively filters out the spikes/glitches within few stages as evident from Fig.9. An iso-radiation strike of 60 uA amplitude and 20 ps τ_F was simulated to compare the glitch propagation. I2, I4, I6, I8 and I10 represent the node voltages at the output of 2nd, 4th, 6th, 8th and 10th inverter respectively. The PTM assisted logic filters out the glitches within 4 stages of the inverter chain as opposed to all stage propagation in baseline design.

V. Conclusion

In this work, we proposed novel integration of Phase Transition Material onto baseline CMOS for improved soft error tolerance. The proposed radiation hardened SRAM bitcell shows approximately 1.35X improvement in Q_{CRIT} compared to other CMOS variants for the same write delay. This improvement in the soft error tolerance can be achieved at zero silicon area overhead at minimal delay degradation. However, to compensate the delay due to PTM switching, transistor upsizing and transistor V_T reduction can be explored. Further, NbO_2 (another Phase Transition Material) characteristics are unaffected upto 1000K making it suitable for radiation hardening applications. Recent experimental investigations on these materials have shown the reliability > 10^9 cycles [20]. However, device to device variability of PTM parameters is one of the major challenges and is being thoroughly explored. Thus, phase transition materials can act as effective technology-assists in improving soft error immunity without significant delay and active area penalty. Further optimization of PTM parameters can improve the soft error performance of these circuits.

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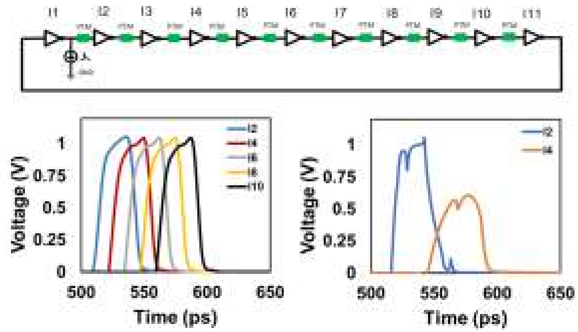

Fig.9 PTM assisted ring oscillator schematic (top) and Glitch propagation along the inverter chain for baseline (left) and PTM assisted inverter chain (right)

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