A Predictive Process Design Kit for Three-Independent-Gate Field-Effect Transistors

Ganesh Gore, Patsy Cadareanu, Edouard Giacomin, and Pierre-Emmanuel Gaillardon
Electrical and Computer Engineering Department
University of Utah
Salt Lake City, Utah, USA
pierre-emmanuel.gaillardon@utah.edu

***Abstract*—The *Three-Independent-Gate Field-Effect Transistor* (TIGFET) is a promising beyond-CMOS technology which offers many unique properties, such as (i) dynamic control of the device polarity, (ii) dual threshold operation and (iii) more expressive logic capabilities. The efficient exploitation of these properties provides opportunity to design area and power optimized logic circuits. However, the evaluation of TIGFET-based design currently relies on a close approximation for the *Power, Performance, and Area* (PPA) rather than traditional layout-based methods. There is a need for a publicly available *Process Design Kit* (PDK) enabling systematic evaluation of the design area. In this paper, we propose Predictive PDK for the 10 nm-diameter silicon-nanowire TIGFET device. This work consists of a SPICE model and full custom physical design files including a *Design Rule Manual*, a *Design Rule Check*, and a *Layout Versus Schematic* decks for Calibre®. We then validate the design rules through the implementation of basic logic gates and a full-adder and compare extracted metrics with FreePDK15nm™ PDK. We show 26% and 41% area reduction in the case of an XOR gate and a 1-bit full-adder design respectively.**

I. Introduction

In the past decade, the semiconductor industry has seen exponential growth in computationally intensive applications such as artificial intelligence, augmented reality, and machine learning. Scaling down the standard semiconductor technologies based on *Complementary Metal-Oxide-Semiconductor* (CMOS) devices has been the primary solution for achieving these performance requirements. With a reduction in transistor size, undesired short-channel effects such as increased leakage current start dominating the device operation. Several 3D semiconductor structures such as *Fin Field-Effect Transistor* (FinFET) or *Gate-All-Around* (GAA) configurations have been proposed to enhance channel electrostatic control and reduce leakage current [1]. However, their fabrication in the sub-10 nm regime is increasingly difficult and expensive [2] and so there is a need to investigate devices which can be scaled functionally rather than physically.

Substantial research has been devoted to novel semiconductor structures [3]–[5]. Device level innovations such as novel geometries and materials introduce improved logic devices such as Spintronics-based FETs, Tunnel FETs, and Ferroelectric FETs [7] or FETs with enhanced functionality [3], [4]. In particular, *Multiple Independent Gate FETs* (MIGFETs), which use additional gate terminals to configure the device to different modes of operation [8]–[11], are considered a promising alternative to conventional MOSFETs.

One promising MIGFET device is the *Three-Independent-Gate FET* (TIGFET) [12], which introduces two gate terminals called *Polarity Gates* (PG) to a traditional FET structure. PG terminals allow for a dynamic configuration of the device to *n*-type or *p*-type. The ability to dynamically control device polarity gives TIGFETs a higher expressive logic capability than conventional devices, resulting in a compact logic gate implementation and lower leakage current per cell. As a result, the circuit-level benefits of TIGFETs have been largely investigated in literature in the past few years and have shown promising implementations for a wide range of logic circuits such as multiplexers [13], adders [14], flip-flops [15] or for use in differential power attack mitigation techniques [16]. However, the area evaluation of TIGFET-based design currently relies on an approximation rather than traditional layout-based methods since no TIGFET-based *Process Design Kit* is publicly available.

In this paper, we introduce an open-source TIGFET PDK available online [17], to be integrated with Cadence® Virtuoso. The *Design Rule Manual* for the proposed PDK is derived from previously fabricated TIGFET device [4] and the publicly available FreePDK15nm™ PDK [18]. Our PDK consists of a SPICE Verilog-A model for a 10 nm diameter *Silicon Nanowire* (SiNW) TIGFET and includes full custom design files, *Design Rule Check* (DRC), and *Layout Versus Schematic* (LVS) decks. The availability of this PDK will allow universities and researchers to explore the benefits of TIGFETs in various domains. The benefits of the proposed PDK are as follows:

- It provides design rules and a layout consistency check for a more reliable and reproducible system design,
- It allows accurate metric evaluations, such as area or delay, of TIGFET-based designs,
- It showcases the area benefits of 26% and 41% for TIGFET-based an XOR and a 1-bit full adder.

The rest of this paper is organized as follows: Section II provides an overview of TIGFET technology. Section III introduces the electrical model of the proposed TIGFET device. Section IV describes the physical TIGFET design and briefly describes the DRC and LVS decks. Section V evaluates the regular layout technique for TIGFETs and showcases the benefits of TIGFET-based applications. Section VI concludes this paper.

II. Technical Background

In this section, we establish the necessary background to understand TIGFET technology. We then briefly review circuit-level opportunities brought by TIGFET devices and discuss publicly available design kits.

A. TIGFET Operation

The TIGFET is composed of drain and source contacts as well as three independent gate contacts, as shown in Fig. 1 (a). The *Control Gate* (CG) controls the potential barrier in the channel in the same manner the gate contact works in a conventional MOSFET device and turns the device *on* or *off*.

The *Polarity Gates* (PG) at the source and drain modulate their respective Schottky barriers, selecting the type of carriers which will enter the channel and dominate the current flow; the ability to make this selection is called device reconfigurability. TIGFET devices have been successfully fabricated with several materials such as Silicon [19], 2D materials, [20] and SiNW [21]. In this paper, we will consider a SiNW TIGFET which is fabricated using a fully CMOS-compatible process. The scanning electron microscopy of a previously fabricated TIGFET is depicted in Fig. 1 (b) [21].

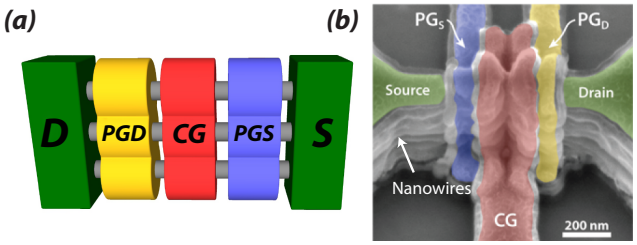

Fig. 1: (a) TIGFET general structure; (b) Scanning Electron Microscopy image of a fabricated TIGFET device comprising of four vertically stacked silicon nanowires [21].

B. Circuit-level Opportunities

TIGFETs show richer switching capabilities per given transistor and this ability is used to implement compact logic gates. For instance, as shown in Fig. 2 (a), a TIGFET NAND requires one fewer transistor than its CMOS counterpart. Similarly, as illustrated in Fig.2 (b) and (c), a CMOS 2-input XOR and 3-input majority gate require 8 and 10 transistors respectively, whereas a TIGFET based implementation requires only 4 transistor per gate. This leads to an area reduction, as is demonstrated in Section V.

C. Publicly Available Physical Design Kits

Previously PDKs based on predictive technologies has been released in the public domain. such as FreePDK45nm [22] and FreePDK15nm [18] which provides the design rules and standard cell libraries [23] for planar CMOS technology. The ASAP7 PDK [24] was released for the more advanced 7 nm FinFET technology node. The set of realistic assumptions included in the ASAP7 PDK simplifies its use in an academic setting. Most recently, an add-on for the FreePDK45nm was proposed to integrate CMOS-compatible Resistive RAM technology with CMOS design [25].

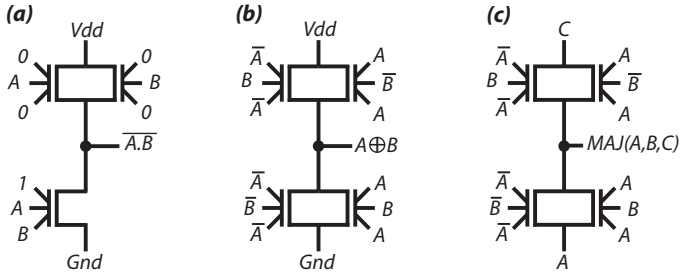

Fig. 2: TIGFET compact gates: (a) 2-input NAND; (b) 2-input XOR; (b) 3-input majority gate.

III. TIGFET Device Properties

In this section, we evaluate the electrical properties of the TIGFET device and present the TIGFET SPICE model which is used in the provided as a part of the PDK.

A. Device TCAD Work

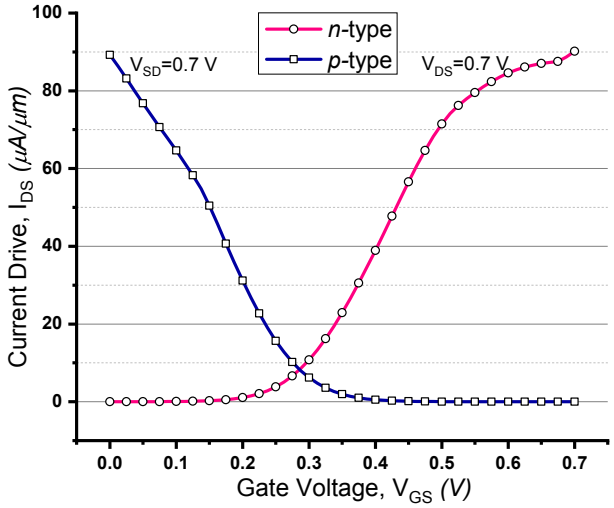

Fig. 3: I_D-V_G characteristics of the 10 nm TIGFET device with V_{DD}= 0.7 V.

TCAD simulations of a 10 nm SiNW TIGFET device with gates of 10 nm and separations of 10 nm were performed in Synopsys Sentaurus. Nickel silicide-silicon is the assumed Schottky barrier contact and the dielectric layer is HfO_2 with a thickness of 8nm. Electrical properties, such as the ON-current (I_{ON}), the OFF-current (I_{OFF}) and the nominal voltage (V_{DD}) were extracted from these simulations. The maximum current drive for *n*-type operation is 90.20 μA/μm and for *p*-type is 89.25 μA/μm, as seen in Fig. 3. These current drives are approximately 10× lower than the previous 22 nm TIGFET device simulations [7] which was operated at a supply voltage of 1.2 V. This reduction in current density is primarily due to the 0.7 V supply voltage used in the 10 nm devices as is standard for technology at this node. This

lowered supply voltage is necessary for fair comparisons with the corresponding CMOS technology. The real benefit to these devices is their reconfigurability, as used in Section V.

B. SPICE Verilog-A Model

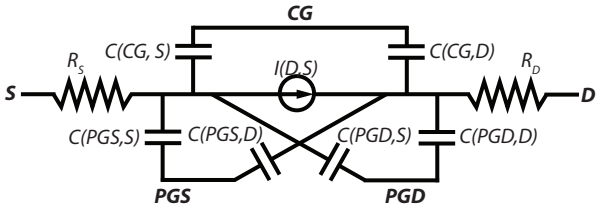

Fig. 4: Macro model of a SiNW TIGFET.

The TCAD simulation results have been used to develop a TIGFET macro model in Verilog-A, as shown in Fig. 4. The nonlinear current source $I(D, S)$ is modeled using TIGFET macro model approach and a function of the drain, source and all three gate voltages. The table stores the current $I(D, S)$ for each bias point combination applied on the device terminals. We chose a bias point granularity of 0.1 V on the PG gates at the source and drain and the CG terminal, and a 0.05 V bias on the drain terminal, totaling to 67,536 bias points. For other bias points, the model uses linear interpolation and extrapolation techniques. Linear interpolation provides relatively better convergence in transient simulation and avoids any spurious false peaks. To model transient behavior, the capacitance between each terminal pair is extracted by AC simulations from TCAD and the average value obtained under all the bias conditions is considered in the proposed model. The terminal access resistances are also extracted using TCAD simulations.The coupling capacitance between gate terminals is very small and omitted from the model. Since TIGFETs are built using vertically stacked SiNWs, as explained in Section II-A, the proposed SPICE model assumes a single SiNW by default. To change the number of wires in the stack, a *nw* design parameter can be changed. A comparison of SPICE model and TCAD simulation result indicates less than 0.1% mean square error for both DC and transient simulations.

IV. TIGFET Physical Design

In this section, we briefly present the TIGFET fabrication process requirements and corresponding constraints. Then, we summarize the sets of DRC and LVS rules. Finally, we discuss the implications of a TIGFET-based physical design.

A. Process Assumptions

In the proposed PDK, we consider *Dual Patterning Lithography* (DPL) for patterning of the gate layer and the first four metal layers. Every DPL layer requires decomposition before the fabrication process. In commercial PDKs this decomposition is achieved by providing different colors for each DPL layer. When two patterns have to be drawn in the same layer with spacing smaller than provided by single patterning lithography, It is drawn using two different colors which correspond to two different masks. These two separate masks are then connected together by inserting a stitch to form an electrical connection between them [27]. A minimum number of stitches must be introduced into each layer to stall printability degradation [28]. Process modeling is also recommended to ensure correct decomposition of layers. In an academic setting, placement and design using all the constraints of the DPL technique can get increasingly difficult. The layer decomposition task is better automated using many proposed layout decomposition EDA tools [29]. To simplify the use of the proposed PDK, we represent each DPL layer with a single color. This results in the gate layer and the first four metal layers being represented using a single color. To simplify further, this PDK does not provide any additional layers for threshold adjustment or a gate cut mask. The proposed PDK's *Back-End-Of-Line* (BEOL) process supports ten layers of metal. The list of key layers is given in Table I.

TABLE I: List of key layers in the proposed PDK.

Layer Name	Drawn Width (nm)	Pitch (nm)
Active	166	32
GATE	20	64*
PG-CG	20	35
SDC	28	40
GC	56	40
IL	24	40
V0	28	36
Metal 1-4	28	36
VM0 5-10	28	36
Metal 5-10	56	72
VM5 5-10	56	72

* Pitch between the gate of two different devices.

B. Single Device Layout and Dimensions

The layout of a single TIGFET is shown in Fig. 5. As discussed earlier, all three gates of the TIGFET are drawn using the same color to represent the gate layer; these are separated later using EDA tools for fabrication of separate PG and CG masks. Vertical strips of polysilicon are patterned uniformly across the chip with a *Contacted Poly Pitch* (CPP) of 44 nm. The gate cut mask generated using the automated EDA tools is used to cut the excess polysilicon from around the active region with a 20 nm extension. Fig. 5 shows the cross-section view of the *Front-End-Of-Line* (FEOL) and *Middle-Of-Line* (MOL) of the proposed predictive process model. Contact to all the gate terminals is made using the *Gate Contact* (GC) layer. Source and drain terminals of the device are connected using *Source Drain Connect* (SDC) layer. Both GC and SDC layers are connected to the first layer of the metal using *Interconnect Layer* (IL). The drain and source terminals of the device have a height and width of 100 nm and 30 nm respectively. The side view of Fig. 5 shows the channel as formed with a maximum stack of four SiNW. Based on the height of the active region, multiple such stacks can be formed with a pitch of 40 nm. Fig. 5 depicts a device with a total of 5 stacks of 4 nanowires. Some of the other key layers are summarized in Table I, along with the drawn width and minimum pitch.

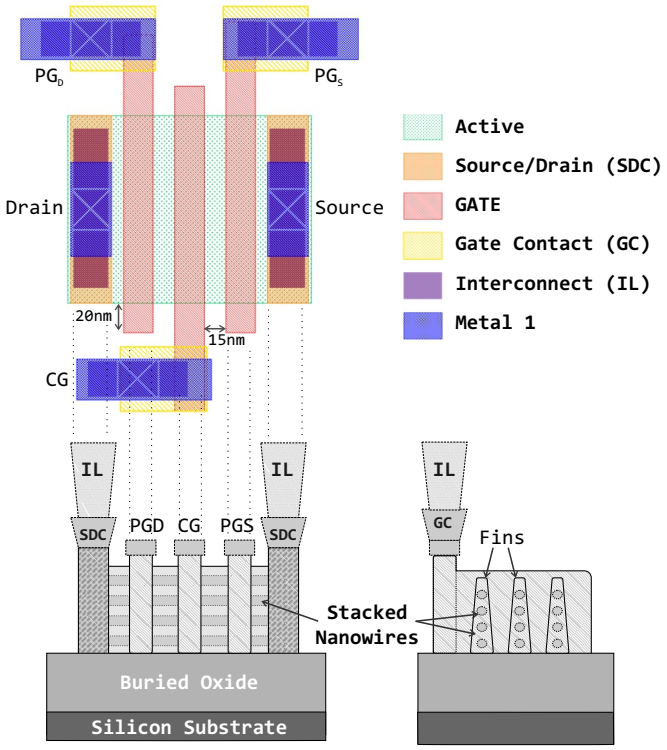

Fig. 5: TIGFET layout and the FEOL/MOL process cross-section.

C. Cell Layout and DTCO Consideration

Meeting fabrication yield and cost targets are particularly challenging tasks when fabricating new semiconductor structures. *Design for Manufacturability* (DFM) and *Design Technology Co-optimization* (DTCO) are widely used techniques to ensure successful device fabrication using novel processes. Using the DTCO approach, manufacturing yield and device density can be improved by customizing the layouts of some widely used structures [24], [30]. In the traditional fabrication processes, the DTCO approach is used for optimizing the highly regular pattern such as an SRAM cell. The SRAM pattern can be carefully tuned using actual manufacturing data allowing tighter tolerance, higher device density, but very few variations in the layout.

In the case of TIGFET-based designs, transistors connected in series (i.e., with shared source and drain contacts) and tied polarity gates are very common, and these are called grouped devices. We use the DTCO approach to optimize the layout of the grouped devices. Fig. 6 shows the schematic and the layout of two grouped TIGFETs. The polarity gates of both devices are shorted together by allowing horizontal routing of the gate layer to the top of the device. The DRC rule for vertical spacing of gates with different potentials is compromised to achieve higher device density. This structure is also very helpful in designing a regular layout using TIGFET devices, as it will be shown in Section V.

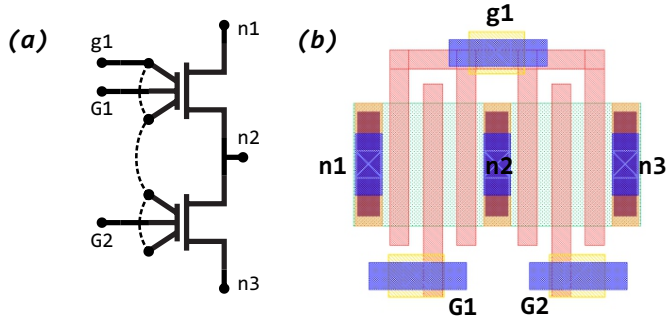

Fig. 6: TIGFET grouped transistors: (a) Schematic; (b) Layout view.

D. Sea-of-Tile Implementation

The enhanced functionality of TIGFETs comes at the cost of two additional gate terminals per device. Using traditional layout and routing methods, the TIGFET-based physical design may not give the best possible results due to the addition of these extra gates. Here, we explore some techniques to mitigate the additional routing complexity. In particular we look at the dual metal power grid routing and then explore the novel layout approach for increasing regularity of the TIGFET-based design, which was first proposed in [31], [32]. At advanced technology nodes, one of the prerequisites for robustness is a layout regularity. This makes the design less sensitive to process variation and improves the yield of fabrication. *Sea-of-Tiles* (SoT) is a fully configurable architecture in which an array of logic tiles are uniformly spread across the chip. A tile is an array of TIGFET devices in which the devices are placed horizontally and adjacent to each other with shorted polarity gates in case they share the same logic on polarity gates. If the devices share the same logic on the control gate, they are aligned vertically with shorted control gates. Based on the number of devices grouped together, many different sizes of tiles are possible. In this work, we will consider $Tile_{G1}$ and $Tile_{G2}$ [32], whose corresponding schematics are shown in Fig. 8 (a) and (b) respectively. Each tile can be configured for different logical operation based on the input provided to its nodes (n1-n6) and gates (g1, g2, G1, and G2). Many other configurations are possible using $Tile_{G2}$, and these are listed in Table II. We implement $Tile_{G1}$ and $Tile_{G2}$ using the proposed design rules in Cadence Virtuoso, as shown in Fig. 8.

E. Grid based Power Routing

A TIGFET device can be configured as a pull-up (*p*-type) network by applying logic 0 to its polarity gates or a pull-down (*n*-type) by applying logic 1. This additional requirement creates a sparse connection of V_{DD}/GND connectivity in the cell. Consequently, traditional power distribution schemes with alternate V_{DD} and GND lines are not efficient. As proposed in [32], we used two metal approach to route power around the cell. Fig. 8 shows the horizontal V_{DD} and vertical GND lines. Comparison of this approach with tradition single metal based power routing has been demonstrated in [31] and shows

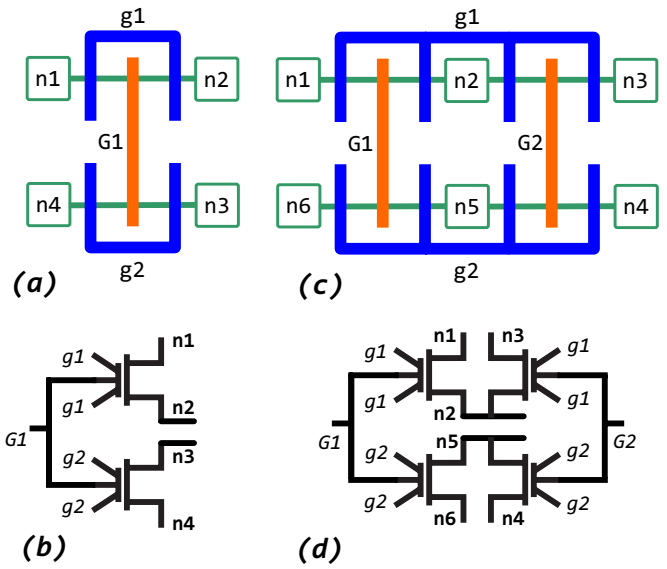

Fig. 7: Logic tiles: (a) $Tile_{G1}$ stick diagram; (b) $Tile_{G1}$ schematic; (c) $Tile_{G2}$ stick diagram; (d) $Tile_{G2}$ schematic.

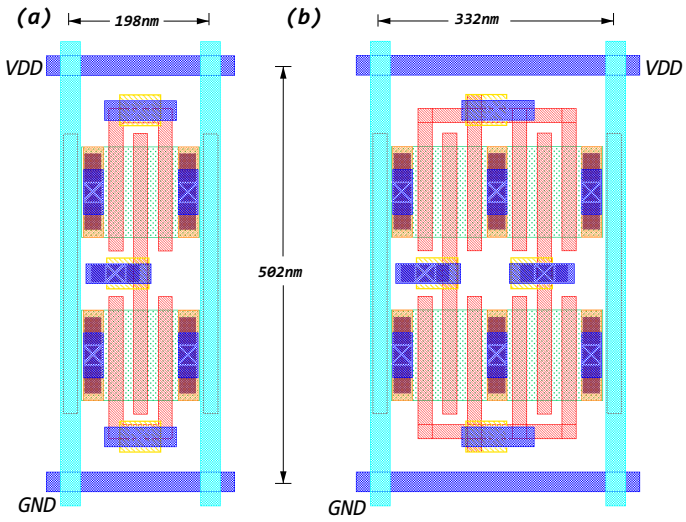

Fig. 8: SoT layout using the proposed PDK: (a) $Tile_{G1}$ (Area=0.10 µm^2); (b) $Tile_{G2}$ (Area=0.17 µm^2).

delay reduction by approximately 28% with minimum routing complexity.

V. PDK Showcases

In this section, we showcase the area benefits of TIGFET technology by presenting two TIGFET compact logic cells designed using the proposed PDK.

A. Compact XOR Cell

Using the higher expressive logic capabilities of the TIGFET device, it is possible to build a compact XOR gate. As illustrated in Fig. 2 (b), a TIGFET-based XOR gate only requires 4 transistors, whereas its CMOS counterpart requires 8 transistors. This compact implementation of a TIGFET-based XOR gate results in an area benefit and leakage power reduction. It is interesting to note that the TIGFET design requires a single device for a pull-up or a pull-down operation, unlike CMOS which requires a series of two transistors. As a result, it reduces the total resistance in the charging and discharging load paths. A TIGFET-based XOR is implemented using $2\times Tile_{G2}$. One is configured as two individual inverters, and another as an XOR gate, as shown in Fig. 2. The complete layout of the CMOS-based XOR gate. The resulting area of the TIGFET-based XOR cell is $0.37\,\mu m^2$, which is 26% smaller than the CMOS implementation which resulted in an area of $0.49\,\mu m^2$. Due to its symmetric structure, the TIGFET-based XNOR has the same area and power benefits.

B. Compact 1-bit Full Adder

We also built a 1-bit full adder using compact TIGFET-based XOR and MAJ logic gates, and compared it to its CMOS counterpart [23]. The layout of the TIGFET ($Area = 0.66\,\mu m^2$) and CMOS-based ($Area = 1.13\,\mu m^2$) full adder are shown in Fig. 10 (a) and (b) respectively. As explained, the richer switching capabilities of TIGFET devices allow them to realize the same CMOS logic function while reducing the number of devices. In the case of the 1-bit full adder, this results in a 41% area reduction.

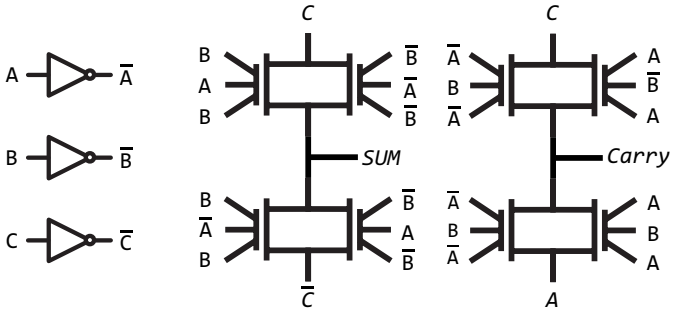

Fig. 9: TIGFET-based compact implementation of a 1-bit full adder.

Similar to the XOR and MAJ gates, various logic functions can be realized by configuring $Tile_{G1}$ and $Tile_{G2}$. Table. II shows the list of functions which can be implemented using SoT approach as well as their respective areas when compared to conventional CMOS gates.

TABLE II: Area comparison of tile-based logic gates implementation.

Logic Gate	Tile	Area TIGFET (µm^2)	Area CMOS (µm^2)
1-bit HA	$2\times Tile_{G2}$	0.34	0.59
XNOR2	$Tile_{G2}$	0.37	0.49
NAND2	$Tile_{G2}$	0.17	0.15
NOR2	$Tile_{G2}$	0.17	0.15
INV	$Tile_{G1}$	0.10	0.10
BUF	$Tile_{G1}$	0.10	0.10

VI. Conclusion

In this paper, we proposed a predictive PDK for a 10 nm-diameter SiNW TIGFET. The design kit is derived using

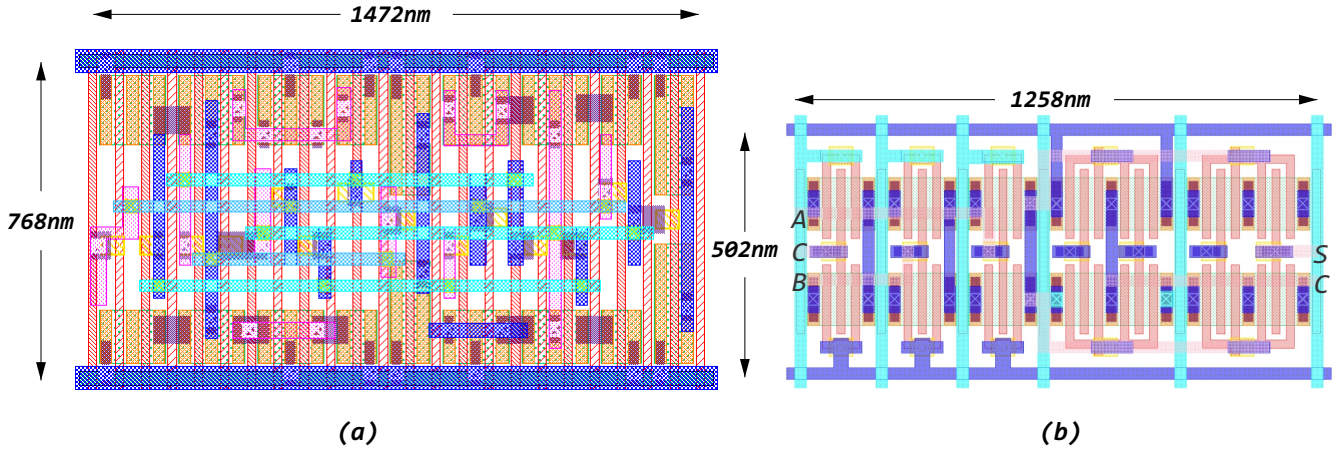

Fig. 10: Layout view of a full adder: (a) CMOS; (b) TIGFET.

TCAD simulations and realistic assumptions made for large-scale production of TIGFET-based systems. We detailed key assumptions made while designing this PDK. Consequently, we derived the set of design rules for physical design in Cadence® Virtuoso. Using the TIGFET PDK, we evaluated previously proposed grouped transistor and grid-based power-line distribution techniques to optimize physical design and mitigate added routing overhead introduced because of additional terminal of TIGFETs. We validated the design rules by implementing an XOR and a 1-bit full adder, and compared those with the FreePDK15nm™ CMOS process, which shows 26% and 41% area reduction respectively. The open source nature of this PDK [17] will allow researchers to evaluate the area, delay and power of TIGFET-based designs systematically.

Acknowledgments

This work was supported by the NSF Career Award number 1751064, and the SRC Contract 2018-IN-2834.

References

[1] Y. Cui *et al.*, *High Performance Silicon Nanowire Field Effect Transistors*, Nano Letters, 3(2): 149-152, 2003.
[2] J.P. Colinge, *FinFET and other multigate transistors*, Springer, 2007.
[3] S. Sutar *et al.*, *Graphene p-n junctions for electron-optics devices*, DRC, 2013.
[4] M. De Marchi *et al.*, *Polarity control in double-gate, gate-all-around vertically stacked silicon nanowire FETs*, IEDM, 2012.
[5] A. Heinzig *et al.*, *Reconfigurable silicon nanowire transistors*, Nano Letters, 12(1): 119-124, 2011.
[6] S. Rai *et al.*, *Emerging reconfigurable nanotechnologies: can they support future electronics?* , ICCAD, 2018.
[7] Jorge Romero-Gonzlez *et al.*, *BCB Evaluation of High-Performance and Low-Leakage Three-Independent-Gate Field-Effect Transistors*, JXCDC, 2018.
[8] J. Trommer *et al.*, *Reconfigurable nanowire transistors with multiple independent gates for efficient and programmable combinational circuits*, DATE, 2016.
[9] L. Mathew *et al.*, *Multiple Independent Gate Field Effect Transistor (MIGFET) Multi-Fin RF Mixer Architecture, Three Independent Gates (MIGFET-T) Operation and Temperature Characteristics*, VLSI Technology, 2005.
[10] S. Rai *et al.*, *Designing Efficient Circuits Based on Runtime-Reconfigurable Field-Effect Transistors*, in IEEE TVLSI, 27(3): 560-572, 2019.
[11] M. H. Ben-Jamaa *et al.*, *An Efficient Gate Library for Ambipolar CNTFET Logic*, IEEE TCAS, 30(2): 242-255, 2011.
[12] J. Zhang *et al.*, *Configurable Circuits Featuring Dual-Threshold-Voltage Design With Three-Independent-Gate Silicon Nanowire FETs*, IEEE TCAS I, 61(10): 2851-2861, 2014.
[13] E. Giacomin, *et al.*, *Low-Power Multiplexer Designs Using Three-Independent-Gate Field Effect Transistors*, NanoArch, 2017.
[14] J. Romero-Gonzalez, *et al. An Efficient Adder Architecture with Three-Independent-Gate Field-Effect Transistors*, ICRC, 2018.
[15] X. Tang *et al.*, *TSPC Flip-Flop Circuit Design with Three-Independent-Gate Silicon Nanowire FETs*, ISCAS, 2014.
[16] E. Giacomin *et al.*, *Differential Power Analysis Mitigation Technique Using Three-Independent-Gate Field Effect Transistors*, VLSI-SoC, 2018.
[17] A 10-nm TIGFET PDK. [Online], 2019. https://github.com/LNIS-Projects/TIGFET-10nm-PDK
[18] Bhanushali, *et al.*, *FreePDK15: An Open-Source Predictive Process Design Kit for 15nm FinFET Technology*, ISPD, 2015.
[19] J. Zhang *et al.*, *A Schottky-Barrier Silicon FinFET with 6.0mV/dec Subthreshold Slope over 5 Decades of Current*, IEDM, 2014.
[20] G. V. Resta *et al.*, *Polarity Control inWSe2Double-Gate Transistors*, Scientific Reports, 6, 2016
[21] J. Zhang *et al.*, *Polarity-Controllable Silicon Nanowire Transistors with Dual Threshold Voltages*, IEEE TED, 61(11): 3654-3660, 2014.
[22] J. E. Stine *et al.*, *FreePDK: An open-source variation- aware design kit*, IMSE, 2007.
[23] M. Martins *et al.*, *Open Cell Library in 15nm FreePDK Technology*, ISPD, 2015.
[24] L.T. Clark *et al.*, *ASAP7: A 7-nm FinFET Predictive Process Design Kit*, Microelectronics Journal, 53: 105-115, 2016.
[25] E. Giacomin *et al.*, *A Resistive Random Access Memory Addon for the NCSU FreePDK 45nm*, IEEE TNANO, 18(1): 68-72, 2018
[26] Finders *et al. Double patterning lithography: The bridge between low k1 ArF and EUV* Microlithography World.
[27] K. Yuan *et al.*, *Double Patterning Layout Decomposition for Simultaneous Conflict and Stitch Minimization*, IEEE TCAD, 29(2): 185-196, 2010.
[28] DZ Pan *et al.*. *Layout optimizations for double patterning lithography* ASICON, 2009.
[29] A. B. Kahng *et al.*, *Layout decomposition for double patterning lithography*, ICCAD, 2008.
[30] J. Ryckaert, *et al.*, *DTCO at N7 and beyond: patterning and electrical compromises and opportunities*, Proc. SPIE9427, 2015.
[31] O. Zografos *et al.*, *Novel grid-based power routing scheme for regular controllable-polarity FET arrangements*, ISCAS, 2014.
[32] S. Bobba *et al.*, *Process/design co-optimization of regular logic tiles for double-gate silicon nanowire transistors*, NanoArch, 2012.