Nanoscale Three-Independent-Gate Transistors: Geometric TCAD Simulations at the 10 nm-Node

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***Abstract*—Three-Independent-Gate Field-Effect Transistors (TIGFETs) are Schottky-barrier-based devices which can be reconfigured to be either *n*- or *p*-type allowing for innovative compact logic gate implementations. In this paper, we present an aggressively scaled 10 nm gate-all-around silicon-nanowire TIGFET device evaluated with *Synopsys Sentaurus* at a 0.7 V nominal supply voltage as typically used at this technology node. When considering a pure silicon channel, the maximum TCAD simulated current drive is 90.20 μA/μm and 89.25 μA/μm for *n*- and *p*-type operation respectively, and these simulations are verified using device physics calculations. In order to achieve higher current drives, we also consider a germanium-nanowire device which results in current drives more than 14$\times$ higher compared to the silicon-nanowire devices, thus making TIGFET devices competitive with FinFET technology at the 10 nm node.**

I. Introduction

Conventional drive in the semiconductor industry has been based on the improvement of device performance and the scaling of these devices, as exemplified by Moore's scaling law which pushes for the doubling of transistors in a given integrated circuit every two years. However, as the physical sizing limits of contemporary manufacturable transistors are being reached, Moore's law is coming to an end and innovations on standard *Fin Field-Effect Transistor* (FinFET) technology are necessary.

Reconfigurability refers to the ability of a single transistor to alternate between *n*-type and *p*-type behaviors post-fabrication. Devices built based on this principle are a viable alternative to scaling due to their ability to enhance system functionality by simplifying logic gate implementations [1], [2]. The *Three-Independent-Gate Field Effect Transistor* (TIGFET) is an experimentally demonstrated reconfigurable device [3]–[5] whose dual-switching ability originates from electrostatic modulation of Schottky barriers at the source and drain contacts using additional gate terminals called *Polarity Gates*.

This paper introduces TCAD simulations performed using *Synposys Sentaurus* for 10 nm-gate TIGFET silicon-nanowire and germanium-nanowire devices designed to operate at the industry standard supply voltage V_{DD} of 0.7 V. These simulations are intended to verify TIGFET device performance at the 10 nm node, thus defining the device's validity for use alongside contemporary devices.

The maximum TCAD simulated current drive for the silicon-nanowire design at the 0.7 V supply voltage is 90.20 μA/μm and 89.25 μA/μm for *n*- and *p*-type operation respectively. In order to boost the current drive of the TIGFET devices while maintaining the low supply voltage, a germanium-nanowire was simulated. This resulted in current drives approximately 14$\times$ higher than the current drives in the silicon-nanowire simulations. The germanium-nanowire simulation current drive results are competitive with those seen for 10 nm FinFET devices.

The rest of the paper is organized as follows: Section II discusses the operation and theory of the TIGFET device; Section III provides an overview of the TCAD simulations for the silicon-nanowire and the germanium-nanowire devices and discusses the validity of the results using device physics calculations; finally, Section IV discusses the significance of and contribution provided by this work.

II. TIGFET Operation

Standard technology such as FinFETs and their predecessors planar MOSFETs require doping to control the ambipolarity of carriers in the channel and thus select either *n*-type (electron) or *p*-type (hole) carriers to be dominant. TIGFETs exploit this ambipolarity instead of suppressing it, through their modulatation of the Schottky barriers at the *Polarity Gates* (PGs). This is done both due to the increasing challenge of doping at smaller nodes and to create devices which can be reconfigured from *n*-type to *p*-type and vice versa post-processing [7]. The lack of doping and resulting simplicity of their fabrication also makes it possible to fabricate TIGFET devices on the same chip and concurrently with existing technologies.

A TIGFET device requires a channel made of a semiconductor material, metallic source and drain contacts, and three gate electrodes: the *Control Gate* (CG), and two symmetric PGs at the source and drain to act as electrostatic doping means at the Schottky barrier interfaces. The device structure is illustrated in Fig. 1.

TABLE I: Gate Biases for Different TIGFET Configurations

Dominant carrier	**Device State**	**Applied Potentials**		
		V_{PG_S}	V_{CG}	V_{PG_D}
n-type	OFF	V_{DD}	0 V	V_{DD}
	ON	V_{DD}	V_{DD}	V_{DD}
p-type	OFF	0 V	V_{DD}	0 V
	ON	0 V	0 V	0 V

Fig. 2 shows a band diagram of combined *n*- and *p*-type operation at equilibrium; Table I summarizes the TIGFET

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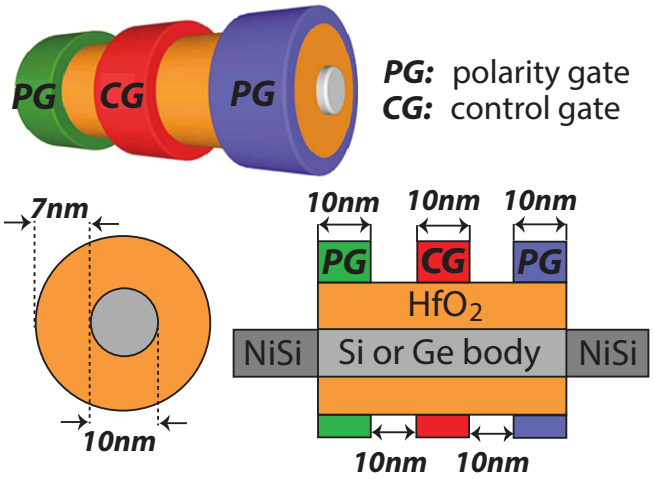

Fig. 1: The structure of the simulated device with 10 nm gate lengths and spacings. The channel material is set to either silicon (Si) or germanium (Ge) with nickel silicide (NiSi) serving as the Schottky-barrier material. Hafnium dioxide (HfO_2) is selected as the gate dielectric material.

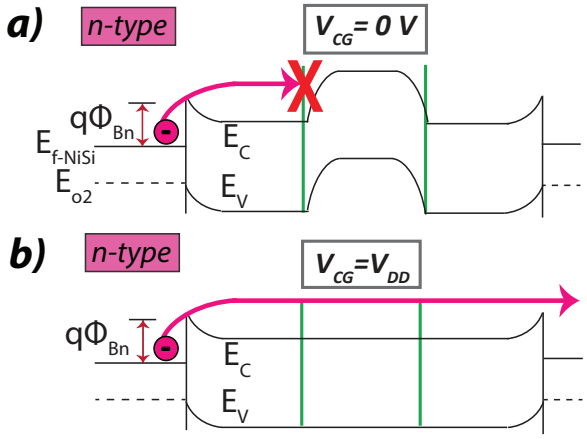

Fig. 3: Band diagrams of a TIGFET device operating in the $n-$configuration. Note that V_{DS} is assumed applied in these band diagrams for carrier conduction to occur; the resulting band bending is omitted for simplicity. (a) When V_{CG} = 0 V the OFF condition occurs, blocking the electron-carrier flow. (b) When V_{CG} = V_{DD} the ON condition occurs, allowing the electron-carrier flow.

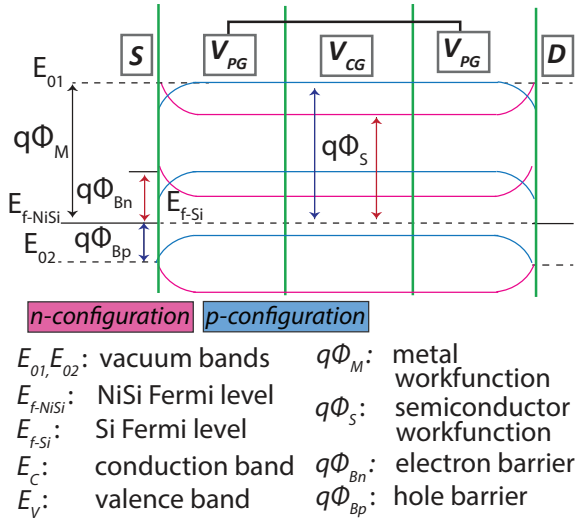

Fig. 2: Band diagram of a TIGFET device assuming the same bias for both polarity gates. Pink bands correspond to $n-$type operation, V_{PG}=V_{DD} and blue bands correspond to $p-$type operation, V_{PG}= 0 V at equilibrium (no V_{GS} applied).

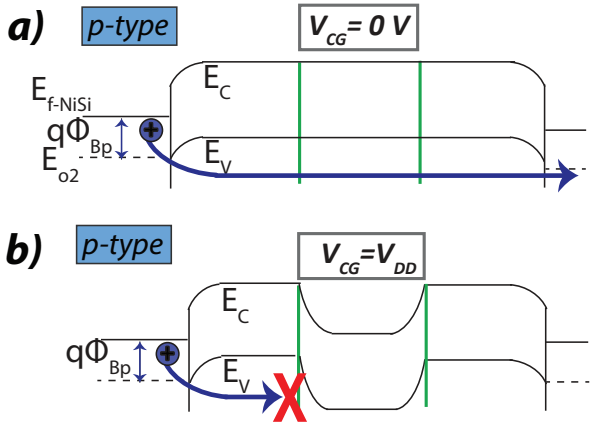

Fig. 4: Band diagrams of a TIGFET device operating in the $p-$configuration. Note that V_{DS} is assumed applied in these band diagrams for carrier conduction to occur; the resulting band bending is omitted for simplicity. (a) When V_{CG}= 0 V the ON condition occurs, allowing the hole-carrier flow. (b) When V_{CG}= V_{DD} the OFF condition occurs, blocking the hole-carrier flow.

device operation. The chosen PG voltages determine which carriers will dominate in the channel: if the PGs are increased to the supply voltage, the device will be *n*-type (electron) carrier-dominated, as seen in Fig. 3, whereas if the PGs are grounded, the device will be *p*-type (hole) carrier-dominated, as seen in Fig. 4. The state of the CG determines whether the selected carriers will pass through, thus effectively turning the device on or off.

III. Overview of the TCAD Simulations

This section develops the assumptions made in the *Synopsys Sentaurus* TCAD simulations. Current conduction is approximated using the *Fermi Physics Package* in this software.

A. Silicon-nanowire Device Simulations

The Schottky barrier in the TCAD simulations was created by a *Nickel Silicide* (NiSi)-to-semiconducting material contact. NiSi is a mid-gap metal and can thus provide symmetric

switching between *n*- and *p*-type carriers. The nanowire configuration was chosen due to its superior electrostatic control over the channel when compared to FinFET technology at the same node [6]. A 7 nm *Hafnium Dioxide* (HfO_2) layer was used as the gate dielectric. Fig. 1 shows the simulated device structure.

Modifications specific to the silicon-nanowire structure were made. These include elevating the *p*-type body doping to $1 \cdot 10^{16}$ cm^{-3}, and the assumption of strained $\langle 111 \rangle$ silicon, edited to effectively make *p*-type carriers 81% faster and *n*-type carriers 58% faster. The NiSi workfunction used in the silicon-nanowire simulation was 4.755 eV, and the corresponding silicon semiconductor work function was 4.59 eV.

Symmetric maximum current drives are achieved at the maximum supply drive of V_{DD} = 0.7 V for *n*- and *p*-configurations, as seen in Fig. 5. The maximum current drive for *n*-type operation is 90.20 μA/μm and for *p*-type is 89.25 μA/μm. Thanks to the Schottky barrier cutoff, I_{OFF} is extremely low at 3.3 nA/μm and 1.16 nA/μm for *n*- and *p*-type operation respectively.

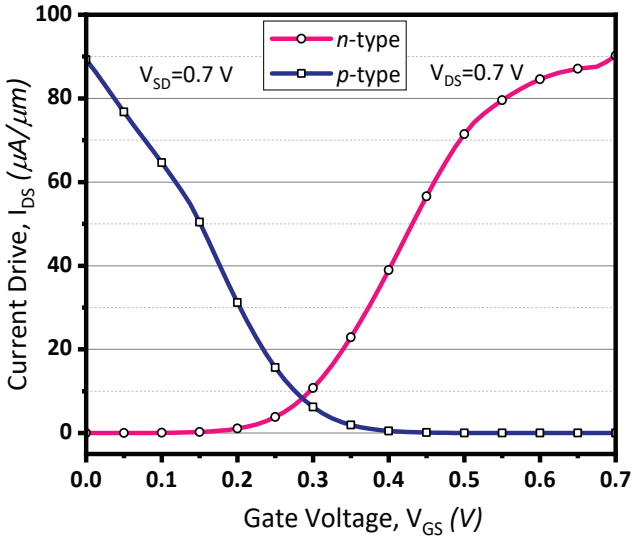

Fig. 5: I_D-V_{GS} characteristics of the silicon-nanowire device at V_{DD}= 0.7 V.

The current drives are much lower for these 10 nm silicon-nanowire simulations compared to the previously published 22 nm TIGFET circuit model [4], The main reason for this is the lowering of the supply voltage from 1.2 V to 0.7 V as is now required for the 10 nm node. However, an improvement is seen in the $<$1% asymmetry between n-type and p-type operation in these 10 nm simulations when compared to the 22 nm TIGFET simulations which exhibited almost 10% asymmetry. This symmetry in current drive as well as the symmetric switching seen at approximately 0.3 V means that neither $n-$ and $p-$type conduction will dominate, as is desired for a well-designed reconfigurable device.

Assuming a diameter of 10 nm and the values in Table II, calculations using the standard Eq. (1) for determining the

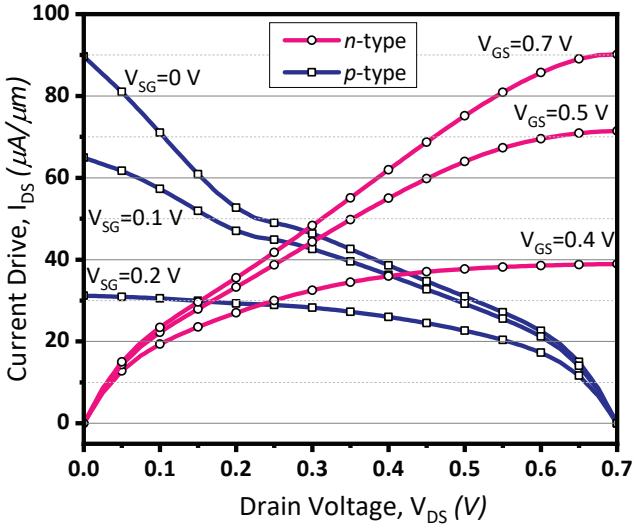

Fig. 6: I_D-V_{DS} characteristics of the silicon-nanowire device. Punchthrough effects are seen for the PMOS curves at V_{SD}= 0, 0.1.

maximum current at the Schottky barriers are performed to determine the validity of these simulated results [8]:

$$J_{ms} = \left(\frac{4\pi m^* q k^2}{h^3}\right) \cdot T^2 \cdot e^{\frac{-q \cdot \phi_{Bp}}{kT}} \cdot \left(e^{\frac{-q \cdot V_{DD}}{kT}} - 1\right). \quad (1)$$

Note that the maximum current is taken to be at the supply voltage, V_{DD}.

This results in a calculated maximum current drive of 196.21 μA/μm which is approximately 2$\times$ the simulated maximum current drive for these devices. This difference is due to Eq. (1) calculating the theoretical current limit of a single Schottky barrier, whereas the simulated TIGFET device consists of two Schottky barriers as well as the standard $p-n$ junctions associated with the CG.

Fig. 6 shows the current drive as a function of drain voltage for the *n*- and *p*-configurations. Symmetric characteristics are

TABLE II: Device Physics Assumptions [8], [9]

	Silicon-nanowire	Germanium-nanowire
Semiconductor electron affinity, χ_s	4.05 eV	4.00 eV
Semiconductor bandgap, E_g	1.12 eV	0.66 eV
Semiconductor doping density, N_A	$1 \cdot 10^{16}$ cm^{-3}	$1 \cdot 10^{14}$ cm^{-3}
Semiconductor intrinsic concentration, n_i	$9.65 \cdot 10^{9}$ cm^{-3}	$2.4 \cdot 10^{13}$ cm^{-3}
Semiconductor workfunction, ϕ_s	4.59 eV	4.13 eV
Semiconductor permittivity, ϵ_s	11.9	16
Effective electron masses, m_t	0.19	0.082
Effective hole masses, m_{lp}	0.16	0.04
Metal workfunction, ϕ_m	4.755 eV	4.46 eV
Operating temperature, T	300 K	

seen for both *n*-type and *p*-type carriers, with the switching centered around V_D= 0.3 V. Saturation is seen for all *n*-type configuration and punchthrough is seen for the device biased *p*-type at V_{sg}= 0 V and 0.1 V. Punchthrough occurs in short-channel devices such as this simulation due to the simulated depletion regions of the source and drain reaching each other which in turn lowers the potential and facilitates current flow near the surface of the device.

B. Germanium-nanowire Device Simulations

A germanium-nanowire 10 nm TIGFET simulation is considered as a higher-current alternative to the silicon-nanowire. The metal and semiconducting workfunctions used are 4.46 eV and 4.13 eV, respectively. As seen in Fig. 7, the maximum current drive achieved with this simulation is 1289.18 μA/μm for *n*-type operation and 1272.65 μA/μm for *p*-type operation. Eq. (1) is evaluated for the germanium-nanowire and results in a maximum expected current drive of 1990.65 μA/μm, which is on the same scale as our simulations. The trade-off for this 14$\times$ drive current improvement over the silicon-based simulations are I_{OFF} values of 7.51 μA/μm for $n-$type, and 4.52 μA/μm for $p-$type operation. The simulated germanium-nanowire TIGFET current drive is on the same scale as 1550 μA/μm, the reported current drive for modern FinFET technology [10].

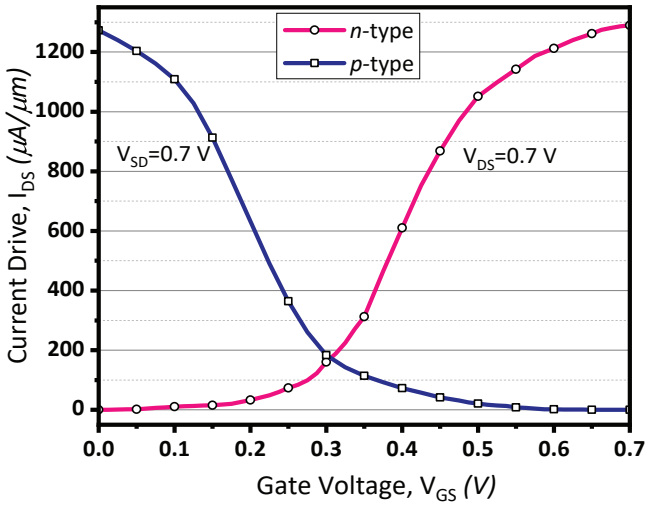

Fig. 7: I_D-V_{GS} characteristics of the germanium-nanowire device at V_{DD}= 0.7 V.

IV. Conclusion

This work presents TCAD simulations for silicon-nanowire and germanium-nanowire gate-all-around TIGFET devices with aggressively scaled 10 nm gate length and gate spacings. The supply voltage used in these simulations was the industry standard of 0.7 V so as to allow for a fair comparison to contemporary 10 nm node FinFET designs which are run at this voltage. The maximum TCAD simulated current drive for the silicon-nanowire design at the 0.7 V supply voltage is 90.20 μA/μm and 89.25 μA/μm for *n*- and *p*-type operation respectively. The germanium-nanowire device was simulated in order to boost the current drive of the TIGFET devices while maintaining the required low supply voltage. This resulted in current drives of 1289.18 μA/μm for *n*-type operation and 1272.65 μA/μm for *p*-type operation which are approximately 14$\times$ higher than the current drives in the silicon-nanowire simulations. The maximum current drives extracted from the *I-V* characteristics were shown to match up well with device physics calculations for the expected Schottky barrier current drives.

The trade-off between the two simulated devices is that the silicon-nanowire configuration is able to achieve extremely low off current, I_{OFF} thanks to the cut-off provided by the Schottky barrier, while the germanium-nanowire configuration has higher I_{OFF} values. Both designs enable different uses: a silicon-nanowire TIGFET device would be useful in low-power applications where small operation voltages and leakage currents are necessary for reducing power consumption, and a germanium-nanowire TIGFET could be used alongside contemporary FinFET technology which has similar ON currents to those seen in our simulations [10]. By providing both of these simulations and comparing their benefits, this paper has established that the TIGFET is a competitive alternative device at the 10 nm node in both material sets.

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