CdMgTe as an Electron Reflector for MgZnO/CdSeTe/CdTe Solar Cells

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***Abstract* — CdMgTe with a 1.8-eV band gap was deposited at the back of MgZnO/CdSeTe/CdTe superstrates to create a conduction band barrier and reduce back surface recombination. To minimize $CdCl_2$ passivation loss, substrate preheat time was varied. Photoluminescence, carrier lifetime, and quantum efficiency showed improvement with shorter preheat and secondary ion mass spectrometry profiles showed retention of $CdCl_2$ passivation for short CdMgTe preheat. An HCl acid etch treatment and CdTe cap layer were incorporated independently after the CdMgTe on additional devices to minimize magnesium oxidation and the CdTe cap device showed initial promise with device efficiency reaching 13.1%.**

***Index Terms* — CdMgTe, electron reflector, CdTe, CSS.**

I. Introduction

Cadmium telluride (CdTe) photovoltaics have made significant progress in the last decade; cell efficiencies reached a record 22% [1] and costs have become competitive with silicon and fossil fuel technologies [2]. However, efficiencies are significantly lower than the theoretical limit for CdTe due primarily to low open circuit voltage (V_{oc}) [3]-[4]. One proposed method to overcome the voltage deficit is to incorporate a high band gap material at the back of the thin-film structure. Modeling shows that this creates a conduction band barrier and reduces back surface recombination by reflecting photoelectrons and forward-current electrons away from the rear surface [3], [5]. Cadmium magnesium telluride ($Cd_{1-x}Mg_xTe$) is well-suited for this layer because it has a higher band gap than CdTe and can be deposited quickly by close-space sublimation (CSS) [3].

Previous work to incorporate CdMgTe as an electron reflector (ER) demonstrated limited success due to certain challenges presented by the material: cadmium-chloride ($CdCl_2$) passivation loss and magnesium-oxide (MgO) formation at the CdMgTe surface [2]-[4]. $CdCl_2$ passivation of the CdTe absorber is a critical step in producing efficient photovoltaic devices. In past work this passivation step was done post-CdMgTe deposition due to high substrate temperatures during CdMgTe fabrication [6]. However, post-CdMgTe passivation stripped Mg from grain boundaries and introduced unfavorable oxidation at the CdMgTe surface. Oxidation was addressed by depositing a thin CdTe layer, or CdTe cap, on the CdMgTe [3]. Use of a CdTe cap on a CdS/CdTe/CdMgTe structure produced the best results for CdTe with a CdMgTe ER to date [3].

This work explores the incorporation of CdMgTe in a new CdTe superstrate configuration. We investigate lower substrate temperatures to determine whether $CdCl_2$ passivation can be better maintained compared to previous work where passivation was reversed due to substrate temperatures above 400°C [6]-[7]. This work presents the effects of lower CdMgTe substrate temperature on film and device characteristics, preliminary data on an HCl acid etch treatment, and demonstrates respectable device efficiencies with a CdTe cap.

II. Experiment

A. Device Fabrication

Four different structures were designed to study the effect of different CdMgTe fabrication methods on device properties and performance. All structures were fabricated with a MgZnO window layer as described in [8]. The absorber was 0.5-µm cadmium selenium telluride (CdSeTe) and 1.0-µm CdTe fabricated with no intentional interdiffusion between the CdSeTe and CdTe layers. This absorber was chosen because it increases device current [8] and is unexplored for CdMgTe ER applications. CdSeTe/CdTe was deposited on the MgZnO by CSS using a fully-automated single-vacuum deposition system [9]. The cell shown in Fig. 1(a) was used as a reference for comparison to devices with CdMgTe. The reference cell received an optimized $CdCl_2$ treatment followed by an evaporated 40-nm Te layer [10].

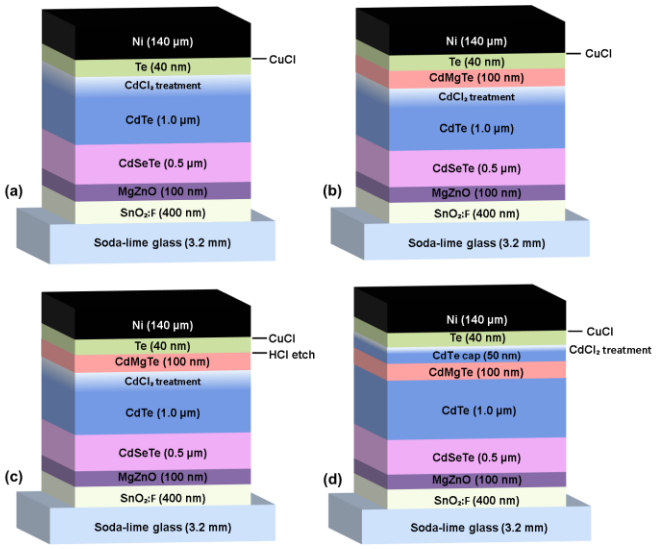

Fig. 1. Device structure for (a) the standard CdSeTe/CdTe reference cell, (b) CdMgTe devices fabricated with varied preheat time, (c) CdMgTe devices treated with an HCl acid etch, and (d) CdMgTe devices with a CdTe cap layer.

The devices with CdMgTe but no HCl etch or CdTe cap, shown in Fig. 1(b), received the optimized $CdCl_2$ treatment of the absorber before the CdMgTe film was deposited. The 100-nm, 1.8-eV CdMgTe layer was deposited by co-sublimation of Mg and CdTe in a separate CSS chamber in an argon environment with <0.01% O_2 to minimize oxidation [4]. Before CdMgTe deposition the substrates were preheated for 30, 60, 90, 120, 150, and 180 seconds where 60, 90, and 180 seconds correspond to substrate temperatures of 275, 350, and 480°C respectively. After CdMgTe deposition 40 nm of Te was evaporated onto the substrates.

The device shown in Fig. 1(c) was fabricated through the CdMgTe layer with a short CdMgTe preheat time. After deposition the CdMgTe received a 5-second HCl acid etch of 10% HCl solution in deionized water to remove oxides from the surface [11] which was followed immediately by 40-nm Te deposition.

For devices with CdMgTe and a CdTe cap, shown in Fig. 1(d), the 100-nm CdMgTe was fabricated directly onto as-deposited CdSeTe/CdTe with substrate preheat times of 60 and 120 seconds. A 50-nm CdTe cap was immediately deposited on the CdMgTe followed by the $CdCl_2$ treatment and 40-nm evaporated Te layer.

All devices were doped with Cu and completed with a 140-µm colloidal Ni paint layer. 25 small-area devices were delineated on each superstrate with areas of ~0.6 cm^2.

B. Characterization

Transmittance was measured on CdMgTe films and band gaps were determined using the Tauc plot method; $(\alpha h\upsilon)^2$ was plotted against photon energy, $h\upsilon$, and the linear portion of the $(\alpha h\upsilon)^2$ curve was fit and extrapolated to the x-axis [12]. External quantum efficiency (QE) and current-density versus voltage (J-V) were measured under standard test conditions, where the J-V light source was a xenon arc lamp at AM1.5 illumination. Room-temperature photoluminescence emission spectroscopy (PL) was measured from the glass side of completed devices with an excitation laser wavelength of 520 nm and a 570-nm long pass filter to minimize any signature from the excitation source. Single-photon time-resolved photoluminescence (TRPL) was also measured from the glass-side of completed devices with an excitation wavelength of 640 nm, average injection power of 0.06 mW, 1.1 MHz repetition rate, and beam diameter of 0.3 mm. TRPL emission was measured using a 870-nm centered bandpass filter. Time-of-flight secondary ion mass spectrometry (SIMS) profiles were measured with a 30 keV primary ion beam and a thermal ionization cesium sputtering source operated in positive mode to look at both electro-positive and electro-negative species on structures without Ni back contacts.

PL, TRPL, and QE were measured on devices with all preheat times, although data are reported as short, medium, and long preheat treatments corresponding to 30, 90, and 180 seconds respectively for clarity. All trends discussed hold for the full set of preheat times.

III. Results and Discussion

A. Benefits of a Short CdMgTe Preheat Treatment

Transmittance was measured on CdMgTe films with varied preheat times to verify that the band gap remained between 1.7 and 1.8 eV. Fig. 2 shows the calculated band gap as a function of preheat time; variation is limited and well within the desired range for CdMgTe to be used as an ER for CdSeTe/CdTe.

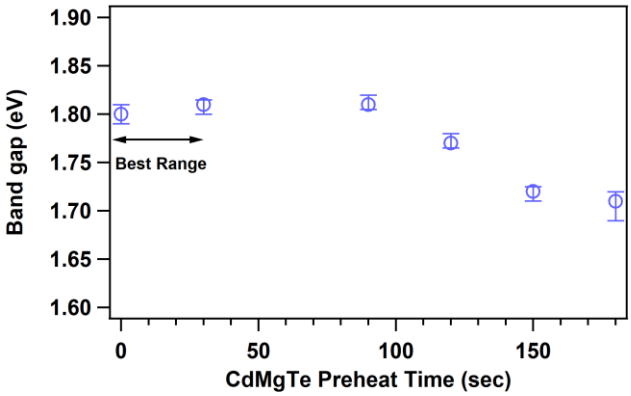

Fig. 2. Band gap as a function of CdMgTe preheat time calculated from transmittance measurements.

Fig. 3 shows PL measured on the device structure in Fig. 1(b) for short, medium, and long preheat treatments. There is no discernable peak in PL for long preheat treatments, a more notable peak for the medium preheat, and a significant increase for the shortest CdMgTe preheat time. Since the PL excitation laser probes ~0.2 µm into the absorber where $CdCl_2$ passivation effects are significant and PL emission is known to disappear for poor or no $CdCl_2$ passivation (as demonstrated in the Fig. 3 inset), the increase in PL with shorter preheat is likely due to improved retention of $CdCl_2$. This supports previous experiments in which transmission electron microscopy showed Cl driven out of passivated absorbers for substrate temperatures above 400°C during CdMgTe deposition [4], [6].

TRPL was measured on the same set of devices, and the normalized TRPL decays are shown in Fig. 4. The data show a clear trend that with decreasing CdMgTe preheat time the TRPL tail lifetime (τ_2) increases. Both τ_2 and PL intensity trends with CdMgTe preheat are compared in Fig. 5 where τ_2 was determined by fitting the tail of the TRPL decay data with an x-offset exponential function. The lifetimes for the short preheat times are considerably larger than that of the reference device.

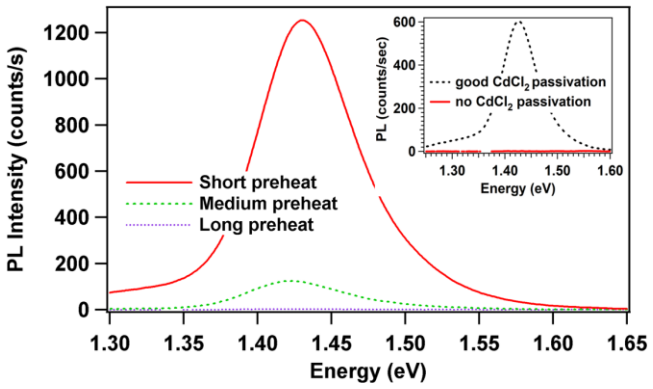

Fig. 3. PL emission shows improvement for shorter CdMgTe preheat times. $CdCl_2$ passivation significantly impacts PL signal.

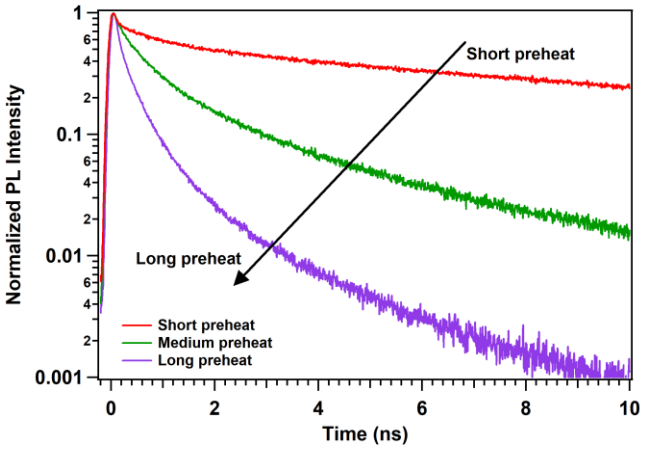

Fig. 4. TRPL decays show better lifetimes for shorter CdMgTe preheat treatments.

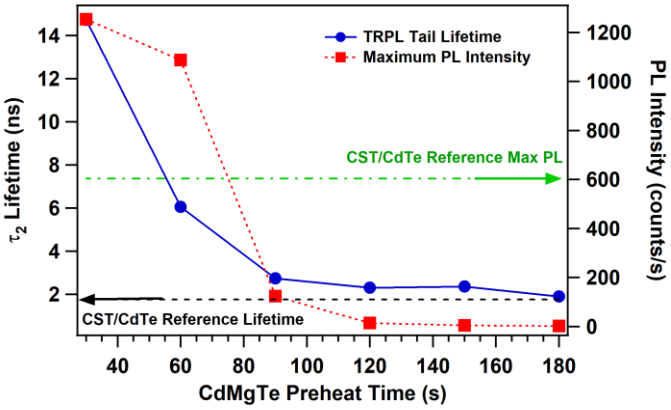

Fig. 5. Maximum PL intensity and TRPL tail lifetimes show a steady decline for longer CdMgTe preheat treatments. The reference sample PL and TRPL lifetimes are given for comparison.

TRPL simulations have shown that τ_2 lifetimes correspond to bulk recombination in CdTe photovoltaic devices [13]-[14], therefore, the improvement in τ_2 for shorter CdMgTe preheat treatment suggests an improvement in bulk properties. Since $CdCl_2$ passivation is known to improve CdTe bulk properties [15]-[16] and τ_2 lifetimes [17]-[18], τ_2 improvement may be indicative of $CdCl_2$ passivation retention in shorter preheat devices.

Fig. 6 shows device QE for various CdMgTe preheats. QE response was poor for devices with long preheat, especially in the low to mid-wavelength range, suggestive of $CdCl_2$ passivation loss. For medium and shorter preheat treatments, the QE improved across the full wavelength range which indicates retention of $CdCl_2$ passivation.

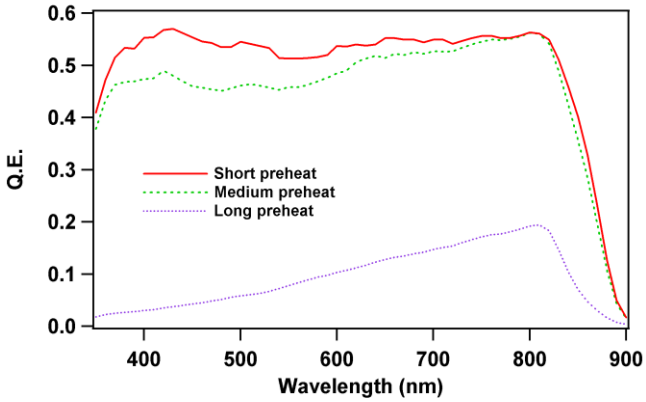

Fig. 6. QE shows improvement with shorter CdMgTe preheat treatments.

TOF-SIMS was measured on samples with a short and long CdMgTe preheat treatment as well as the reference sample to understand the effects of CdMgTe preheat time on Cl passivation and CdMgTe deposition properties. The reference-sample sputter time has been offset from zero to align the absorber regions of the samples and to highlight the CdTe/CdMgTe interface. Fig. 7(a) shows the Cl SIMS profiles of the short and long CdMgTe preheat treatments and CdSeTe/CdTe reference. The small spike in Cl signal at the CdTe/CdMgTe interface is due to residual Cl buildup despite a deionized water rinse after $CdCl_2$ deposition.

For a short CdMgTe preheat the Cl signal is comparable to that of the reference throughout the absorber, whereas for a long CdMgTe preheat it is notably lower. This verifies the initial interpretation of PL, TRPL, and QE measurements: short CdMgTe preheat treatments can be used to maintain $CdCl_2$ passivation whereas long CdMgTe preheat treatments will remove Cl from the absorber, reversing $CdCl_2$ passivation. Therefore, a short preheat treatment is an effective technique for maintaining $CdCl_2$ passivation during CdMgTe deposition.

Fig. 7(b) shows Mg SIMS profiles on the same sample set. For both preheat treatments there is a clear increase in Mg at the back compared to the reference, which indicates proper deposition of the CdMgTe independent of preheat treatment. Mg diffusion from the CdMgTe layer into the absorber occurs for both preheat treatments due to the temperature of the

substrate during deposition. The diffusion is more extensive throughout the absorber for the long CdMgTe preheat treatment due to the higher temperature of the substrate before CdMgTe deposition.

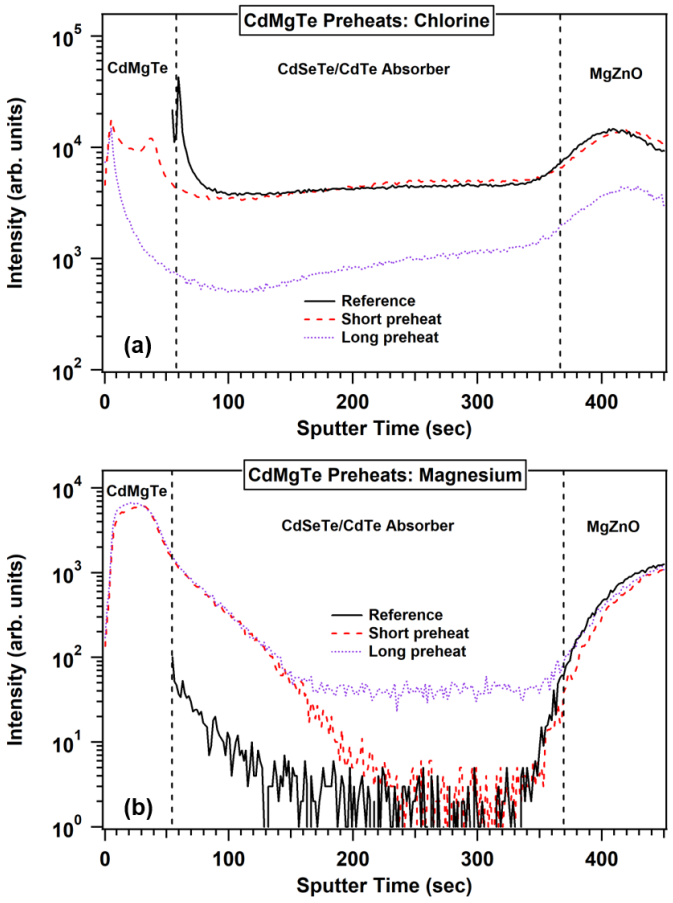

Fig. 7. (a) Cl SIMS profiles show retention of Cl and a decrease in Cl throughout the absorber for short and long CdMgTe preheats respectively. (b) Mg SIMS profiles show Mg at the back of CdMgTe samples and that diffusion of Mg occurs to different extents for short and long preheats

Despite good PL emission and τ_2 lifetimes, definitive deposition of CdMgTe at the back, and maintenance of $CdCl_2$ passivation, devices with short CdMgTe preheat treatment showed only fair J-V characteristics. This is likely due to poor interfaces at the back of the structure although determination of the cause is ongoing.

B. HCl Etch of CdMgTe on CdSeTe/CdTe Absorbers

J-V comparison of the HCl-etched sample in Fig. 1(c) and the CdSeTe/CdTe reference sample is shown in Fig. 8. The CdMgTe/HCl etch device shows a notable reduction in V_{OC}, a slightly lower J_{SC}, a higher shunt conductance (3.4 vs. 0.9 mS/cm^2), and lower fill factor than the reference sample. The V_{OC}, J_{SC}, fill factor and efficiency of the CdMgTe/HCl etch device are 0.648V, 22.8 mA/cm^2, 60.4%, and 8.9% respectively and the corresponding device parameters of the reference cell are given in Table I.

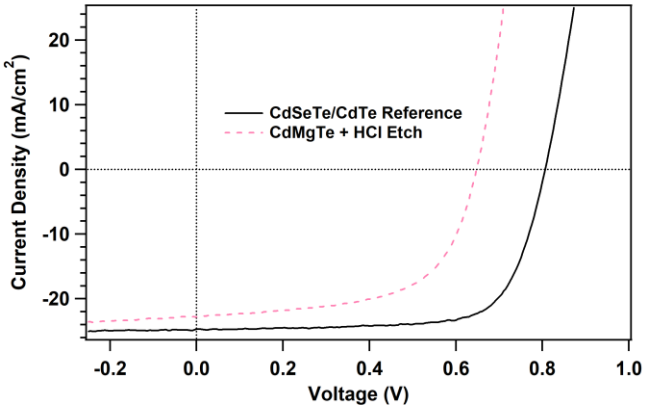

Fig. 8. J-V of the best HCl-etched CdMgTe device compared to the reference shows a notable drop in V_{OC}.

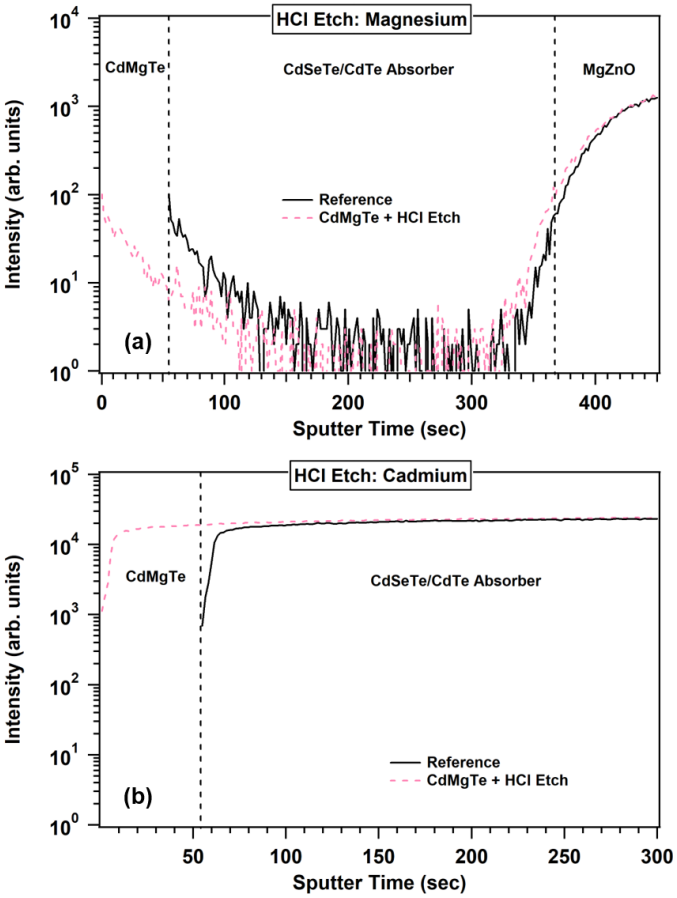

Fig. 9. Mg (a) and Cd (b) SIMS profiles of the HCl-etched CdMgTe structure show removal of Mg at the back.

To better understand why the CdMgTe/HCl etch device performance and V_{OC} were notably lower than the reference, SIMS was measured on both film structures. The Mg and Cd

SIMS profiles for the etched and reference structures are given in Figs. 9(a) and (b) respectively. Equivalent Mg levels and identical Cd profiles at the back indicate that the HCl etch removed Mg from the CdMgTe layer leaving CdTe. Based on these data, we believe that the lower J-V performance of the etched CdMgTe device may be due to removal of Mg from the CdMgTe layer and damage to the CdTe layer incurred from the HCl etch. Therefore optimization experiments of etched-CdMgTe will involve a less aggressive etch in the future. Since the HCl etch work is purely preliminary, device performance is promising; with optimization, etched-CdMgTe could be a good path forward for improving the efficiency of CdSeTe/CdTe devices.

C. CdSeTe/CdTe Absorbers with CdMgTe and CdTe Cap

Devices with CdMgTe and a CdTe cap shown in Fig. 1(d) received a short and medium preheat treatment and were compared to the CdSeTe/CdTe reference device. Light J-V curves for the best devices are shown in Fig. 10 and the corresponding parameters are reported in Table I. The CdMgTe with a CdTe cap does not improve the device efficiency compared to the CdSeTe/CdTe reference, however, the efficiencies are higher than those previously reported [3], [7] and fairly close to the reference. In agreement with preheat trends in section A, the capped device data also show better performance of the shorter preheat than the medium preheat device: J_{sc} values are comparable but V_{oc} and fill factor are both notably better with a shorter preheat. Devices with a short preheat treatment show V_{oc} only slightly lower than the reference.

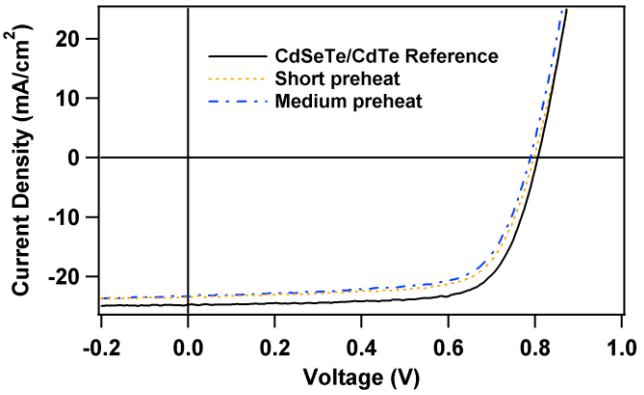

Fig. 10. J-V of devices with CdMgTe and CdTe cap is best with a shorter preheat time.

SIMS measurements were done on the best-performing CdMgTe/CdTe cap structure and the Mg profiles of the cap and reference samples are shown in Fig. 11. Due to the heat of the CdTe cap deposition process there is a fair amount of Mg diffusion throughout the absorber layer. The increase in Mg signal at the back indicates that the CdMgTe layer is present, however, the Mg level is lower than in the uncapped CdMgTe films shown in Fig. 7(a), indicating some Mg removal. Previous work with a CdTe cap demonstrated that although the cap minimized MgO formation at the CdMgTe surface there was still some localized Mg loss that appeared at grain boundaries [3]. This was attributed to Mg diffusion due to the high temperatures required for the CdTe cap deposition. Therefore the slightly lower performance of the capped devices may be due to localized Mg losses at the back.

TABLE I
J-V PARAMETERS FOR BEST CDTE CAP DEVICES

Device	V_{oc} (V)	J_{sc} (mA/cm²)	FF (%)	Eff (%)
CdSeTe/CdTe Reference	0.806	24.7	72.6	14.5
120s CdMgTe preheat	0.789	23.3	68.9	12.7
60s CdMgTe preheat	0.797	23.4	70.3	13.1

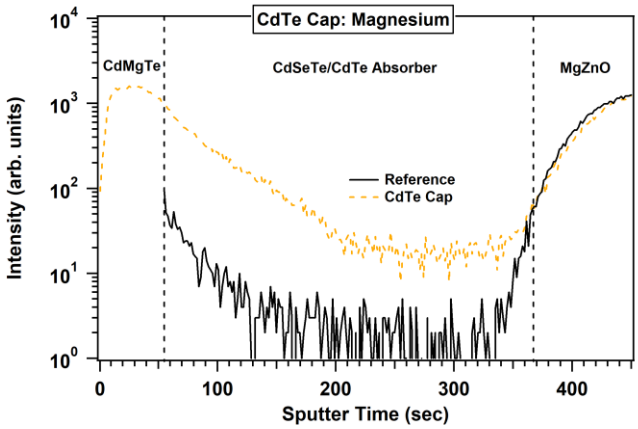

Fig. 11. Mg SIMS profiles of CdTe cap structure show some increased levels of Mg at the back, but film may have some Mg loss. Diffusion of Mg from the CdMgTe into the absorber occurs due to substrate heating during CdTe cap deposition.

IV. CONCLUSION

CdMgTe with a band gap of ~1.8 eV was deposited by CSS on CdSeTe/CdTe superstrates to develop fabrication methods which minimize difficulties of CdMgTe ER work. Four device structures were fabricated: a CdSeTe/CdTe reference, low-temperature CdMgTe, HCl-etched CdMgTe, and CdMgTe with a CdTe cap.

Devices fabricated with different preheat times utilized lower temperatures than in previous work [6]-[7] to minimize loss of Cl in the absorber. Increases in PL emission and τ_2 lifetime for shorter preheat times suggested that $CdCl_2$ passivation was better maintained for lower temperature CdMgTe deposition. Changes in $CdCl_2$ passivation retention were corroborated by QE measurements: QE response was poor for devices with long preheat times and improved for

shorter preheat times. SIMS measurements verified the presence of CdMgTe at the back and the effect of CdMgTe preheat on $CdCl_2$ retention in the absorber: long preheat treatment showed diminished levels of Cl in the absorber, while short preheat treatment showed Cl levels comparable to the reference sample, indicative of $CdCl_2$ passivation retention. Little or no CdMgTe preheat treatment provides a promising method to minimize $CdCl_2$ losses from CdMgTe deposition.

Preliminary results of a wet HCl acid etch treatment after CdMgTe deposition demonstrated decent device performance but reduced V_{OC} and fill factor compared to the CdSeTe/CdTe reference. Mg SIMS comparisons of HCl-etched CdMgTe and the reference showed equal levels of Mg at the back indicating the HCl etch removed Mg from the CdMgTe layer and likely damaged the CdTe film. Given the preliminary nature of the etch treatment, we believe that with optimization, an etched CdMgTe layer is a promising fabrication method for ER devices.

A CdTe cap was deposited behind the CdMgTe layer on additional devices to reduce Mg oxidation of the CdMgTe. Devices with a short preheat treatment demonstrated better performance than those with a medium preheat treatment due to better V_{oc} and fill factor, although neither outperformed the reference sample. A comparison of oxygen SIMS profiles for the reference and CdTe cap samples showed no sign of oxidation at the CdMgTe surface. The Mg profiles obtained from SIMS measurements showed Mg at the back of the structure, although at lower levels than an uncapped CdMgTe device. As previous publications have suggested, this is likely due to localized Mg loss due to the high temperatures of the CdTe cap deposition. Despite lowered levels of Mg at the back, CdTe cap devices demonstrated that good performance can be achieved with CdMgTe on the MgZnO/CdSeTe/CdTe structure, and the resulting 13.1% efficiency is the highest reported efficiency for CdTe devices that have CdMgTe at the back deposited by CSS. Progress remains to be made since V_{oc} is still lower than modeling predicts for a CdMgTe ER, but short preheat treatment, and etched-CdMgTe or a CdTe cap offer promising pathways for success.

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