Multi-Objective Simulation-based Optimization of Analog Transistor Sizing

Vaibhav Venugopal Rao and Ioannis Savidis
Department of Electrical and Computer Engineering
Drexel University, Philadelphia, PA 19104
vv85@drexel.edu, isavidis@coe.drexel.edu

Abstract—In this paper, the simulated annealing (SA) and genetic algorithm (GA) are explored for automating the design of an analog circuit. The transistor sizing methodology performs optimization with simulation-based feedback. The sizes of the transistors of an analog circuit are determined by the optimization algorithm and are applied to a schematic representation of the circuit for characterization through SPICE simulation. The characterized response of the circuit is then provided as input to the optimization algorithm for further tuning. The proposed transistor sizing methodology is applied to an active inductor based voltage controlled oscillator (VCO) for multiple target frequencies and amplitudes. The SA algorithm produced no more than a 6% error in frequency from target values, while the GA produced transistor sizes that resulted in no more than 6% error in frequency and 13% error in amplitude. In addition, the GA provided superior results in determining transistor sizes for higher target frequencies, as determined through calculation of the cost function. However, the improved results came at a considerably greater computational cost. A hybrid optimization technique is proposed, where GA performs coarse search space exploration to determine the initial conditions for the SA, and SA is then executed for fine optimization of the transistor sizes. The hybrid optimization technique not only resulted in 2.6x faster computational time as compared to GA but also resulted in a significantly lower cost function as compared to both the GA and SA optimization techniques. The results indicate that the proposed methodology provides a quick and accurate means of determining transistor sizes for target analog circuit specifications, which significantly reduces the cost and the design time of analog circuits.

Keywords—analog EDA, simulation-based optimization, simulated annealing, genetic algorithm

I. Introduction

The need for robust analog design methodologies is driven by circuit complexity along with lengthy and costly design cycles. According to a study by the IBS group [1], 20% of the circuit area is occupied by analog components, while 40% of the total effort is dedicated to analog design. Also, 50% of the overall costly design re-cycles are due to the analog components. The complexity in the synthesis of analog circuits is due to not only topology and layout synthesis but also in determining the transistor sizes of the circuit.

Although electronic design automation (EDA) tools are widely used in the design and verification of digital circuits, the use of EDA tools is not widespread in the analog domain. The lack of EDA tools for analog circuits is primarily due to

the high non-linearity and extreme sensitivity to noise and temperature of analog blocks. In addition, analog circuits are mostly custom designed for a target application and lack the modularity of digital circuits. Therefore, most analog blocks are manually designed and integrated to form a complex system. Designing the entire analog system typically requires many iterations of running lengthy simulations to explore the complex multi-dimensional design space to generate a solution that meets the system specifications.

Optimization methods have been proposed for the automation of transistor sizing of analog circuit blocks. Classical optimization methods include both deterministic-based and statistical-based techniques, such as Simplex [2], Dynamic Programming [3], Branch and Bound [4], and Goal Programming [5]. The deterministic and statistical optimization techniques are efficient for small size problems with less than 10 variables [6]. Due to the inherent solution mechanism and the dependence on the algorithm parameters, the classical optimization techniques provide limited use when pursuing multi-criteria constrained problems. The statistical optimization techniques require accurate circuit modelling and a strong initial starting point in the search space to produce accurate results. In addition, the statistical optimization techniques are computationally costly and do not guarantee convergence to a global optimal solution.

Heuristic-based optimization algorithms including simulated annealing [7, 8], Tabu search [9, 10], evolutionary algorithms [11], and genetic algorithms have gained importance due to the ability to explore large multi-dimensional search spaces that include a significant number of criteria and constraints while providing means to escape local minima/maxima within bounded computational costs. Heuristic-based optimization algorithms have been used for analog transistor sizing as well, where the optimization methods are applied to complex analog models and equations. In order to achieve higher accuracy of results, models that account for circuit non-linearity and non-idealities are required, which results in increased computational complexity. In addition, modeling analog systems consisting of non-identical analog sub-blocks is highly complex and time consuming.

The primary contribution of this paper is the development of an optimization methodology to determine transistor sizes and biasing conditions for a wide range of analog circuits, where the core optimization algorithm is fast and circuit and technology independent. In the proposed design methodol-

ogy, simulation based performance evaluation of an analog circuit is performed within an iterative optimization loop. Through simulation based heuristic optimization, accurate transistor sizes are determined for the target performance constraints at a fraction of the computational time and resources of a traditional and mostly manual design approach. Analog circuit specifications are used to formulate a set of constraints and performance metrics that provide the basis for a developed cost function. The developed methodology is applied to the design of an active inductor based VCO where simulated annealing, a genetic algorithm, and a hybrid genetic algorithm-simulated annealing (GA-SA) optimization approach is used to determine transistor sizes and biasing values for different operating conditions while minimizing the overall circuit area.

II. SIMULATED ANNEALING OPTIMIZATION FOR ANALOG TRANSISTOR SIZING

Simulated annealing (SA) is a stochastic based global optimization algorithm that performs random sampling of the search space to maximize or minimize the value of a cost function without becoming trapped in local maxima or minima [7]. The simulated annealing optimization methodology is inspired by the process of annealing in metallurgy, where a metal is heated and then cooled slowly to increase the size of crystals and reduce defects in the metal. For simulated annealing, heating the system refers to the relaxation of the acceptance criteria of the sample solution within the search space, while cooling the system refers to the narrowing of the acceptance criteria of the sample solution to more finely optimize the result around the target criteria. The SA algorithm randomly samples the search space, where a probabilistic function constrains the acceptance of a sub-optimal solution as the temperature cools. The transition from a current point p in the search space to a new point p_n is controlled by a random perturbation $\delta(p)$ at point p. The acceptance probability of the transition is defined as

$$F = \frac{1}{e^{\frac{f(p_n) - f(p)}{T}}}, \tag{1}$$

where $f(p_n)$ and $f(p)$ are the calculated cost function at the next and current point, respectively. The current temperature T controls the probability of accepting the transition from p to p_n. When the exploration of the search space first begins, the temperature T is set to a high value, which results in a high probability of accepting a sub-optimal solution. During the optimization process, T is reduced based on the specified cooling schedule, which reduces the probability of accepting a sub-optimal transition to a new point p_n.

A. *Problem Formulation*

The proposed SA optimization algorithm works in conjunction with SPICE simulation of the circuit, where transistor sizes $S = \{s_1, s_2, s_3....s_k\}$ are determined through execution of the optimization algorithm and the cost function Φ is evaluated through simulation. A simulation is executed on an extracted netlist of the analog circuit that includes transistor sizes determined by the optimization algorithm. The simulation returns the performance parameters $P = \{p_1, p_2, p_3...p_l\}$ (such as gain, bandwidth, operating frequency, etc) and the circuit area, which are included in the calculation of the cost function Φ when executing the optimization algorithm. The pseudo-code of the transistor sizing methodology is provided as Algorithm 1.

For multi-objective transistor sizing of an analog circuit, simultaneous optimization of all objective functions is completed to obtain an approximate Pareto-optimal front. In the case of multi-objective constraint optimization, performances are set as either objective functions or as constraints involving sensitivity analysis between different objective functions. The multi-objective optimization problem is formulated such that the performance of the VCO is maximized while minimizing the area.

Algorithm 1: Evaluation of objective function through simulation

Input: $S = \{s_1, s_2, s_3....s_k\}$
Output: $\Phi = \{P = \{p_1, p_2, p_3...p_l\} \cap \text{Area}\}$
analog_circuit (S)
    Generate netlist based on transistor sizes S
    Based on extracted netlist run simulations
    Capture performance values P
    Evaluate cost function Φ;
return P, *area*

B. *Optimization Algorithm*

The pseudo-code of the algorithm to optimize the transistor sizing of a VCO using SA is provided as Algorithm 2. Based on random initial values of S and T, an initial solution is determined. From the initial solution, a certain number of random points n in the search space are explored by slightly modifying the initial S. If the explored solution results in a lower cost function than the current solution (minimization problem) or if, on calculation of (1), the acceptance probability F is greater than that of a randomly selected point, then a decision to consider the selected solution is made. In addition, the temperature is decreased by the specified cooling rate k for each iteration of execution of Algorithm 2 for m number of iterations. The total number of iterations is given by m x n. The algorithm returns the best solution producing the lowest cost function Φ.

III. GENETIC ALGORITHM FOR ANALOG TRANSISTOR SIZING

The Genetic Algorithm (GA) is a search based meta-heuristic based on the principles of genetics and natural selection. The GA belongs to a larger class of evolutionary algorithms (EA), where GA mimics the process of biological evolution by choosing the genomes that are best suited to survive in an environment over successive generations. The GA uses a population of individuals (solutions) instead of a single solution to search the problem space in parallel, where for every generation, a new set of candidate solutions are generated by the bio-inspired processes of selection,

Algorithm 2: Simulated annealing algorithm to minimize area and maximize performance parameters

Input: Φ, number of iterations, T, k
Output: S_{best}, $Area_{best}$
$S_{best} = S_{current}$
for i to m **do**
  $S_i \leftarrow$ CreateNeighborSolution($S_{current}$)
  $T_{current} \leftarrow CalculateT(i, T_{max})$
  if $\Phi(S_i) \leq \Phi(S_{current})$ **then**
    $S_{current} \leftarrow S_i$
    if $\Phi(S_i) \leq \Phi(S_{best})$ **then**
      $S_{best} \leftarrow S_i$
  else if $Formula > Rand()$ **then**
    $S_{current} \leftarrow S_i$
  $T = T - T \cdot k$
return S_{best}

cross-over, and mutation. The GA generates a viable solution through the successive evolution of substandard solutions.

The GA optimization technique evaluates the fitness value Φ (cost function) of a given solution for the sizing of an analog circuit. The transistor sizes $S = \{s_1, s_2, s_3....s_k\}$ are determined through the optimization algorithm and the fitness value Φ is evaluated through SPICE simulation of the circuit. For each execution of the simulation loop, an analog circuit netlist is generated based on the transistor sizes determined by the optimization algorithm. Each iteration of simulation returns the performance parameters $P = \{p_1, p_2, p_3...p_l\}$ and the circuit area, which are used to calculate the Φ by the optimization algorithm.

Algorithm 3: Genetic algorithm to optimize analog transistor sizes for target performance specification.

Input: M, N, p_c, p_m, and k
Output: S_{best}, $Area_{best}$
Create N population randomly of string size l
for m in range 1:M **do**
  for n in range 1:$\frac{N}{2}$ **do**
    Select 2 parents through tournament selection
    Crossover parents' genes to get children at p_c
    Mutate children at p_m
  Get new generation of mutated children
  Keep track of the best chromosome in each generation
  $m = m + 1$
S_{best} = The chromosome with the best fitness value from all the generations
return S_{best}

The genetic algorithm implemented in this paper applies binary encoding to the chromosomes and tournament selection for choosing parents. The flowchart and the pseudo-code of the GA for analog transistor sizing is shown in the Fig. 1 and Algorithm. 3, respectively. The GA begins with an encoding of analog circuit design parameters (transistor sizing for this work). The transistor sizes for the analog circuit are binary encoded to represent a chromosome of a particular length l. Based on the range of transistor sizes and the computational complexity as given by the number of allowed iterations, the optimal length of the chromosome l is selected, with each chromosome string represented by a bit $B \in \{0, 1\}$. All chromosomes encoding the target parameters of the transistors are combined to form an initial genome. Based on the initial genome, the initial population of size N is generated by randomly altering the chromosome bits. Applying selection, crossover, and mutation to the initial population results in the creation of the first generation genomes. The genome with the best fitness value from the first generation is saved, and the genetic processes of selection, mutation, and crossover are then applied to the first generation genomes, which results in the second generation genomes. The process of producing new generations and storing the genome with the best fitness value is completed M times, and the genome with the best-fitness value from all the M generations is selected as the desired solution. The chromosome bits are decoded to obtain the values for each design parameter.

A. *Selection*

Selection is the process of choosing two genomes from the population for breeding. The stochastic-based tournament selection technique is utilized. The selection technique is implemented as follows.

1) Three random genomes ($k = 3$, where k is the number of genomes considered for tournament selection) from the population are randomly selected.
2) A fitness value for the randomly chosen genomes is determined as follows.
   - Decode the genome to obtain the values of the target design parameters,
   - Apply the values of the decoded design parameters (transistor sizes) to SPICE simulations to characterize the circuit response, and
   - Add the error between the simulated and the target values of different performance parameters to obtain the fitness value.
3) The genome with the best fitness value is selected as the first parent.
4) Steps (1-3) are repeated to select the second parent.
5) Steps (1-4) are repeated $\frac{N}{2}$ times to obtain N parents.

The process of selecting parents is followed by crossover, where two children are obtained from each pair of parents.

B. *Crossover*

Crossover is a stochastic process used in GA to combine genetic information of the two parents to produce two offspring. Two-point crossover is utilized, where two points in the parents' genome selected randomly are combined to produce two offspring. The crossover process is depicted in Fig. 2. The probability that a random point in the parent chromosome is picked for crossover depends on the value
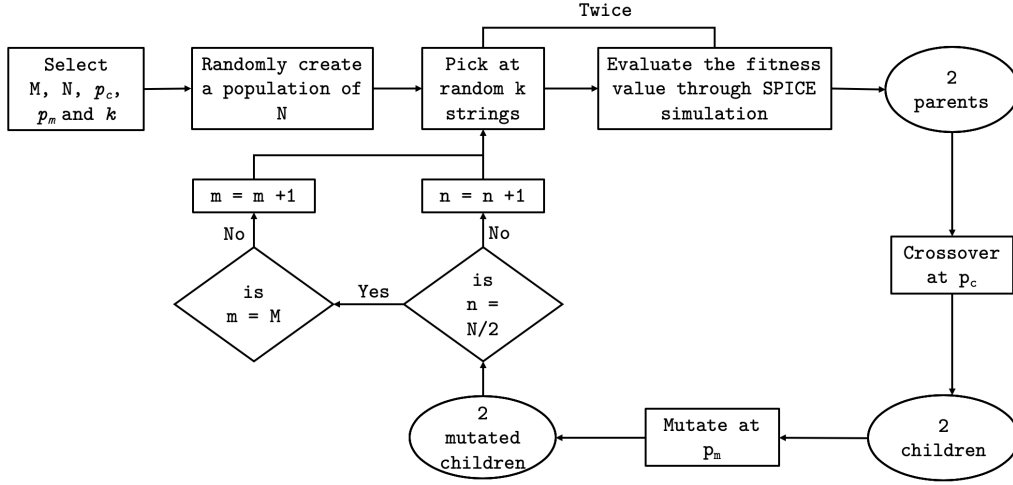
Fig. 1: Flowchart of the genetic algorithm with tournament selection for analog transistor sizing.
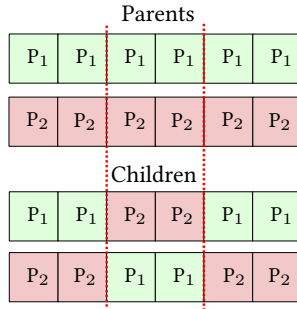

Fig. 2: Pictorial representation of the two-point crossover operation applied by the genetic algorithm.

of the probability of crossover (p_c). The bits of the parent chromosomes between the two randomly selected points are swapped, resulting in two children as shown in the Fig. 2.

C. *Mutation*

Mutation is a process used for maintaining genetic diversity from one generation to another by altering the state of one or more chromosomes from the initial state. In the proposed GA, an initial probability of mutation p_m is set. For each chromosomal bit, a random probability value is selected between 0 and 1. If the random number selected is less than p_m, then the chromosome bit is flipped. If, however, the random number is greater than p_m, then the initial bit of the chromosome is preserved. The genetic operators of selection, crossover, and mutation are performed $\frac{N}{2}$ times, which results in N number of children belonging to the next generation.

IV. APPLICATION OF OPTIMIZATION ALGORITHMS ON A VCO

The proposed analog design methodology based on simulated annealing and genetic algorithm optimization is applied to an active inductor based voltage controlled oscillator. A voltage controlled oscillator (VCO) is an essential component of radio-frequency systems that generates a stable

and tunable oscillating frequency based on an applied input voltage. The VCOs are used in frequency synthesizers including local oscillators, phase locked loops (PLL), and clock recovery circuits. Traditional VCOs utilize a passive inductor-capacitor (LC) tank architecture. Primary disadvantages of LC-tank based VCOs include 1) the tuning range of the oscillator is relatively low (around 10% to 20% of the nominal locking frequency), 2) on-chip passive inductors exhibit poor high frequency performance without active compensation, and 3) on-chip passive inductors significantly increase the circuit area [12, 13].

To improve the tuning range, increase the oscillating frequency, and reduce the area, an active inductor based VCO is implemented with a schematic topology as shown in Fig. 3. Transistors M_1 to M_6 form the active inductor, whose equivalent inductance is given by

$$L_{eq} = \frac{2 \cdot (C_{gs_1} + C_{gs_3})}{g_{ds_5} \cdot (2 \cdot g_{m_1} + g_{m_5} - g_{ds_5})} \qquad (2)$$

where L_{eq} is the equivalent inductance of the gyrator, C_{gs} is the gate to source parasitic capacitance of the given transistor, g_m is the small signal transconductance of the given transistor, and g_{ds} is the small signal output conductance of the given transistor [14, 15]. The equivalent inductance of the gyrator is controlled by the voltage L_{cntrl}. Transistors M_{var1} and M_{var2} form the active capacitor, whose equivalent capacitance is given by

$$C_{var} = C_{ox} \cdot W_{var} \cdot L_{var} + C_{gs} \cdot W_{var} + C_{gd} \cdot W_{var} \quad (3)$$

where C_{var} is the equivalent capacitance of the varactor, C_{ox} is the oxide capacitance of the M_{var} transistor, C_{gs} is the gate-to-source capacitance, and W_{var} and L_{var} are the width and the length, respectively, of the M_{var} transistors. The capacitance of the varactor is tuned by the control voltage C_{cntrl}. Transistors M_7 and M_8 form the negative resistor, which compensates for the parasitic resistances of the gyrator and varactor circuits and increases the voltage swing.

TABLE I: SPICE results from characterization of the active inductor based VCO with transistor dimensions determined by the simulated annealing optimization algorithm for multiple target frequencies and amplitudes.

Target Frequency	Target Amplitude	Number of Iterations	Time	Simulated Frequency	Simulated Amplitude	% Frequency Error	% Amplitude Error	Cost Function	Area (um*um)
1.5 GHz	1.2 V	500	5693 s	1.49 GHz	0.92 V	0.67 %	23.58 %	0.29	254.15
2.0 GHz	1.0 V	500	5678 s	1.99 GHz	0.91 V	0.50 %	9.10 %	0.10	251.00
2.5 GHz	1.0 V	500	5713 s	2.45 GHz	0.89 V	2.00 %	10.60 %	0.16	219.29
3.0 GHz	0.9 V	500	5901 s	3.01 GHz	0.79 V	0.33 %	12.78 %	0.13	220.19
3.5 GHz	0.9 V	500	5714 s	3.30 GHz	0.81 V	5.71 %	10.00 %	0.29	215.83
4.0 GHz	0.9 V	500	5473 s	4.10 GHz	1.17 V	2.50 %	30.00 %	0.37	66.787

TABLE II: SPICE results from characterization of the active inductor based VCO with transistor dimensions determined by the genetic algorithm for multiple target frequencies and amplitudes.

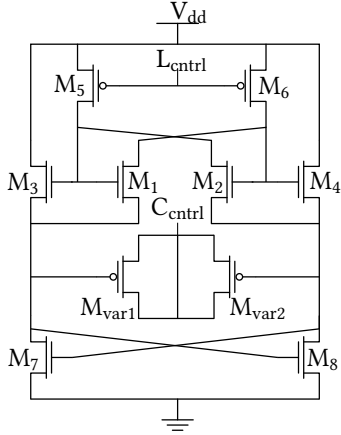| Target Frequency	Target Amplitude	Number of Iterations	Time	Simulated Frequency	Simulated Amplitude	% Frequency Error	% Amplitude Error	Cost Function	Area (µm*µm)
1.5 GHz	1.2 V	500	22982 s	1.58 GHz	1.05 V	5.33%	12.50%	0.23	270.89
2.0 GHz	1.0 V	500	22587 s	1.93 GHz	0.95 V	3.50%	5.00%	0.12	268.18
2.5 GHz	1.0 V	500	24922 s	2.51 GHz	0.88 V	0.40%	12.00%	0.13	225.28
3.0 GHz	0.9 V	500	22392 s	3.05 GHz	0.80 V	1.67%	11.11%	0.15	232.22
3.5 GHz	0.9 V	500	20363 s	3.55 GHz	0.89 V	1.43%	1.11%	0.06	195.81
4.0 GHz	0.9 V	500	20253 s	3.95 GHz	0.87 V	1.25%	3.33%	0.08	217.42

Fig. 3: Schematic representation of the active inductor based voltage controlled oscillator.

The simulated annealing and genetic algorithm is implemented in Python 2.7. The simulation framework is implemented using a combination of Cadence SKILL and the OCEAN scripting language. The circuit simulations are performed using SPECTRE.

The independent execution of both SA and GA results in the selection of widths for transistors M_1 to M_8, M_{var1}, and M_{var2} of the active inductor based VCO circuit shown in Fig. 3, which is then characterized through SPICE simulation. Parameters provided to the cost function include operating frequency and oscillating amplitude. The cost function (fitness value) for the active inductor based VCO is given by

$$\Phi = |F_{target} - F_{simulated}| \cdot 10^{-9} \\ +|Amp_{target} - Amp_{simulated}|, \quad (4)$$

where F_{target} and $F_{simulated}$ are the target and SPICE simulated frequencies, respectively, and Amp_{target} and $Amp_{simulated}$ are the amplitude of the target and SPICE determined output voltages, respectively. The operating fre-

quency and the amplitude of the simulated VCO with sizes determined using the optimization algorithm are compared against the desired specifications. The analysis is performed for 1.5 GHz, 2 GHz, 2.5 GHz, 3 GHz, 3.5 GHz, and 4 GHz target frequencies with accuracy and performance results listed in Table I and Table II for, respectively, SA and GA.

V. Results and Discussions

The SA and GA are implemented with an upper execution limit of 500 iterations. The simulated annealing algorithm searches five neighbors each iteration around a selected point as the temperature is decreased 100 times from $1000°C$ to $0°C$. For the genetic algorithm, the size of the population N for each generation is set to 10, and the total number of generations M is set to 50. Both SA and GA are executed five times with randomly generated initial conditions for each target frequency and the results with the best cost function (fitness value) are listed in Table I and Table II, respectively.

The results listed in Table I and Table II indicate that simulated annealing is almost 4x faster than the genetic algorithm for the same number of iterations. For lower target frequencies, the SA optimized transistor sizes of the VCO resulted in simulated frequencies with percentage errors, measured as a deviation in frequency from the target value, less than that observed for transistor sizes optimized by applying GA. At higher frequencies, the percentage error in the simulated frequencies from the SA optimized VCO were larger as compared to results produced by the GA. The fitness value calculated for the GA optimized VCO is much lower than the cost function determined for the SA optimized VCO, which indicates a superior quality of results from applying GA optimization on multivariate problems.

A hybrid algorithm consisting of both the simulated annealing and genetic algorithms combines the computational efficiency offered by SA with the greater quality of results provided by GA for multivariate search space exploration. For the hybrid algorithm, the GA is used to initially explore

TABLE III: SPICE results from characterization of the active inductor based VCO with transistor dimensions determined by the hybrid GA-SA optimization algorithm for multiple target frequencies and amplitudes.

Target Frequency	Target Amplitude	Number of Iterations	Time	Simulated Frequency	Simulated Amplitude	% Frequency Error	% Amplitude Error	Cost Function	Area (µm*µm)
1.5 GHz	1.2 V	300	7659 s	1.52 GHz	1.11 V	1.33%	7.50%	0.11	266.66
2.0 GHz	1.0 V	300	7528 s	1.97 GHz	0.94 V	1.50%	6.00%	0.09	247.13
2.5 GHz	1.0 V	300	7579 s	2.48 GHz	0.91 V	0.80%	9.00%	0.11	224.56
3.0 GHz	0.9 V	300	7722 s	2.94 GHz	0.84 V	2.00%	6.67%	0.12	212.24
3.5 GHz	0.9 V	300	7638 s	3.54 GHz	0.86 V	1.14%	4.44%	0.08	178.28
4.0 GHz	0.9 V	300	7466 s	3.92 GHz	0.94 V	2.00%	4.44%	0.12	196.66

the search space and determine ideal starting transistor dimensions that are then provided to the SA algorithm, which returns an optimized solution for the given constraints and circuit topology. The results from characterizing the VCO optimized by the hybrid algorithm are listed in the Table. III. As GA provides better search space exploration while SA provides improved localized optimization to find a minima, the number of iterations to optimize the VCO was reduced to 300 while the computational time was at least 2.6x shorter. The GA was performed for 150 iterations with N set to 10 and M to 15. The SA was then performed for an additional 150 iterations, where 5 nearest neighbors were searched each iteration around a selected point. The temperature was decreased 30 times from $1000°C$ to $0°C$. The hybrid-optimization technique generated transistor sizes that when simulated in SPICE resulted in output frequencies of the VCO that were no more than 2% from target values, amplitudes that were no more than 9% from target values, and calculated cost functions that were lower than either SA or GA optimization alone. The results indicate that hybrid optimization not only reduces the number of iterations and computational time, but also improves the accuracy of the solution by more efficiently pruning the search space.

VI. Conclusions

A low overhead and circuit and technology independent simulation based optimization methodology for analog circuit transistor sizing is described that applies both SA and the GA, resulting in a reduction in design time and cost. The proposed optimization algorithms take analog specifications as inputs and utilize multivariate search space exploration to output transistor sizes that minimize the error between the simulated and the target circuit performance parameters. The proposed methodology was applied to an active inductor based VCO for multiple target frequencies and amplitudes. The number of iterations of the optimization and simulation loop was set to 500. The SA algorithm produced no more than 6% error and 24% error between the simulated and target frequencies and amplitudes, respectively, while also generating transistor sizes that resulted in lower overall area. The GA produced transistor sizes that resulted in no more than 6% error in frequency and 13% error in amplitude, while providing a superior quality of results when selecting transistor sizes for higher target frequencies. Based on the results of the SA and GA, a hybrid optimization technique is proposed, where GA performs coarse search space exploration to determine the initial conditions for the SA algorithm, and the

SA algorithm performs fine grain optimization to determine the optimal solution for the given search space. The hybrid optimization reduces the computational time by at least 2.6x and produces transistor sizes that result in significantly lower cost functions as compared to executing GA or SA optimization alone. The proposed methodology provides an efficient approach to size analog circuits by reducing the design time and complexity.

References

[1] IBS Corporation, "IBS Corporation, Industry Reports," 2003.
[2] J. A. Nelder and R. Mead, "A Simplex Method for Function Minimization," *Proceedings of The Computer Journal*, pp. 308–313, January 1965.
[3] S. Hu, M. Ketkar, and J. Hu, "Gate Sizing For Cell Library-Based Designs," *Proccedings of the ACM/IEEE Design Automation Conference (DAC)*, pp. 847–852, June 2007.
[4] A. H. Land and A. G. Doig, *An Automatic Method for Solving Discrete Programming Problems*, Springer Berlin Heidelberg, November 2009.
[5] M. J. Schniederjans, *Goal Programming: Methodology and Applications*, Springer Science & Business Media, December 2012.
[6] Z. B. Zabinsky, "Stochastic Methods for Practical Global Optimization," *Proceedings of the Journal of Global Optimization*, pp. 433–444, December 1998.
[7] S. Kirkpatrick, C. D. Gelatt, and M. P. Vecchi, "Optimization by Simulated Annealing," *Proceedings of the Science Journal*, pp. 671–680, May 1983.
[8] P. Siarry, G. Berthiau, F. Durdin, and J. Haussy, "Enhanced Simulated Annealing for Globally Minimizing Functions of Many-Continuous Variables," *Proceedings of the ACM Transactions on Mathematical Software*, pp. 209–228, June 1997.
[9] F. Glover, "Tabu Search-Part I," *Proceedings of the Operations Research Society of America Journal on Computing*, pp. 190–206, August 1989.
[10] X. Lai, J. K. Hao, and D. Yue, "Two-stage Solution-Based Tabu Search for the Multidemand Multidimensional Knapsack Problem," *Proceedings of the European Journal of Operational Research*, pp. 35 – 48, April 2019.
[11] E. G. Pena and A. Araujo, "Multi-Objective Evolutionary Algorithm with Prediction in the Objective Space," *Proceedings of the Journal on Information Sciences*, Vol. 501, pp. 293 – 316, October 2019.
[12] F. Herzel, H. Erzgraber, and P. Weger, "Integrated CMOS Wideband Oscillator for RF Applications," *Proceedings of the IEE Electronic Letter*, pp. 727–736, March 2002.
[13] N. Troedsson and H. Sjoland, "High Performance 1 V 2.4 GHz CMOS VCO," *Proceedings of the IEEE Asia-Pacific Conference on ASIC*, pp. 185–188, August 2002.
[14] J. Laskar, R. Mukhopadhyay, and C. Lee, "Active Inductor-Based Oscillator: A Promising Candidate for Low-Cost Low-Power Multi-Standard Signal Generation," *Proccedings of the IEEE Radio and Wireless Symposium*, pp. 31–34, January 2007.
[15] S. Rajeshwari and V. Vaithianathan, "Design of Active Inductor Based Tunable Voltage Controlled Oscillator," *Proceedings of the IEEE International Conference on Communication and Signal Processing (ICCSP)*, pp. 0879–0883, April 2017.