A Low-Power Complementary Topology-based Switched-Capacitor Charge Pump Converter

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***Abstract*—Charge pump circuit is a subset of step-up DC-DC converter circuit to obtain a higher than input DC voltage in a variety of applications such as battery fast charging circuit, phase lock loop (PLL), dynamic random-access memory (DRAM), flash circuit, etc. This paper proposes a complementary Switched-Capacitor (SC) Dickson charge pump DC-DC converter circuitry simulated with standard 0.13 μm BiCMOS process. The proposed converter circuit introduces an additional completely symmetric charge pump to connect with the original single converter to create a complementary SC charge pump converter. The proposed circuit reduces the equivalent output impedance of the original single converter circuit and shows a stronger ability to drive loads. Simulation results show that the complementary based converter has faster dynamic response than the single converter topology. The overall power dissipation of the proposed converter circuit is only 21.88 nW.**

***Index Terms*—switched-capacitor, charge pump, complementary topology, dynamic response**

I. Introduction

Charge pump circuit is a power circuit that converts a low DC power supply input to a high DC power level. In the field of battery fast charging applications, the high-quality MOS monolithic integrated switched-capacitor converter circuit is being widely used because of its high reliability, high power density, and faster dynamic response [1]. Fig. 1 shows a typical wireless power transfer (WPT) based battery management unit where the DC-DC converter module plays a critical role for power flow and recharging the battery. The micro-processor unit (MCU) controls the entire charging module by detecting the battery status through the voltage measurement module, current measurement module, and other health monitoring modules. Based on the status update, the MCU controls the DC-DC converter to directly charge the battery module.

The DC-DC converter with multiple conversion ratios plays an extremely important role in the implementation of modern constant-voltage (CV) to constant-current (CC) combined fast charging method. Compared to the conventional LRC DC-DC boost converter circuit, the charge pump contains only switches and capacitors to regulate the required voltage. As a subset circuit of power converter, the charge pump is widespread in power management module, chip design, dynamic random-access memory (DRAM), electrically erasable programmable read-only memory (EEPROM), phase locked loop (PLL), and flash circuits [2]–[4], [6].

Charge pump transfer charges from the power supply to the output node through only switches and capacitors, which

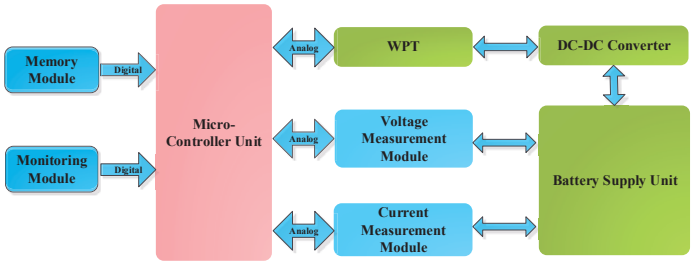

Fig. 1. Schematic diagram of a battery management system, where DC-DC converter is being integrated.

facilitates for the perfect integration in a monolithic chip instead of off-chip. With no inductive component, the SC charge pump has high linearity and high dynamic response [2], [8], [9]. Furthermore, in most portable power management devices, the inductor is not suitable for integration into the chip design due to its Q value requirements and its strong nonlinear characteristics. In general, the charge pump circuit has a strong de-linearization feature, and as part of the chip circuit, this step-up converter reduces the system fabrication size and cost of the power management module [12] [13]. In a WPT system composed with inductive coupling, the power source drives the mutual coupling primary inductor through the power amplifier to transmit the electrical energy to the secondary inductor in the form of electromagnetic waves [7]. Then, the secondary inductor charges the battery with constant voltage through AC-DC rectification and DC-DC conversion. However, in the conventional LRC DC-DC power converter, the addition of the filter inductor and the associated nonlinearity not only affects the size but also affects the harmonic response of the entire converter. The size of the inductor also makes the converter circuit unsuitable for multi-battery and distributed battery management modules. The nonlinearity of the inductor makes it susceptible for the entire converter circuit to have a bifurcation problem that ultimately leads to instability and uncontrollability of the converter system [10], [11].

In the SC DC-DC converter, Seeman et. al [12], developed a fundamental model for SC converters and introduced the methodology for analysis using the slow switching limit (SSL) impedance and fast switching limit (FSL) impedance. It introduced a network-theoretic method for determining the conversion ratio and output impedance. Additionally, E. Boniz-

zoni [5] and T. Sai [14] focused on high conversion efficiency by using different types of SC converter topologies. Although the analysis method is in general and it addresses the SSL and FSL output impedance modeling problem, the methodology is only for steady-state analysis. However, under different types of load circumstances, such as for battery charging unit with faster charging time requirement, improvement of the dynamic response is significant for SC DC-DC converter.

In this paper, a complementary topology based SC charge pump converter is proposed. Th proposed converter circuit introduces an extra completely symmetric charge pump to connect with the original single converter to produce a complementary SC charge pump converter. The proposed circuit reduces the equivalent output impedance of the original single converter circuit and shows a stronger ability to drive loads and faster dynamic response. The proposed complementary SC DC-DC converter is adapted to other converter topologies with different types and conversion ratios.

The organization of the paper is as follows. Section II presents an overview of the existing single Dickson charge pump circuit. A thorough analysis of the proposed complementary Dickson charge pump is presented in Section III. Sections IV and V present the simulation results and conclusion, respectively.

II. Overview of the Single SC Dickson Charge Pump

SC converter circuit is a subset of power DC-DC converter circuit, which contains only switches and capacitors. Compared to conventional LRC power converter circuit, SC converter achieves different conversion ratios only by converter's structure that switching sequence to change capacitors charging and discharging status. This relatively unfixed structure in order to achieve multiple conversion ratios is a disadvantage of SC converter, but at the same time it is also providing highly flexible and diverse for chip circuit design. Inevitably, the SC converter has inherent defects in continuous conversion ratio and regulation.

A single SC 1:2 Dickson charge pump converter structure is shown in Fig. 2. The capacitor C1 and C2 are defined as bypass capacitors and the capacitor C3 is defined as flying capacitor. As this configuration, the conversion ratio of this converter structure is 1:2, which DC input Vin over DC output Vout is 1:2, also called voltage doubler circuit. This charge pump circuit is working with two non-overlapped square wave control signals, while the odd number of switches (S1, S3, S5, S7) are turned off then the even number of switches (S2, S4, S6, S8) are turned on. Under the action of the control signals, the switches are continuously turned on and off, so that the capacitors are constantly changing in the charging and discharging states. After a period of charging and discharging, this circuit finally provides a steady-state DC voltage at the output node. The idealized transformer equivalent circuit is shown in Fig. 3. The converter ratio M is,

$$M = \frac{m}{n} = \frac{V_{in}}{V_{out}} \tag{1}$$

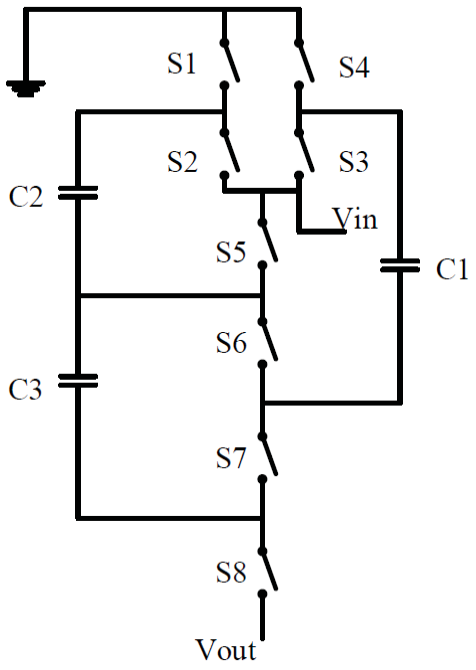

Fig. 2. Diagram of conventional 1:2 Dickson charge pump.

where M is the DC-DC power converter ratio, m and n represent from primary side to secondary side. Furthermore, V_{in} is the input side DC voltage and V_{out} is the output side DC voltage separately. The equivalent output resistant R_{out} can be represented as,

$$R_{out} = \sqrt{R_{SSL}^2 + R_{FSL}^2} \tag{2}$$

where R_{SSL} is the slow switching limit (SSL) impedance and R_{FSL} is the fast switching limit (FSL) impedance. The R_{SSL} value is only depending on converter structure, capacitor value and switching frequency. This calculation is to ignore the equivalent impedance of the capacitors at low frequency, and the idealized switches do not consider the effects of the turn-on resistance and the turn-off capacitance. Besides, the FSL impedance is characterized by constant current flow between capacitors. The switches' turn-on resistance and other resistances are sufficiently large that cannot be neglected.

III. Proposed Complementary SC Dickson Charge Pump

As a partial of DC-DC converter, the SC converter is suitable for no load or pure capacitive load connection, which

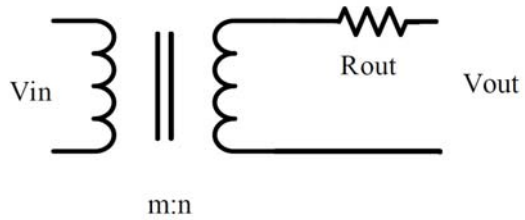

Fig. 3. SC converter idealized transformer equivalent circuit.

is one of the reasons why SC converters are commonly used in power supply module integrated in chip circuit. In order to increase the load driven capability and its dynamic response, a new complementary SC converter topology is proposed in this paper. The circuit diagram is shown in Fig. 4.

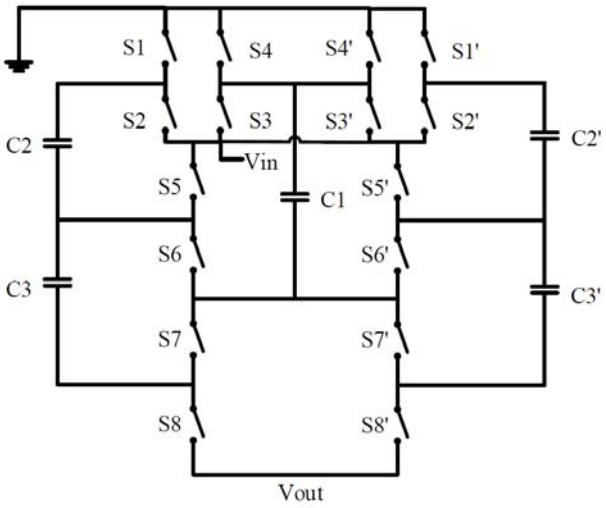

Fig. 4. Complementary 1:2 Dickson charge pump.

This complementary SC DC-DC converter is also working with two non-overlapped square wave control signals. A complete symmetric Dickson charge pump is connected mirrorlike with single charge pump circuit. The odd number and the even prime number of the switches forming one group, while they (S1, S3, S5, S7, S2', S4', S6', S8') are turned on then the others (S2, S4, S6, S8, S1', S3', S5', S7') are turned off. This calculation is to ignore the equivalent impedance of the capacitors at low frequency, and the idealized switches do not consider the effects of the turn-on resistance and the turn-off capacitance. Due to the addition of a symmetrical structure, the equivalent bypass capacitor is enhanced to facilitate the filtering of the steady-state ripple voltage.

Within this proposed complementary topology, the equivalent output impedance $Rout$ is significantly reduced, which enhances the load driven capability and dynamic response of the charge pump converter. The enhanced load driven capability reduces the input impedance design of the subsequent load circuit, and has a faster dynamic response to the power supply voltage while ensuring immunity to power voltage interference.

IV. Simulation Results

Cadence simulations are performed to access the SC DC-DC converter integrated in single chip. The proposed complementary circuit and the compared single converter circuit are designed and simulated with 0.13 μm standard BiCMOS process. The Vin is 0.3 V DC power supply. As well as the two non-overlapped square wave control signals' (Φ1 and Φ2) frequency are 200 MHz, which are shown in Fig. 5.

From the transient simulation results shown in Fig. 6, the steady state output voltage of the single converter is 598 mV

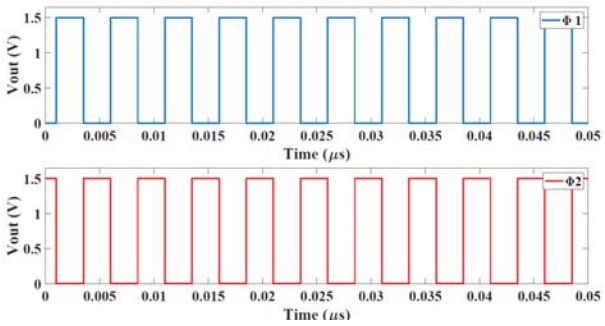

Fig. 5. Two non-overlapped control signals

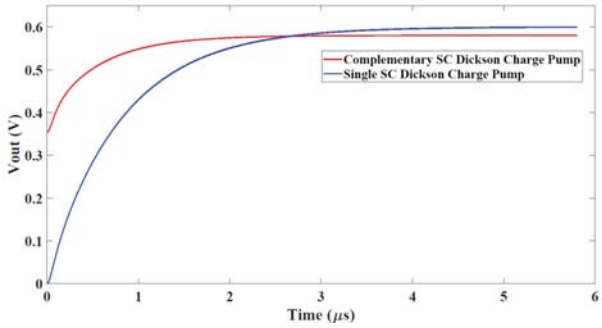

Fig. 6. Output voltage comparison of single converter and complementary converter

and the settling time is 1.83 μs. Furthermore, the steady state output voltage of the complementary converter is 579 mV and the settling time is 668.91 ns. For the complementary converter, the steady-state DC output error voltage is 21 mV (3.5%), which is higher than the single converter of 2 mV (0.3%), and the settling time of the complementary converter is only 36.5% of the single converter. The comparison data between the single 1:2 Dickson SC DC-DC converter with the proposed complementary 1:2 Dickson SC DC-DC converter is shown in Table I. The faster settling time means less charging and discharging state that reducing the power consumption and improving faster dynamic response.

Furthermore, as the SC DC-DC converter power efficiency η can be represented from the transformer model shown in Fig. 3,

$$\eta = \frac{V_{out}I_{out}}{V_{in}I_{in}} = \frac{1}{1+\frac{R_{out}}{R_{load}}} \tag{3}$$

The power efficiency comparison result between single converter and complementary converter under some value of load resistor is shown in Fig. 7.

This complementary SC DC-DC converter reflects the suitability and compatibility of integrating on a single chip for its simple circuits based CMOS switches and capacitors. The proposed structure improves the power conversion efficiency by decreasing the equivalent output resistance with enchancing the dynamic response connecting the symmetric converter and minimize the circuit area.

TABLE I
SUMMARY OF PERFORMANCE COMPARISON

Converter Type	Single Dickson Converter	The Proposed Complementary Converter	Y. Jiang ISSCC'18 [15]	D. Lutz ISSCC'16 [16]	J. Jiang JSSC'17 [17]
Technology	130nm BiCMOS	130nm BiCMOS	65nm CMOS	350nm HVCMOS	130nm CMOS
Converter Type	Boost	Boost	Buck-Boost	Buck-Boost	Buck
DC Input Value (V)	0.3	0.3	0.22∼2.4	2∼13	1.6∼3.3
Steady-state Output Value (V)	0.598	0.579	0.85∼1.2	5	0.5∼3
Steady-state Output Error (V)	0.002	0.021	N/A	N/A	N/A
Settling Time (ns)	1834.6	668.9	N/A	N/A	N/A
$\eta_{peak}(\%)$	94.23	93.87	Buck: 84.1 Boost: 83.2	Buck:81.5 Boost: 70.9	91

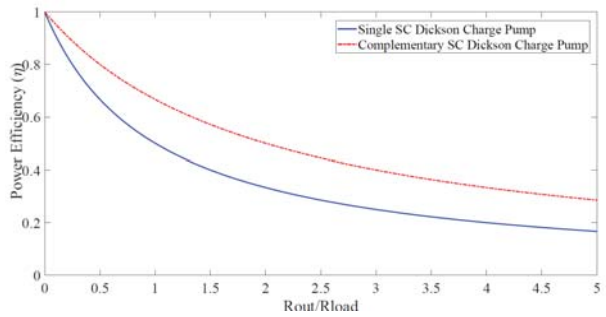

Fig. 7. Power efficiency comparison between single converter and complementary converter.

V. CONCLUSION

In this paper, a complementary topology has been implemented in the single Dickson 1:2 charge pump circuit for DC-DC converter design in a monolithic chip. The complementary topology decreases the equivalent output impedance and enhances the load driven capability. Moreover, the proposed converter effectively increases the power conversion efficiency and decreases the settling time. Simulation results indicate that the steady-state DC output error voltage of the proposed complementary converter is 21 mV (3.5%), which is higher than the single converter of 2 mV (0.3%). However, the settling time of the complementary converter shows a tremendous improvement, which is only 36.5% of the single converter. The faster settling time enables faster charging of the battery unit. The overall power consumption of the complementary architecture is only 21.88 nW that makes the proposed architecture an excellent choice for portable device applications with rapid charging of battery modules.

ACKNOWLEDGMENT

The work is supported in partial by the National Science Foundation (NSF) Award No. ECCS-1813949 and Award No. CNS-1645863.

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