

Formal Design Methodology for Discrete Proportional-Resonant (PR) Controllers Based on Sisotool/Matlab Tool

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Abstract— This paper presents a formal methodology for the analysis and design for discrete time proportional-resonant classic (PR) controllers applied to a single-phase DC/AC converter using Sisotool/Matlab tool. This tool allowed integrating and visualizes the classical control theory requirements (overshoot, settling time, etc.) with the design of Proportional Resonant (PR) controllers. Simulations results demonstrate the effectiveness of the methodology presented for the design of PR controllers.

Keywords—Proportional-resonant (PR) controller, single-phase inverter, microgrid,

I. INTRODUCTION

Distributed Generators (DGs) based on power electronic interfaces, DC/AC or AC/AC converters allow renewable energy such as solar and wind energies to be integrated into the power system or in a Microgrid. The controllers of these DGs must maintain the proper operation of the generator in the power grid without a communications system. A hierarchical control is widely used to ensure proper operation of DGs.

This control consists of four levels and divides the tasks to make a Microgrid more controllable [1]. The lower levels of the control (Zero level and 1st level) consists of two loops on the inverter, an inner and an outer. The inner loop is used for the current and voltage regulation while the outer loop uses the PQ droop curves and the virtual impedance to share the active and the reactive power to the loads using only the control's local variables. These levels are the foundation on which the higher levels are built.

Renewable energies are intermittent in behavior, potentially leading to large disturbances in the electric system [2]. To cope with the technical challenges related with integration of large quantity of variable renewable energy onto the electricity grid, safely and reliably, the flexibility of the power system must increase [3]. Typically, these control levels are implemented using classical controllers such as Proportional-Resonant (PR)

controller when they use stationary framework ($\alpha\beta$), and a Proportional-Integral (PI) controller when they use the dq framework [4], [5]. These controllers offer adequate results, achieve zero steady state error at the selected frequencies, while providing a good combination of simplicity and high performance but do not guarantee robustness under external disturbances. Optimal Controllers such as Linear-Quadratic Regulators and H^∞ controllers are synthesized such that performance and robustness characteristics are maximized [6], [7].

Although the fact that the PR controller does not guarantee robustness under external disturbances, they are an excellent starting point for researchers who are venturing into the topic of microgrid control, since, it allows understanding and strengthening basic concepts of the zero level of hierarchical control, specifically, control of voltage/current of Inverter Based Generators (IBG).

Most of the studies related to PR controllers have been carried out in the continuous domain, however, their observations and conclusions cannot be directly applied to digital devices that work in the discrete time domain [8]. In turn, in these studies they perform a "tuning" of the controllers by locating poles, Bode Diagrams, Nyquist, etc. [9]–[12]. However, there is no evidence of a formal methodology for the design of PR controllers using of classical control theory requirements (overshoot, settling time, etc.).

In this article, a formal methodology is proposed for the design of classic PR cascade voltage/current controllers based on settling time and overshoot requirements, using the Sisotool/Matlab tool for an IBG connected to a load.

The proposed design methodology is validated by simulation results obtained for a single-phase inverter connected to an LCL filter and a load.

II. DESCRIPTION AND MODELING OF THE SYSTEM

In this work, for simplicity, a single-phase bridge converter was implemented. The use of this converter does not cause loss of generality, so the same design can be used for single-phase half-bridge or three-phase converters with output filter.

Fig 1 shows the converter system with voltage/current cascade PR controller, considered in this work. The converter system is comprised of a standard single-phase voltage source inverter driven from a constant DC bus and connected to load through an LCL filter.

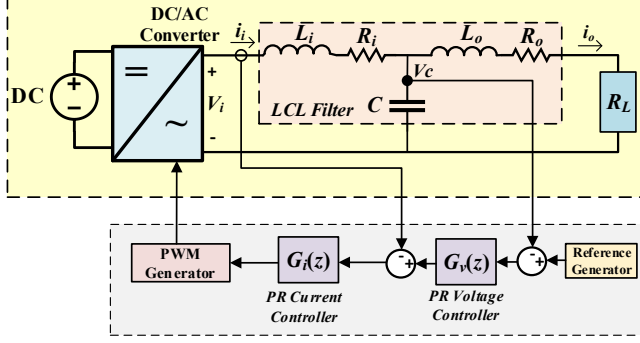


Fig 1. Typical scheme of voltage/current cascade control with PR controller for a single-phase inverter

The analytical model is an important tool for prediction of dynamic performance and stability limits using different control laws and system parameters. A mathematical model of the inverter must be established before the design stage.

Using Kirchhoff's law of voltages and currents in the schematic diagram of the proposed single-phase inverter system shown of Fig 1, The following diagram represents the model of the system:

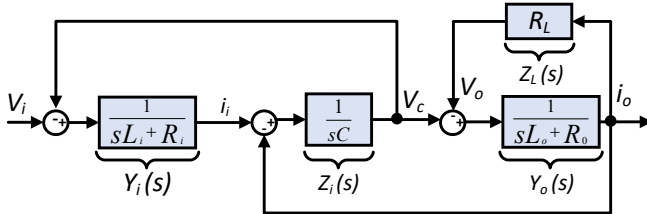


Fig 2. Block Diagram of LCL Filter

Applying block algebra in the Fig 2, the following transfer functions are obtained:

$$G_p^i(s) = \frac{i_i(s)}{V_{in}(s)} \quad (1)$$

$$G_p^i(s) = \frac{Y_i(s)[1 + Y_o(s)Z_c(s) + Y_o(s)Z_L(s)]}{1 + Y_o(s)Z_c(s) + Y_o(s)Z_L(s) + Y_i(s)Z_c(s)[1 + Y_o(s)Z_L(s)]}$$

$$G_p^v(s) = \frac{V_c(s)}{i_i(s)} = \frac{Z_c(s)[1 + Y_o(s)Z_L(s)]}{1 + Y_o(s)Z_c(s) + Y_o(s)Z_L(s)} \quad (2)$$

Using equations (1) and (2), it is possible to represent the closed-loop circuit system for cascade control of current and voltage as shown in Fig 3. The measured voltage (v_c) is

compared to the reference so that the error is processed by a PR controller that performs the same procedure but with the measured inner current (ii).

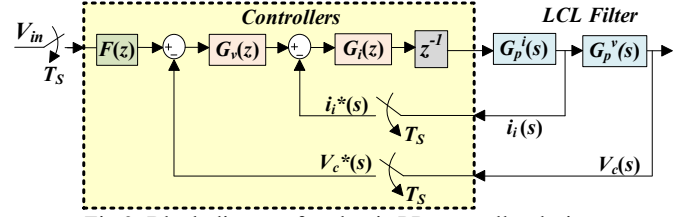


Fig 3. Block diagram for classic PR controller design

$F(z)$ is a pre-filter used only for the design of PR controllers. The pre-filter is the sine function divided by the unit step function, which will allow observing the response of the system to a sinusoidal step when PR controllers are being designed. The following equation represents the transfer function of the prefilter:

$$F(z) = \mathcal{Z} \left\{ \frac{\sin(\omega_o t)}{u(t)} \right\} = \left(\frac{z-1}{z} \right) \left(\frac{\sin(\omega_o T_s)}{z^2 - 2 \cos(\omega_o T_s)z + 1} \right) \quad (3)$$

where ω_o is the fundamental frequency that will be used for the design of the PR controllers, and T_s is the sample time.

III. CONTROLLER DESIGN

In this work, a formal PR controller design methodology for DGs is presented. The design of two PR voltage and current controllers in cascade is presented using the Matlab tool called sisotool, specialized for the design of control systems. This tool is used since it allows to include and visualize classical control requirements for the design of controllers such as overshoot, rise time, settling time, etc. For the design and simulation tests, the parameters of the single-phase voltage inverter with full-bridge topology are shown in Table I.

TABLE I. SYSTEM PARAMETER VALUES

Parameter	Value
Switching frequency (f_c)	10 KHz
Fudamental frequency (ω_o)	376.99 Rad/s
Rate Voltage	120 V_{RMS}
DC bus voltage (V_{DC})	400 V
Filter Capacitance (C)	8.8 μF
Filter Inner Inductante (L_i)	1.8mH
Filter Output Inductante (L_o)	1.8mH
Inner Inductante Resistenace (R_i)	0.1 Ω
Output Inductante Resistenace (R_o)	0.1 Ω
Load Resistance (R_L)	50 Ω

A. PR Controller Description

PR controllers are often used to regulate output voltage or current in a stationary $\alpha\beta$ or ABC reference frame. A PR controller has the following transfer function (TF):

$$G_{PR}(s) = k_p + k_i \frac{\overbrace{s}^{H_{Res}(s)}}{s^2 + \omega_n^2} \quad (4)$$

where k_i is the resonant control gain and ω_n is the nominal microgrid angular frequency. The term $s^2 + \omega_n^2 = (j\omega_n)^2 + \omega_n^2$ becomes zero at the nominal frequency. Thus, the open-loop gain of the PR controller at the nominal frequency is infinite with zero phase. An infinite open-loop gain implies that the PR controller achieves zero steady-state error when a sinusoidal reference signal oscillates at the nominal frequency [13].

Considering that these controllers are implemented in embedded systems, the design was carried out directly in discrete time. The $G_{pi}(s)$ and $G_{pv}(s)$ plants were discretized using First Order Hold (FOH). A very good approximation is obtained in the dynamic behavior of the system with respect to the continuous-time model when this discretization method is used.

One of the most used ways to implement the PR controller is by using two discretized integrators using Euler forward and backward as discretization methods [4]. The main advantage of this structure is its simplicity when frequency variations occur and they have to be corrected online, since it is not necessary to calculate the regulator gains to perform the frequency adaptation. However, this method has the disadvantage that it does not provide a zero steady-state error at the desired resonance frequency, especially for high frequencies. Another form of implementation, which will be adopted in this work, is discretizing the entire PR controller transfer function using Tustin with pre-deformation frequency. For this work, the method was used to discretize the proposed controller. The term $H_{Res}(s)$ of equation (4) was discretized using “Tustin with pre-warping method”. This method is the most appropriate and approximate for this type of controllers according to the study carried out in [8]. The following equation represents the discretized PR controller used in this work:

$$G_{PR}(z) = k_p + k_i \left(\frac{\sin(\omega_o T_s)}{2\omega_o} \right) \left(\frac{\overbrace{z^2 - z}^{H_{Res}(z)}}{z^2 - 2 \cos(\omega_o T_s)z + 1} \right) \quad (5)$$

B. Design Methodology (Sisotool)

The process of computing the cascade PR voltage and current controllers can be described by the following algorithm:

- 1) Obtain a mathematical model in the form (1) and (2) of the DGs to be controlled.
- 2) Set design requirements: overshoot, rise time, settling time, etc., for the inner current control loop and for the external voltage control loop.
- 3) To design the inner current control loop, select the control architecture 1 in sisotool and enter: in C the TF of the PR current controller, in G the TF $G_p^i(z)$ and in F the pre-filter mentioned in (3). Choose a gain of the resonant k_{ii} and vary the proportional gain k_{pi} until obtaining a response to the desired sinusoidal step that meets the established requirements.

- 4) To design the outer voltage control loop, select the control architecture 6 in sisotool and enter: in C1 the TF of the PR voltage controller, in C2 the TF of the PR current controller designed in the step 2, in G1 and G2 the TF $G_p^i(z)$ and $G_p^v(z)$ respectively, and finally in F the pre-filter mentioned in (3). Choose a gain of the resonant k_{iv} and vary the proportional gain k_{pv} until obtaining a response to the desired sinusoidal step that meets the established requirements.
- 5) If the performance is not suitable for the designer requirements set up in the step 2, repeat the process from step 3 by changing the values of k_{pi} and k_{ii} .
- 6) Evaluate the performance of the PR voltage and current controllers in cascade controller by using a simulation of the diagram shown in Fig 1.

Cascade controllers design requires that the dynamics of the inner and outer control loops be separated. Usually, it is designed for the inner control loop to be faster than the outer one. However, due to the topology of the classic PR controllers used in this work, by making the inner current loop faster than the outer voltage loop, it is not possible that the system of Fig 1 with the parameters of Table I meet established design requirements. Therefore, for this work, it was designed so that the outer voltage loop was faster than the inner current loop and thus meet the design requirements. The effect of this consideration is that the control effort leaving the voltage controller, which is the current reference for the inner current control loop is much larger than the controlled current (i_i). This greater control effort helps the response of the inner loop of the current control to be much faster and does not cause any physical damage since it is a signal that runs within a digital system and not a physical signal. In the results section, there are more details.

Applying the algorithm described in the system with the parameters given in Table I, the following results were obtained.

For the design of the inner current controller, the following control requirements are established: rise time of less than 0.1s, settling time of less than 0.2s and an overshoot of less than 10%. Subsequently, step 3 is performed to meet these requirements $k_{ii}=5085$ and $k_{pi}=4.62$ were found. Fig 4 shows the response to a sinusoidal step of amplitude 1 provided by sisotool. The yellow section in the graph represents the established requirements. To determine that the response meets the requirements, it must be within the white section in the graph, as effectively is observed in Fig 4

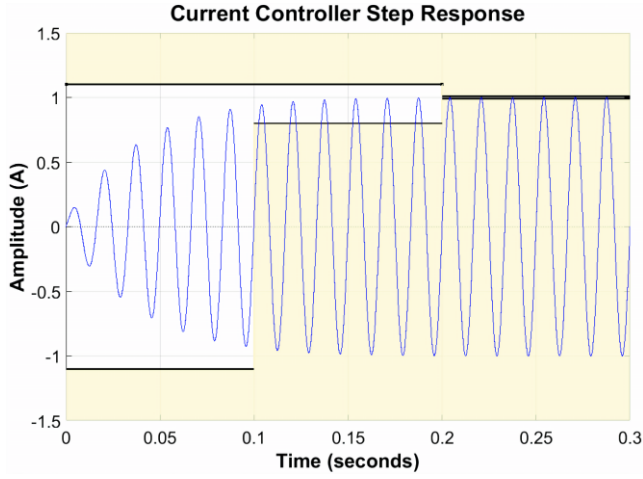


Fig 4. Response to Sinusoidal Step of Current in the Inner Inductor

Additionally, to verify the robustness and stability of the inner current loop, Fig 5 shows the Nyquist diagram provided by sisotool, where it is evident that the system is stable since it never wraps around the point $(-1,0)$. It also has good stability margins: 15.8dB of gain margin and 53.6° of phase margin.

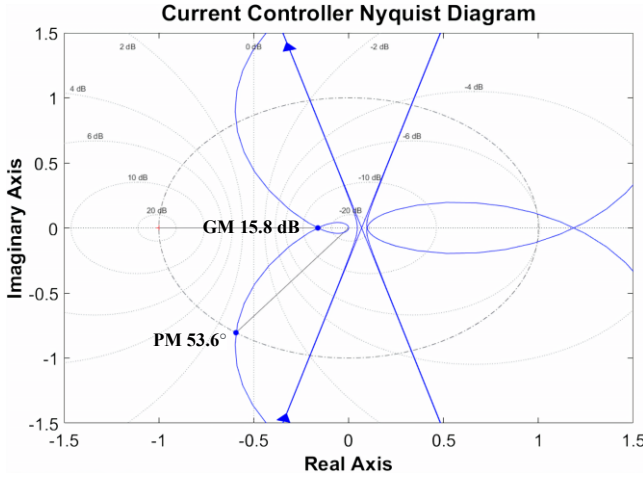


Fig 5. Nyquist Diagram for the Inner Loop of Current

For the design of the outer voltage controller, the following control requirements are established: rise time of less than 0.05s, settling time of less than 0.1s and an overshoot of less than 10%. Subsequently, step 3 is performed to meet these requirements $k_{ii}=150$ and $k_{pi}=0.042$ were found. Fig 6 shows the response to a sinusoidal step of amplitude 170 provided by sisotool. The yellow section in the graph represents the established requirements. To determine that the response meets the requirements, it must be within the white section in the graph, Fig 6. In this case, it is observed that in the first cycle of the response to the sinusoidal voltage step, there is an overshoot in the region of the requirements, but this can be omitted because in power electronic systems, a soft start is always performed in the voltage reference and not a 100% step that changes instantaneously, avoiding these overshoots.

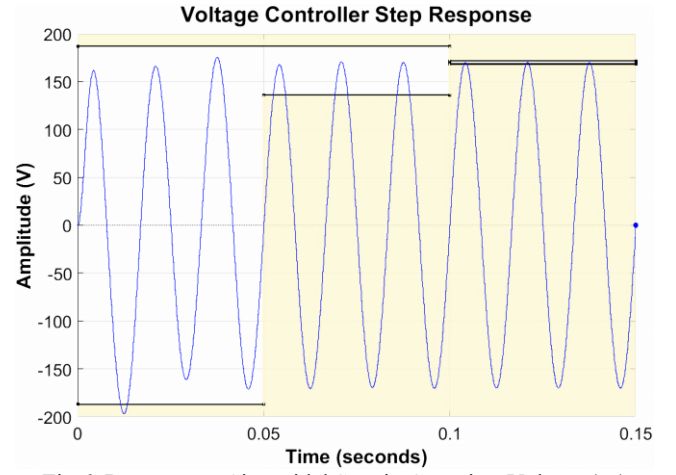


Fig 6. Response to Sinusoidal Step in Capacitor Voltage (v_c)

Similar to the inner current loop, in order to verify the robustness and stability of the inner voltage loop, Fig 7 shows the Nyquist diagram provided by sisotool, where it can verify that the system is stable since it never wraps around the point $(-1,0)$. It also has good stability margins: 4.6dB of gain margin and 50.8° of phase margin.

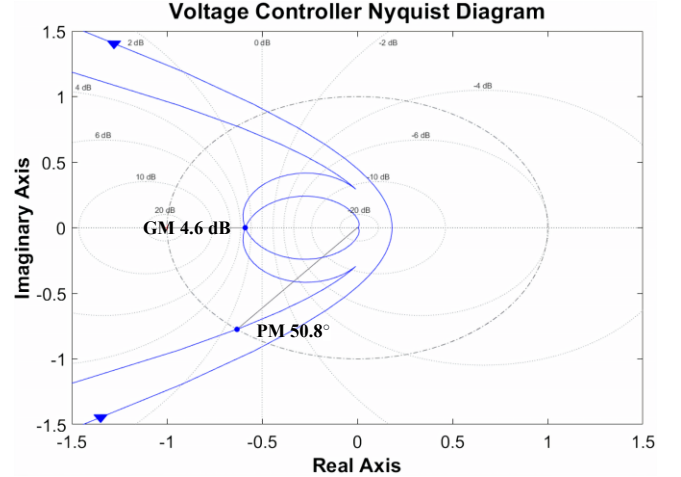


Fig 7. Nyquist Diagram for the Outer Loop of Voltage

IV. SIMULATIONS RESULTS

To assess the performance of the designed PR controllers, the system described in Fig 1 was simulated in Simulink/Matlab. The system parameters used for the simulation are the same parameters used in the design stage, they are shown in Table I.

For this validation, the reference voltage in the inverter capacitor v_c started with a peak value of $108\sqrt{2}$ V, minimum amplitude allowed by the IEEE1547 standard [14], it also starts with a resistive load of 100ohm. At $t = 0.05$ s, the inverter's v_c reference increased to a peak value $132\sqrt{2}$ V, the maximum value allowed by the IEEE1547. Subsequently at $t = 0.16$ s a second resistive load with value of 100ohm is connected to the system. Fig 8 and Fig 9 show the current and voltage waveforms in the inner current loop (i_i) and outer voltage loop (v_c) respectively, for the cascade PR controller simulated system.

Fig 9 shows the behavior of the current i_i . The dotted green signal is the current reference from the voltage controller $G_v(z)$, it is observed that it is twice the amplitude of the controlled current i_i (gray signal) which causes a faster response in i_i , effect of making the loop inner slower than outer loop. The blue signal is the current error, it is observed that when the first event occurs at $t = 0.05$ s the error has a peak of more than 4A but the current i_i has an overshoot of less than 5% and settling time of 0.07s with a steady state error of less than 2%. Moreover, when the second event occurs at $t = 0.16$ s the current reference is again greater than the current i_i but both current amplitudes have a difference of less than 0.04A. For this event, an overshoot of less than 1%, a maximum error during the transient of less than 0.5A and a settling time of 0.06s were observed. The minimum requirements established during the design stage for the inner current loop were fulfilled in both cases.

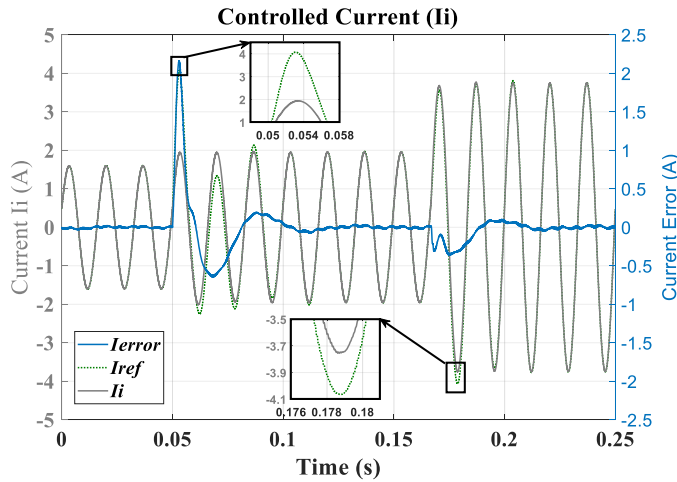


Fig 8. Inner Current (i_i) Loop Controller Performance

The outer voltage loop controller response is shown in Fig 9. The red signal is the voltage reference and the blue dotted signal is the voltage in capacitor v_c . It is observed that for the first event at $t = 0.05$ s the voltage error (green signal) has a maximum peak of 8.3V. In addition, v_c has an overshoot of less than 3% and a settling time of 0.07s, as well as a steady state error of less than 1%. Moreover, when the second event occurs at $t = 0.16$ s, the voltage v_c decrease close to 5.5V with respect to the reference, but it manages to stabilize and recover its value after 0.6s with a steady-state error of less than 1%. For both events, compliance with the requirements established during the design stage for the outer voltage loop was evidenced. In addition, it was shown that, although the design only considers the changes in the voltage reference, when performing disturbances in the load, a response is obtained from the system that meets the established requirements.

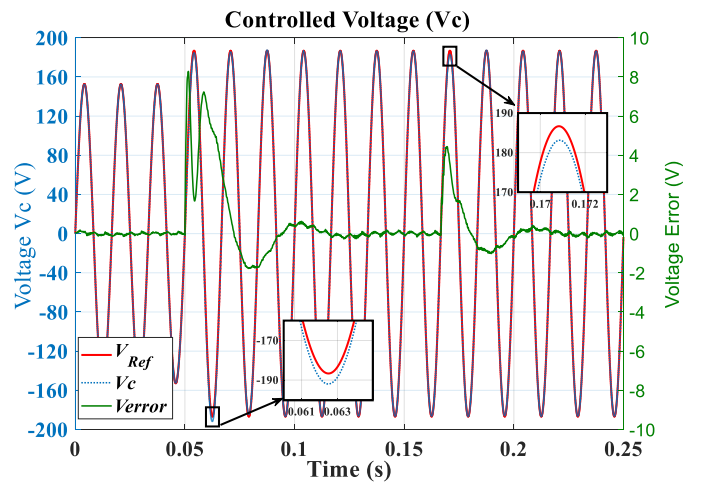


Fig 9. Inner Voltage (v_c) Loop Controller Performance.

CONCLUSIONS

In this paper, a formal methodology for the analysis and design of classical resonant proportional controllers in the discrete domain is presented using the Sisotool/Matlab tool. The proposed design methodology demonstrated simplicity using classical control requirements in basic design tools such as sisotool. Although it is designed only with variations in the voltage reference in mind, the system with two PR controllers in cascade presents a response within the established requirements when faced with sudden load disturbances.

REFERENCES

- [1] J. C. Vasquez, J. M. Guerrero, J. Miret, M. Castilla, and L. Garci, "Hierarchical Control of Intelligent Microgrids," no. December 2010, pp. 23–29, 1932.
- [2] S. M. Hakimi and S. M. Moghaddas-Tafreshi, "Optimal planning of a smart microgrid including demand response and intermittent renewable energy resources," IEEE Trans. Smart Grid, vol. 5, no. 6, pp. 2889–2900, 2014.
- [3] E. Dall'Anese, P. Mancarella, and A. Monti, "Unlocking Flexibility Shifting Supply and Demand Across Spatiotemporal Scales," no. February, pp. 43–52, 2017.
- [4] A. G. Yepes, F. D. Freijedo, Ó. López, and J. Doval-Gandoy, "High-performance digital resonant controllers implemented with two integrators," IEEE Trans. Power Electron., vol. 26, no. 2, pp. 563–576, 2011.
- [5] Y. Han, P. Shen, X. Zhao, and J. M. Guerrero, "Control Strategies for Islanded Microgrid Using Enhanced Hierarchical Control Structure with Multiple Current-Loop Damping Schemes," IEEE Trans. Smart Grid, vol. 8, no. 3, pp. 1139–1153, 2017.
- [6] F. Huerta, D. Pizarro, S. Cóbrecas, F. J. Rodríguez, C. Girón, and A. Rodríguez, "LQG servo controller for the current control of LCL grid-connected Voltage-Source Converters," IEEE Trans. Ind. Electron., vol. 59, no. 11, pp. 4272–4284, 2012.
- [7] X. Quan, Z. Wu, X. Dou, M. Hu, and A. Q. Huang, "Load Current Decoupling Based LQ Control for Three-Phase Inverter," IEEE Trans. Power Electron., vol. 33, no. 6, pp. 5476–5491, 2018.
- [8] A. G. Yepes, F. D. Freijedo, J. Doval-Gandoy, S. Lopez, J. Malvar, and P. Fernandez-Comesana, "Effects of Discretization Methods on the Performance of Resonant Controllers," IEEE Trans. Power Electron., vol. 27, no. 12, p. 4976, 2012.

- [9] A. S. B. Ribeiro, A. D. O. Almeida, P. G. Barbosa, and P. M. De Almeida, "Analysis and design of proportional-resonant controllers based on pole placement approach," SBSE 2018 - 7th Brazilian Electr. Syst. Symp., no. 1, pp. 1–6, 2018.
- [10] P. Cossoli, M. Caceres, L. Vera, A. Firman, and A. Busso, "Proportional-Resonant Controller and LCL Filter Design for Single-Phase Grid-Connected PV Micro-Inverters," Proc. 2018 IEEE PES Transm. Distrib. Conf. Exhib. - Lat. Am. T D-LA 2018, pp. 0–4, 2018.
- [11] M. S. Lima, L. A. D. S. Ribeiro, and J. G. De Matos, "Comparison analysis of resonant controllers in discrete domain taking into account the computational delay," 2015 IEEE 13th Brazilian Power Electron. Conf. 1st South. Power Electron. Conf. COBEP/SPEC 2016, vol. 1, pp. 1–6, 2015.
- [12] R. E. Carballo, F. Botterón, G. G. Oggier, and G. O. García, "A simple design approach for discrete time resonant controllers for UPS applications," 2015 16th Work. Inf. Process. Control. RPIC 2015, 2016.
- [13] F. B. Blaabjerg, K. Z. Zhou, D. W. Wang, and Y. Y. Yang, Periodic Control of Power Electronic Converters. Institution of Engineering and Technology, 2016.
- [14] IEEE Standard Association, IEEE Std. 1547-2018. Standard for Interconnection and Interoperability of Distributed Energy Resources with Associated Electric Power Systems Interfaces. 2018.