Velocity-Tuned Oscillators for NeuroSLAM and Spatial Navigation

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***Abstract*—In this paper, we present the implementation of Velocity Controlled (or tuned) Oscillators (VCO) to model spatial coding and navigation in the mammalian hippocampus. Specifically, we demonstrate these spatial cells by representing a spatial firing map of grid, place, and border cells. Since the VCO is the basis for Oscillatory Interference (OI) models based on the Spatial Envelope Synthesis (SES) approach of hippocampal and entorhinal navigation, we use these models in our hardware implementation to construct more complex spatial cells from simple interference between VCOs. We develop the design of a VCO ASIC chip containing up to 128 independently tuned VCOs.**

***Keywords*—Neuromorphic Computing, Low Power Navigation, SLAM, Velocity Controlled Oscillators**

I. Introduction

Research conducted over the past four decades suggests that various cells in the hippocampal formation provide a detailed representation of animals' current location and orientation. To this end, several major classes of spatially tuned neurons have been identified. Depending on their role in navigation, these neurons can be categorized as place cells, grid cells, and border cells [1], [2]. As the name suggests, place cells are activated when the animal visits a particular spatial location. By contrast the border cells exhibit activity when the animal encounters a boundary. Finally, grid cells fire at multiple locations which lie at the edges of a hexagonal lattice. From the neuroscience studies it is evident that animals, and by extension humans have a unique ability to utilize these spatially tuned cells to form maps of the environment. These studies have therefore triggered many researchers in the robotics community to investigate more cost effective, and power efficient algorithms for navigation and map formation inspired by the hippocampal models.

The idea of constructing a map of an environment as it is being explored is called Simultaneous Localization and Mapping (SLAM). SLAM is a standard and difficult problem in mobile robotics, and typically involves heavily over-sensored and mathematical complex algorithms. On the other hand, the neurally inspired version of SLAM, called NeuroSLAM or RatSLAM [3], offers a method that operates as under-sensored and ultra-low power algorithms [4]. Clearly, the NeuroSLAM approach to navigation promises performance that can mimic living organisms, which at this point, greatly surpasses the performance of artificial systems.

Previous neural SLAM implementations [3]–[6] take inspiration from general models of spatial coding and navigation in rat hippocampus and para-hippocampal regions. These implementations, while brain-inspired, do not explicitly model navigational cells in the brain or include biologically-plausible spiking neurons. The algorithmic organization reflects general principles of rodent navigation, but lower-level representations, transformations, and computations eschew neural implementations for traditional computational techniques. By failing to seek bio-plausibility, these models fail to take advantage of the power saving nature of neuromorphic systems, on both a software and hardware level [7].

Last year our group demonstrated an implementation of biologically faithful spatial coding cells in neuromorphic hardware [8]. Key to our implementation was the realization of Velocity Controlled (or tuned) Oscillators (VCOs) which mimic the role of theta oscillations in the cortex. In an effort to demonstrate a purely neuromorphic design, our previous work demonstrated the VCO functionality in an Integrate-and-Fire Array Transceiver (IFAT) device, which is a custom mixed mode chip capable of implementing an array of neurons with dynamically reconfigurable synapses [9]–[12].

In our implementation, each VCO was constructed by incorporating a feedback connectivity map inside an FPGA device, servicing the IFAT chip. While successful at implementing biologically relevant firing behavior of VCO cells, our proposed architecture suffered from a number of limitations inherent to IFAT. Particularly, while IFAT is ideal for implementing feedforward Convolution Neural Networks (CNN) to realize the Spatial Envelope Synthesis (SES) neurons to generate grid, place, and border cells, it struggles to implement many VCO cells in parallel, because of the number of feedback connections and large rate of spike feedback required.

In order to overcome the bottleneck in communication complexity and spike traffic density encountered when using neural arrays, such as the IFAT, to implement the VCOs, we are developing a custom VCO ASIC, described in this paper, to provide velocity tuned theta oscillations as input to the IFAT system. The IFAT will then combine the outputs of various oscillators, similar to a CNN, to implement the place, grid

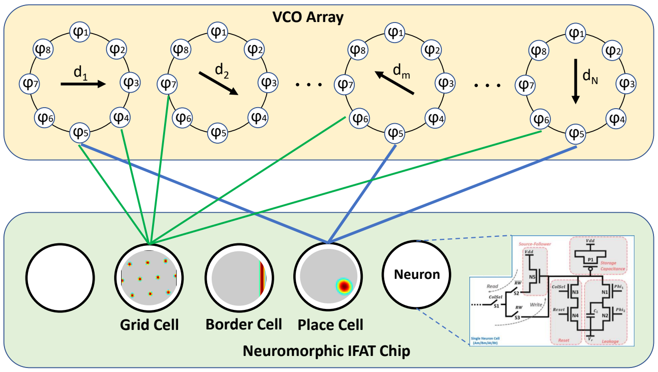

Fig. 1: Conceptual diagram of our biologically inspired spatial neurons. Following [13], theta firings are represented as Velocity Controlled Oscillators (VCO) whose frequency is modulated by the preferred movement direction and velocity. Output from multiple VCO units is projected neurons in the IFAT device with the connect matrix required to create place, grid or boarder cells when the animal reaches particular locations in space. Hence, the VCO and neurons work together to perform path integration, and the neurons only fire at specified locations in space. Various connectivity maps can be exploited in order to generate place cells, grid cells, and border cells.

and boarder cells (Fig. 1).

The paper is organized as follows. In section II we will provide a brief introduction of the underlying mathematical model for our VCO module. We will also introduce the Oscillatory Interference (OI) model which has been adapted from [14]. This model was first introduced in 2008 to describe the formation of spatially tuned neurons as interference between multiple VCOs with distinct preferred velocity and direction vectors. Section II concludes with a MATLAB simulation of the spatially tuned neuron firing process as it is relevant to SLAM. In Section III we will discuss our VCO ASIC implementation in 65 nm process. Finally we will conclude this paper by discussing our future directions.

II. Computational Models

Computational models of spatially tuned neurons aim to describe the firing behavior of the neural cells, encoding information about familiar locations. Given the inter-relationship between spatial location and velocity, these models often attempt to compute the animal's location by a process known as path integration (i.e. integrating the moving velocity over time). While many mechanisms have been proposed to describe interactions among VCO cells, in our design (Fig. 1) we chose to follow the Oscillatory Interference (OI) model proposed by Welday et al. [13]. This model represents the theta phase precession as VCOs whose operating frequency is modulated by the movement direction and speed, such that their firing phase is synchronized with displacement along a preferred direction. This model is particularly attractive from a hardware implementation standpoint as it creates a modular, low power, and highly re-configurable platform for generating spatially tuned neurons such as place cells, grid cells, and border cells.

A. Velocity Controlled Oscillator Model

As it was mentioned above, VCOs are the building block of the neurons formed by the OI model. The output of the nth VCO can be described as:

$$VCO_n(t) = \cos(\Phi_n(t)) \tag{1}$$

where:

$$\Phi_{n(t)} = \Phi_0 + \mathbf{d}_n \cdot \mathbf{[x(t)\text{-}x(0)]} \tag{2}$$

Given that the phase is related to frequency as $f = d\phi/dt$, each oscillator's frequency can be expressed in terms of its preferred movement direction and velocity according to the following equation:

$$f_{vco} = f_{base} + \mathbf{d} \cdot \mathbf{V} \tag{3}$$

Where f_{base} is the base frequency of oscillation. **d** and **V** are the VCO's preferred direction vector and the animal's instantaneous velocity vector, respectively. This expression can be decomposed in terms of the Cartesian coordinate system as:

$$f_{vco} = f_{base} + d_x \cdot v_x + d_y \cdot v_y \tag{4}$$

According to the OI model [13], neurons are formed when N VCO units with different phase offsets, and preferred directions interfere constructively at a given location. When the animal's velocity moves in its preferred direction, each VCO oscillates at its maximum angular frequency. On the other hand, each VCO operates at its minimum frequency when the animal's velocity vector is in the opposite orientation with respect to its preferred direction vector. Note, that in our implementation each VCO can output oscillations in 8 equally spaced phases (i.e. $\phi = n\pi/4$, where $n = 1, 2, ..., 8$).

B. Creation and Navigation of a Spatial Maze

A spatial map of a maze can be created in the hippocampus model establishing a sequence firing of place cells that tile space that the animal roams. As depicted in Fig. 2, border cells fire when the animal encounters a boundary in this 2D space maze. As the animal explores the space, a grid-like firing field appear across the 2D space. This shows that a grid cell responds when the animal is in particular locations in the room, and those places are spaced out in a hexagonal lattice [15].

III. Hardware Implementation

A. Architecture

The design of our VCO ASIC is in 65 nm CMOS technology. The circuit includes an array of 128 mixed-mode VCO units, each with a uniquely programmable preferred direction vector. Each asynchronous VCO unit will take in a common velocity input from an external sensor. As described in Eq.3, the frequency of oscillations for each VCO unit will be modulated according to the projection of the input velocity

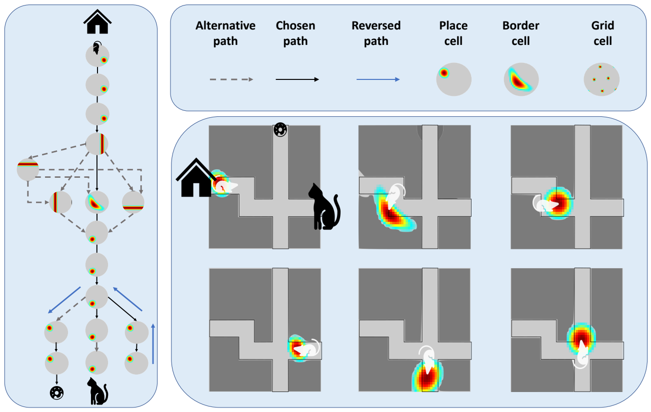

Fig. 2: Demonstration of the firing of place and border cells as the animal explores a maze in 2D space. The maze is representative of a few select states from the graph shown on the left. Black solid lines are the path the animal has taken, broken grey lines are other possible paths, and blue lines are paths that the animal had to travel in reverse in order to make it to its goal. The maze consists of three destination points, namely, “cheese”, “cat”, and “exit”. A place cell is fired at ”home”, followed by a border cell firing when the animal hits the boundary, changes direction, and hits another border cell. The animal continues its trajectory until it encounters a “cat” at the far end of the maze, and decides to change direction and hit an “exit” path. The animal finally changes its direction towards the “cheese”.

vector and the VCO unit’s preferred direction. The output event stream of the VCO chip will be presented to the IFAT chip as spikes, where grid, place, and border cells are created using the Spatial Envelope Synthesis (SES) approach. Each VCO has 8 taps, corresponding to different phase states in accordance with the analytical description provided in section II.

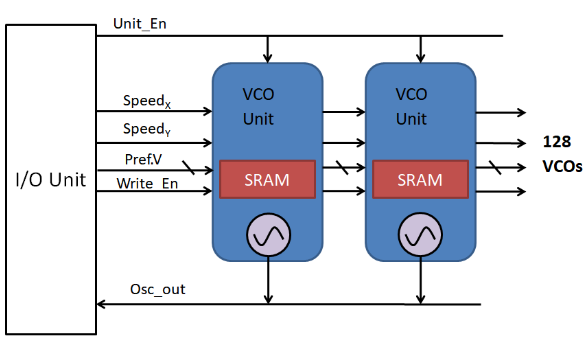

Fig. 3: Block diagram of VCO chip. Each VCO unit is individually enabled by the I/O unit. Current object speed, preferred velocity and its write enable are common to all units. The oscillation is outputted to one common pin.

Fig. 3 shows the block diagram of the VCO chip and its corresponding I/O connections. Fig. 4 shows the structure of our VCO unit cell. Each unit contains a local control I/O module through which the **X** and **Y** components of the preferred direction vector (i.e. d_x and d_y) are pre-loaded into the local SRAMs as a pair of 4-bit words. Each stored component of the

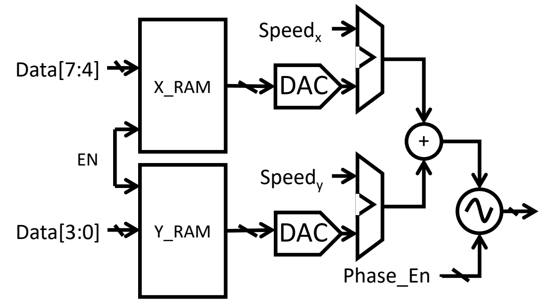

Fig. 4: Structure of the VCO unit. Each VCO unit converts the stored preferred vector to analog values then preform analog computation. The result controls the output oscillation.

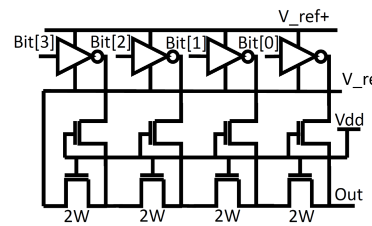

Fig. 5: W-2W transistor ladder DAC.

direction vector is then converted to an analog voltage using a W-2W digital to analog converter module (DAC) [16]. Key to our VCO implementation are the multiplier cells which calculate the instantaneous dot products between each VCO unit’s preferred direction and its instantaneous velocity (i.e. v_x and v_y). The outputs from the dot products units are further used to drive the frequency of output oscillations.

Below we will provide a brief discussion of our VCO’s building blocks.

1) SRAMs: The two 4-bit, sign + magnitude, SRAMs hold the preferred **X** and **Y** coordinates of the preferred direction vector. Each SRAM is preloaded with data upon start-up.

2) A/D Converters: The aim of our design is small area and low power. Since the stored preferred velocity vectors are not to be changed frequently after configuration, capacitance DACs that requires refreshment are not preferred here. We adopted a W-2W transistor ladder [16] with long transistor length to minimize the current consumption, shown in Fig. 5.

3) Analog Computation Module: The theta model for the VCO requires that the frequency is controlled by the inner product of the VCO unit’s preferred velocity and the current movement velocity. As illustrated in Fig. 6, in order to perform the dot product for each VCO unit with minimum power and area, we use two Gilbert cells to compute four quadrant multiplication that generate differential voltages as the product. Two pairs of differential voltages representing the product of x and y component is converted into two currents using stacked differential pairs, and the sum of the two currents is the result of the dot product.

4) Oscillator: The basic structure of the oscillator is a current starved ring oscillator, where the control current for the

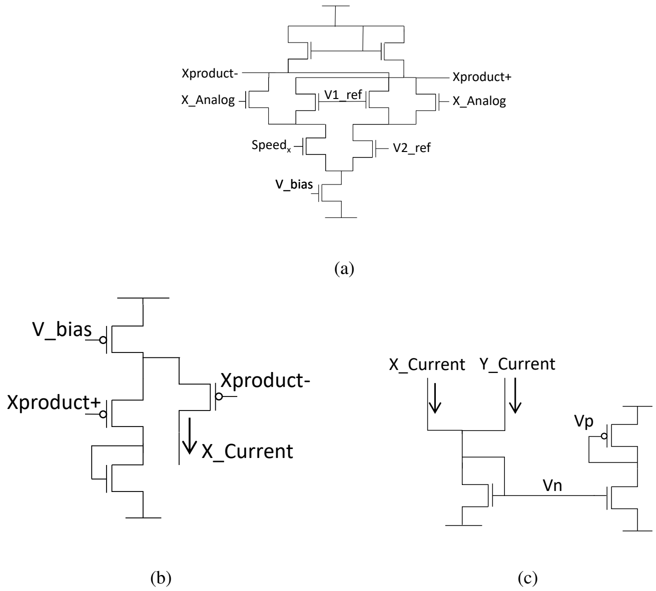

Fig. 6: (a) Gilbert four quadrant multiplier cell. (b) Differential voltage to current amplifier. (c) Current summation and bias generation for oscillator control.

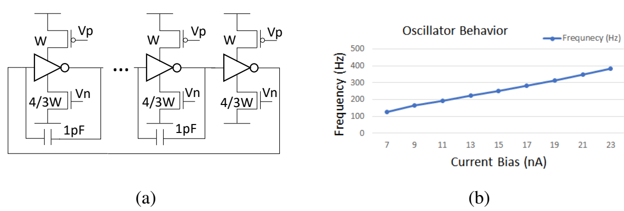

Fig. 7: (a) Parallel capacitance ring oscillator. (b) Oscillator behavior, current bias vs. the frequency.

ring oscillator is provided by the dot product circuit. In order to achieve a linear relation between current and frequency, as well as reduce the oscillation frequency, i.e. increase the effective capacitance of each stage of the oscillator, the inverters are connected in parallel with each delay capacitor, thus taking advantage of the Miller Effect, and ultimately reducing the capacitance needed down to 1pF each.

5) I/O unit: Since the oscillator's frequency is lower than 1000-Hz, it is possible to scan each oscillator signal using time multiplexing (TDMA). One long shift register with bypassing capability generate the enable signal for sampling the VCOs' oscillations as well as initial configuration. On startup, the shift register shifts through all phases of all VCO units. The preferred velocity stored in local VCO SRAMs, and which VCO or phase of which VCO to bypass is stored in an SRAM with equal length to that of the shift register. Only the desired VCO units and desired phase of those VCO units will then be output. This allows us to minimize the traffic on the output bus and to only access needed VCOs to construct the designed place, grid and border cells.

A ring oscillator is used in our implementation where we opted to widen the NMOS current mirror with a factor of

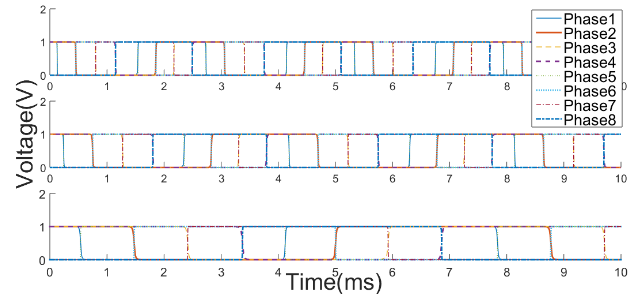

Fig. 8: Results of the oscillations displaying all the phases. The top subplot shows the oscillation when the preferred velocity coincides. The middle subplot shows the oscillation when the two vectors are orthogonal. The bottom subplot shows the oscillation when the two vectors are at opposite direction.

4/3 to achieve a *50%* duty cycle of oscillation across the range of operation frequency in order to get VCO outputs as shown in Fig. 7. Additionally, as a representative example Fig. 8 shows the operation of a VCO unit with a constant input velocity held at ($v_{xmax} = a, v_{ymax} = a$). When the preferred direction vector is in line with the input velocity, the frequency is maximized at 363-Hz. By contrast, when the preferred direction vector is orthogonal to the input velocity (i.e. $d_x = 1, d_y = -1$), VCO will run at its base frequency of 250-Hz. Finally, if the preferred direction vector is in opposite direction to the input velocity (i.e. $d_x = -1, d_y = -1$), the lowest frequency of 136-Hz is achieved.

B. Power Consumption

The power consumption will vary under various conditions, such as output clocking speed, input velocity, bypassed units, and the setup for preferred velocities for each VCO unit. The power of a typical VCO unit will range around 2μW, thus the total power of the VCO chip containing 128 VCO units is expected to be under 300μW.

IV. Discussion

In this paper, we present an implementation of spatial cells by representing a spatial firing map of grid, place, and border cells. Furthermore, we develop the design of a mixed mode VCO ASIC to serve as an input layer to the Integrate-and-Fire Array Transceiver (IFAT). This chip contains up to 128 independently tuned VCOs, each allowing 8 phases to be tapped. In moving forward with concurrent software and hardware development, we set out to implement this VCO model on the IFAT developed by Molin et al. [12]. In doing so, we are able to implement complex spatial networks on low-power neuromorphic hardware. Hence, this neural system can provide a robust, low-power, and bio-plausable neurally-inspired model for robotic navigation and guidance systems for autonomous mobile robots.

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