Radiation Hardened Memory and Logic using Phase Transition Material

Jaydeep P.Kulkarni
Department of Electrical and Computer Engineering
University of Texas at Austin
Austin, Texas
Email: jaydeep@austin.utexas.edu

S.S. Teja Nibhanupudi
Department of Electrical and Computer Engineering
University of Texas at Austin
Austin, Texas
Email: subrahmanya_teja@utexas.edu

***Abstract*— Soft error tolerant circuits have been presented with Phase Transition Material (PTM) as technology assists. PTM leverages the large insulating state resistance to block the propagation of glitches to subsequent stages thereby preventing data loss due to radiation strikes. Delay penalty is minimal due to voltage delta dependent switching to the metallic phase thereby offering an optimal rad-hard solution. Detailed PTM parameter design space exploration is presented for improved soft error performance. The soft error improvement in standard logic gates and 6T SRAM bit cell are quantified.**

Keywords*— *Phase Transition Material (PTM), Soft Error Tolerance (SET), Critical Charge

I. Introduction

With scaling feature sizes and operating voltages, the sensitivity of Integrated circuits (IC's) to high-energy particle strikes has significantly increased [1-3]. Cosmic rays present in the space environment and radio-active elements present in semiconductor packaging materials are the source of these high-energy particles. These high-energy particle strikes may result in data loss of single bit (Single Bit Upset) or multiple bits (Multi bit upset) in memory/logic circuits. Especially, the electronic circuits designed for space applications need to be robust to sustain the high LET (Linear Energy Transfer) strikes.

Redundancy techniques such as TMR (Triple Modular Redundancy) [4], DMR (Dual Modular Redundancy) [5] have been adopted to enhance the immunity of circuits to particle strikes. Further, specialized bit-cell configurations such as DICE (Dual Interlocked) cell [6], Quatro cell [7] have been proposed to reduce the sensitivity of SRAM storage nodes to particle strikes. However, these approaches incur significant area and performance penalty. Hence, there is a critical need to develop circuit topologies with minimal delay, area and power overheads while achieving improved soft error tolerance.

In this paper, we present Phase Transition Material assisted circuits for improved soft-error tolerance of memory/logic circuits with minimal performance and zero area penalty. The key contributions of the paper are:

1. We present PTM as technology assist to enhance the immunity of logic and memory to soft-errors.
2. We discuss heterogenous back end of line (BEOL) integration of these materials onto baseline CMOS circuits.
3. We quantify the soft error performance of PTM assisted SRAM bit cell for single event upset (SEU) particle strike and compare with other CMOS variants.
4. We present design space exploration study to understand the impact of PTM parameters on soft-error performance.
5. We propose PTM assisted logic circuits for reduced glitch propagation

II. Phase Transition Material

A. Phase Transition Material

Transition metal oxides such as VO_2, NbO_2 exhibit abrupt insulator-metal transition under the influence of an external electric field owing to interaction of charge, lattice, orbital and spin degrees of freedom [8-9]. This novel property is being exploited to realize transformational circuit topologies such as hyper-FET and selector for crossbar memory arrays [10-11]. In this work, we propose soft-error tolerant circuits by leveraging the abrupt resistance switching property of these materials. The PTMs suppress the high-energy particle strike induced glitch propagation in logic and prevent bitflips in memory. Also, the intrinsic switching of the PTM filters out narrow pulse-width radiation strikes thereby by further enhancing the soft-error immunity of the circuits.

B. Phase Transition Material based MIM fabrication

Two terminal M-I-M (Metal-Insulator-Metal) structures have been fabricated by sandwiching VO_2 thin film in between metal electrodes. 100nm thick VO_2 thin film has been deposited by thermal evaporation of commercially available VO_2 powder.

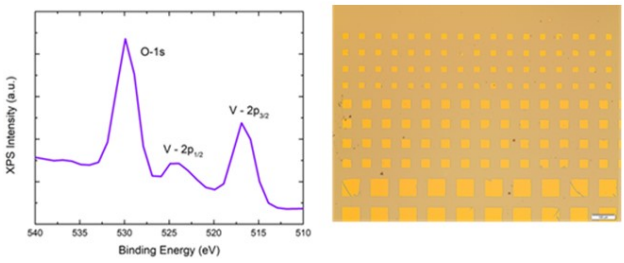

Fig. 1 Measured XPS and top view of fabricated VO_2 M-I-M structures

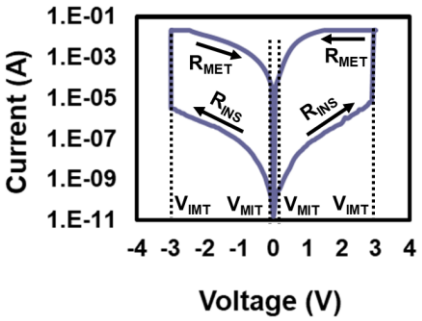

Fig. 2 Measured I-V characteristics: VO_2 M-I-M structures

ρ_{MET}	$5x10^{-3}$ Ω-cm
ρ_{INS}	1 Ω-cm
J_{CMIT}	10^6 A/cm^2
J_{CIMT}	$4x10^4$ A/cm^2
L_{PTM}	36 nm
A_{PTM}	36 nm x 20 nm

Table.1 PTM parameters

The thin film has been deposited on n++ silicon substrate which also served as bottom electrode. Fig.1 shows the XPS profile of the deposited VO_2 thin film. Nickel metal was deposited to serve as the top electrode. The deposited nickel was patterned to form vertical isolated MIM structures of varying dimensions as shown in Fig.1. The fabricated MIM structures exhibited the I-V characteristics as shown in Fig.2.

C. *Electrical Characteristics*

The I-V characteristics of the PTM based MIM structures can be modelled using few parameters shown in Table.1 [12]. $\rho_{INS/MET}$ correspond to resistivity of the PTM in insulating state and metallic state respectively. J_{CMIT}/J_{CIMT} correspond to the current density in insulating state and metallic state respectively. L_{PTM} represents the thickness of the thin film and A_{PTM} represents the area of cross-section of the MIM structure. Under zero bias condition, the PTM is in insulating state ($R_{INS} = \rho_{INS} \times L_{PTM} / A_{PTM}$). As the applied voltage bias increases, very little current flows through the PTM device ($I=V/R_{INS}$). When the current through the device reaches the I_{IMT} ($I_{IMT} = J_{CIMT} \times A_{PTM}$) threshold, phase transition is triggered and the PTM becomes metallic. The corresponding voltage is referred to as V_{IMT} threshold ($V_{IMT} = I_{IMT} \times R_{INS}$). In the metallic state, large current flows in the circuit owing to the small resistance ($R_{MET} = \rho_{MET} \times L_{PTM}/A_{PTM}$). The PTM device remains in the metallic state for all the voltages above V_{IMT} threshold. The PTM device exhibits hysteresis behavior and the reverse phase transition to insulating phase is triggered when the current reduces to I_{MIT} ($I_{MIT} = J_{CMIT} \times A_{PTM}$) threshold. The corresponding voltage is referred to as V_{MIT} threshold ($V_{MIT} = I_{MIT} \times R_{MET}$). The PTM device exhibits similar behavior as the applied voltage polarities are reversed. Also, the PTM device requires finite time to switch from insulating phase to metallic phase and vice versa. This duration is referred to as intrinsic switching time (T_{PTM}) and has been observed to be in the sub-nanosecond regime [13-14].

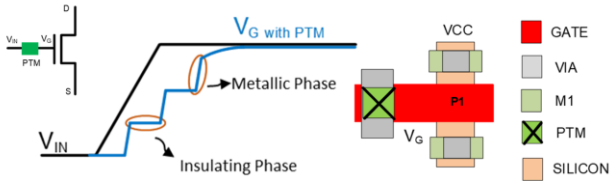

Fig.3 Soft-FET schematic, transient response and layout

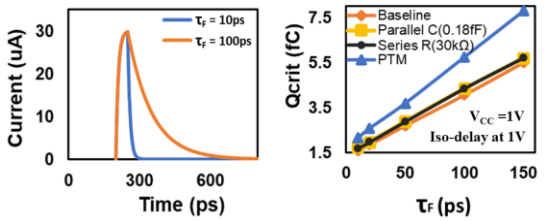

Fig.4 Double exponential current spike and Q_{CRIT} variation with fall time constant, τ_F

D. *Soft-FET*

The PTM device when placed in series with the gate of MOS transistor is referred to as "Soft-FET" [15]. The Soft-FET exhibits unique soft switching transient behavior on a ramping input voltage as shown in Fig.3. However, the DC characteristics of the Soft-FET remain unaltered as compared to baseline MOS transistor. The transient behavior of the Soft-FET is determined by the abrupt resistive switching property of the PTM. The gate terminal of the Soft-FET can be modelled using an $R_{PTM}C_G$ circuit. Where R_{PTM} corresponds to the resistance of the PTM and C_G is the gate capacitor. Under zero bias condition ($V_G=V_{IN}= 0$), the PTM is in insulating state. As the input voltage V_{IN} increases, the gate capacitor is charged with a large associated time constant ($R_{INS}*C_G$). Hence, the V_G voltage rises slowly (horizontal portion of staircase waveform) leading to increasing voltage difference (V_{IN}-V_G) across the PTM. When, the (V_{IN}-V_G) voltage reaches the V_{IMT} threshold, phase transition is triggered and PTM becomes metallic in nature. In the metallic state, the gate capacitor is charged quickly owing to small associated time constant ($R_{MET}*C_G$). Hence, the V_G voltage rises rapidly (vertical portions of the staircase waveform) leading to reducing voltage difference across the PTM (V_{IN}-V_G). When the (V_{IN}-V_G) voltage reaches the V_{MIT} threshold, reverse phase transition to insulating phase is triggered. This alternating slow and quick charging cycles continues until $V_G=V_{CC}$ resulting in staircase waveform as shown in Fig. 3.

E. *Phase Transition Material Integration*

The PTM can be integrated onto baseline CMOS through back end of line (BEOL) integration techniques as highlighted in Fig. 3. Therefore, the PTM can be envisioned as 'special via' contact at the gate input and would not incur any area penalty. Hence, the PTM assisted circuits can offer better area scaling compared to previously proposed radiation hardening circuit techniques requiring additional transistors.

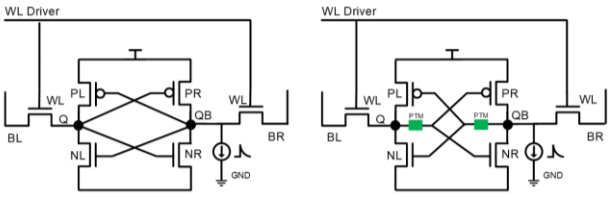

Fig.5 SRAM schematic without and with PTM

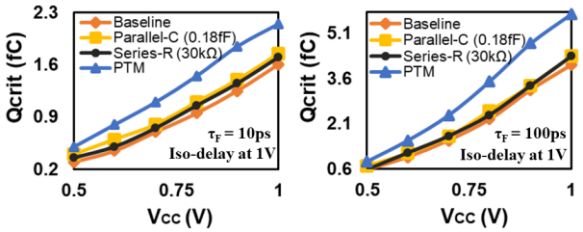

Fig. 6 Q_{CRIT} variation with supply voltage for τ_F=10 ps strike (left) and τ_F=100 ps strike (right)

III. Radiation Hardened PTM Assisted SRAM Bitcell

A. Simulation Setup

The proposed PTM assisted radiation hardened circuits have been evaluated through SPICE simulations using commercial 40nm CMOS process technology. The PTM I-V characteristics have been represented using phenomenological Verilog-A model [16]. The radiation particle strike has been emulated using a current source with the double exponential waveform [17] as shown in Fig.4. The τ_R and τ_F parameters correspond to rise and fall time constants of the spike respectively. The radiation particle strike pulse-widths have been chosen to vary between 10ps to 100ps based on earlier study of radiation strikes on advanced technology nodes [18-19]. A radiation strike can accumulate sufficient charge to aid the (1→ 0) transition or (0 → 1) transition. In the (1→ 0) transition as the weaker PMOS transistor provides the restoring current and therefore is the worst case radiation strike. Hence, this 1 → 0 node transition is chosen for all the simulations in this study.

B. PTM assisted 6T SRAM bitcell

High density SRAM arrays with minimum dimension transistors are more vulnerable to radiation strike induced bitflips. We propose PTM assisted SRAM bitcell to improve immunity against radiation strikes. The schematic of the PTM assisted 6T SRAM bitcell is shown in Fig. 5. The radiation strike has been positioned at the QB storage node storing logic '1'. The strike has to traverse through the PTM in order to impact the storage node Q. The presence of PTM hinders this propagation through the following mechanisms,

1. The PTM in insulating state delays the propagation of the spike owing to large associated R_{INS}*C_G time constant. Therefore, radiation strikes which cannot trigger the insulator-metal transition are completely filtered out prior to reaching the storage node Q.
2. Even if the radiation strike has sufficient energy to trigger the insulator-metal transition, the PTM requires intrinsic switching time to complete the transition. Therefore, the radiation strikes with pulse-width smaller than the intrinsic switching time are compensated by the restoring currents prior to impacting the storage node Q. Further, the immunity is enhanced by the presence of two PTMs in the positive feedback loop (QB → Q → QB).

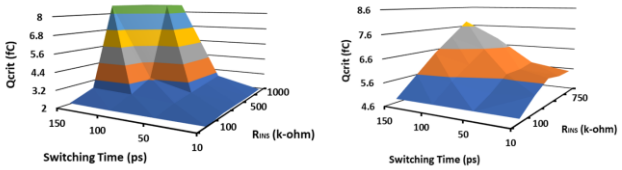

Fig.7 Q_{CRIT} variation with switching time and insulating resistance for (τ_F=10 ps) and (τ_F=100 ps)

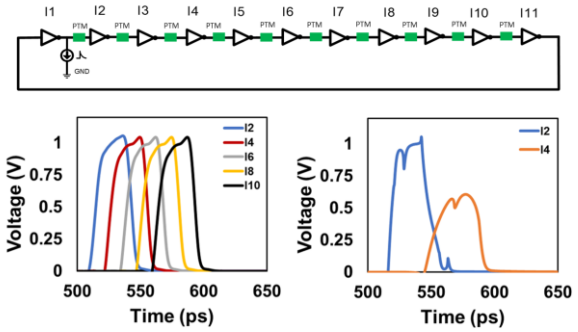

Fig.8 PTM assisted ring oscillator schematic (top) and Glitch propagation along the inverter chain for baseline (left) and PTM assisted inverter chain (right)

In summary, the PTM effectively blocks the radiation strikes either with smaller amplitude or with smaller pulse-widths. In addition, the PTM hinders the propagation of high-energy strikes thereby improving the immunity of the circuit. It should be noted that the PTM affects only the small signal transients such as radiation strikes/glitches. However, the large signal voltages can trigger the phase transition and therefore the SRAM write-time is not significantly affected.

C. Simulation Results

SPICE simulations are performed to evaluate the performance of the PTM assisted SRAM bitcell using critical charge (Q_{CRIT}) as the metric. Critical charge is the minimum amount of charge required to flip the data stored in the SRAM bitcell. Radiation tolerant SRAM bitcell are designed to exhibit Q_{CRIT} value compared to baseline SRAM bitcell. To evaluate the soft error improvement of the PTM assisted SRAM bitcell, two other CMOS variants (Series-Resistor and Parallel-Capacitor) have also been compared. The Series-Resistor bitcell scenario is similar to the PTM assisted bitcell with PTM replaced with resistor. The Parallel-Capacitor bitcell scenario is the baseline bitcell with capacitor connected to storage nodes. These scenarios have been chosen as they increase the Q_{CRIT} of the SRAM bitcell. For the purpose of fair comparison, three scenarios are analyzed to (PTM, Series-R, Parallel-C) to have the same delay at 1V (iso-write-time at 1V). Fig. 4 shows the

variation of QCRIT with fall time constant. The PTM assisted SRAM bitcell shows ~1.5x improvement in the Q_{CRIT} at large pulse-width strikes. Although, the PTM in insulating phase incorporates delay, the PTM in metallic phase compensates for the delay penalty leading to reduced overall delay. Fig.6 shows the improved performance of the PTM assisted bitcell across voltage range for smaller pulse-width strikes and larger pulse-width strikes. The proposed design achieves 1.3x and 1.4x improvement in the Q_{CRIT} for small pulse-width and large pulse-width strikes respectively.

D. Design Space Exploration

The intrinsic switching time and insulating state resistance of the PTM determine the soft-error performance. A design space sensitivity analysis is performed to understand the impact of these parameters on the Q_{CRIT}. The insulating state resistance can be altered by scaling the device dimensions ($R_{INS} = \rho_{INS} \times L_{PTM} / A_{PTM}$). However, varying L_{PTM} also impacts the voltage thresholds ($V_{MIT/IMT} = \rho_{MET/INS} \times J_{CMIT/CIMT} \times L_{PTM}$) which can affect the soft-error tolerance. Hence, only A_{PTM} parameter is scaled to vary the insulating state resistance. The intrinsic switching time, on the other hand is a strong function of the growth-techniques/fabrication process. The Q_{CRIT} variation with switching time and insulating state resistance is shown in Fig. 7 for (τ_F = 10ps) pulse-width and (τ_F = 100ps) pulse-width strikes. It is evident that Q_{CRIT} increases with both switching time and insulating state resistance based on the two explained mechanisms. For the (τ_F=10ps) scenario, the bitcell does not flip for large T_{PTM} and large R_{INS} (peaks in Fig.7 beyond the Y-axis maxima). This is due to the large propagation delay compared to pulse-width of the radiation strike. Based on the design space exploration study, an optimized PTM with large R_{INS}, low V_{IMT} and moderate T_{PTM} can yield higher soft-error tolerance with minimal delay penalty.

IV. RADIATION HARDENED PTM ASSISTED LOGIC

We propose the integration of PTM onto baseline CMOS logic circuit for improved soft-error performance. Fig. 8 shows the schematic of 11-stage ring oscillator with PTM inserted at each stage (Soft-FET based inverter). The Q_{CRIT} in logic is defined as the minimum charge required to generate a glitch of 50% V_{CC} magnitude at the next stage output. The PTM assisted logic effectively filters out spikes/glitches with few stages as shown in Fig. 8 For fair comparison, an iso-radiation strike of 60uA amplitude and 20ps τ_F was applied to the first stage of ring oscillator with/without PTM. I2, I4, I6, I8 and I10 correspond to output node of the 2nd, 4th, 6th, 8th and 10th stages of ring oscillator. It is evident that PTM assisted logic gates filter out the radiation induced glitches within 4 stages whereas the baseline circuit experiences the glitch propagation across all stages.

V. CONCLUSION

In this work, we present soft-error tolerant circuits designed with PTM as technology assists. The proposed PTM assisted SRAM bitcell shows ~1.35x improvement in Q_{CRIT} compared to other CMOS variants. This improvement can be achieved at zero silicon area overhead and minimal delay overhead. Transistor up-sizing/or transistor V_T can be optimized to further reduce the delay penalty. Experimental investigations on these materials have shown reliability > 10^9 cycles suggesting the suitability for large scale industry applications [20]. Optimization of PTM parameters can further enhance the soft-error performance of logic/memory circuits.

VI. REFERENCES

[1] N. N. Mahatme et.al., "Impact of technology scaling on the combinational logic soft error rate." In *Reliability Physics Symposium, 2014 IEEE International*, pp. 5F-2. IEEE, 2014.

[2] I. Chatterjee et.al., "Impact of technology scaling on SRAM soft error rates." *IEEE Transactions on Nuclear Science* 61, no. 6 (2014): 3512-3518

[3] R.C.Baumann, "Radiation-induced soft errors in advanced semiconductor technologies" *IEEE Transactions on Device and materials reliability*, *5*(3), pp.305-316.

[4] L. E. Robert et.al., "The use of triple-modular redundancy to improve computer reliability." *IBM Journal of Research and Development* 6, no. 2 (1962): 200-209.

[5] T. John "Self-voting dual-modular-redundancy circuits for single-event-transient mitigation." *IEEE Transactions on Nuclear Science* 55, no. 6 (2008): 3435-3439.

[6] T. Calin et.al., "Upset hardened memory design for submicron CMOS technology." *IEEE Transactions on Nuclear Science* 43, no. 6 (1996): 2874-2878

[7] S.M. Jahinuzzaman et.al., "A soft error tolerant 10T SRAM bit-cell with differential read capability" *IEEE Transactions on Nuclear Science*, *56*(6), pp.3768-3773.

[8] G. Stefanovich et.al., "Electrical switching and Mott transition in VO2" *Journal of Physics", Condensed Matter*, *12*(41), p.8837, 2000.

[9] J. Park et.al., "Multilayered NiOx/NbOy/NiOy fast drift free threshold switch with high Ion/Ioff ratio for selector application", Scientific Reports.

[10] N. Shukla et.al., "A steep-slope transistor based on abrupt electronic phase transition." *Nature communications* 6, pp.7812, 2015.

[11] M. Son et.al.,"Excellent Selector Characteristics of Nanoscale VO2 for High-Density Bipolar ReRAM Applications." *IEEE Electron Device Letters* 32, no. 11, pp.1579-1581, 2011

[12] A. Aziz et.al., "COAST: Correlated material assisted STT MRAMs for optimized read operation" In *Low Power Electronics and Design (ISLPED), 2015 IEEE/ACM International Symposium on* (pp. 1-6). IEEE.

[13] M. Jerry et.al., "Dynamics of electrically driven sub-nanosecond switching in vanadium dioxide", In *Silicon Nanoelectronics Workshop (SNW), 2016 IEEE* (pp. 26-27). IEEE, 2016.

[14] S. Srinivasa et.al., "Correlated material enhanced SRAMs with robust low power operation", *IEEE Transactions on Electron Devices*, *63*(12), pp.4744-4752, 2018.

[15] S. Teja and J.P. Kulkarni, "Soft-FET: phase transition material assisted soft switching field effect transistor for supply voltage droop mitigation", In *Proceedings of the 55th Annual Design Automation Conference* (p. 76). ACM, 2018.

[16] W.Y. Tsai et.al., "Enabling new computation paradigms with HyperFET-an emerging device", *IEEE Transactions on Multi-Scale Computing Systems*, *2*(1), pp.30-48, 2016.

[17] T. Heijmen et.al., "Factors that impact the critical charge of memory elements" In *On-Line Testing Symposium, 2006. IOLTS 2006. 12th IEEE International* (pp. 6-pp). IEEE.

[18] S.V. Walstra et al., "Circuit-level modeling of soft errors in integrated circuits" *IEEE Transactions on Device and Materials Reliability*, *5*(3), pp.358-364.

[19] R.C. Harrington et al., "Estimating Single-Event Logic Cross Sections in Advanced Technologies" *IEEE Transactions on Nuclear Science*, *64*(8), pp.2115-2121.

[20] J. Frougier et.al., "Phase-transition-FET exhibiting steep switching slope of 8mV/decade and 36% enhanced ON current," in *Proc.* IEEE *VLSI Technology Symposium, 2016, pp. 1-2*