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Modeling of FinFET SRAM array reliability degradation due to electromigration

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A B S T R A C T

Effective assessment of degradation induced by electromigration (EM) is necessary for the design of reliable circuits based on FinFET technology. In this paper, a new methodology is proposed where FinFET SRAM cell array activity is used to evaluate the resistance degradation due to EM. The implementation of this methodology consists of analysis of stress evolution, a time-dependent resistance model, cell array activity extraction, and a customized algorithm for cell array reliability evaluation. The stress model is derived from the material transport equation which contains the driving forces due to the gradient of vacancy concentration, temperature, hydrostatic stress, and EM itself. The time-dependent resistance shift describes the effect of stress evolution. The customized algorithm is applied to calculate the resistance degradation while considering the characteristics of metal wire arrays in SRAMs. The statistical degradation in a FinFET SRAM cell array reveals that, for the tested case, in addition to the percentage of the workload in various operating modes, the cell array activity distribution also affects EM degradation. More evenly distributed cell activity results in better EM reliability.

1. Introduction

A FinFET circuit is stressed and degraded during operation by various front-end wearout mechanisms, such as Bias Temperature Instability (BTI), Hot Carrier Injection (HCI), and Gate-oxide Time Dependent Dielectric Breakdown (GTDDB), and by back-end wearout mechanisms such as Electromigration (EM) [1–10]. In light of the International Technology Roadmap for Semiconductors (ITRS) report 2015, the expected operating current density ranges between 1 MA/cm^2 and 10 MA/cm^2 in recent years. As this current density continues to increase, interconnect failure induced by EM continues to be an important and long-standing issue for the achievement of reliable CMOS semiconductor circuits and systems [11]. It has been observed that EM-induced degradation is more significant for FinFETs in advanced technology nodes, where the dual damascene structure, shown in Fig. 1(a), is adopted [12].

Fig. 1(b) illustrates two cases for EM, considering the electron flow direction, the void formation in the via-below (early failure mode) case and the void formation in the via down-above (later failure mode) case, which are shown on the left and right side of the figure, respectively. It is necessary to build an accurate methodology to study degradation due to EM for both cases.

This study focuses on the degradation of a FinFET SRAM cell array due to EM. The SRAM is important since SRAM arrays occupy most of the area of advanced microprocessors. In an SRAM, the metal lines suffering from EM, include Bit-lines, power lines, and ground lines. This study focuses on the Bit-lines. Since the power/ground lines are relatively wider and their resistance shift in a practical range doesn't have obvious effects on the cell's performance metrics, their EM induced resistance shift is less important. The other short interconnects are considered to be EM immortal because of their short length or because of the small current density flowing through them [13].

In the traditional approaches for evaluating EM-induced failure, a mean-time-to-failure (*MTTF*) is calculated for each metal wire segment using Black's equation and the Blech limit in Eqs. (1) and (2):

$$MTTF = Aj^{-n} \exp(E_a/k_B T) \tag{1}$$

$$(jL)_{crit} = \frac{\Omega \sigma_{crit}}{eZ^*\rho} \tag{2}$$

where A and n are fitting constants, j is the effective density of current flowing through metal line, E_a is the activation energy, T is the temperature, and k_B is the Boltzmann constant. Ω is the atomic volume, σ_{crit} is the critical stress for void formation, e is the electron charge, Z^* is the effective charge number, ρ is the metal wire electrical resistivity, and L is the length of interconnect segment.

The segments with a jL product smaller than $(jL)_{crit}$ are considered as EM immortal. Then the overall circuit lifetime can be evaluated by combining the lifetime distributions of each segment. It is fast and easy to assess circuit EM degradation with this method, especially for very large scaled circuits, and this methodology is convenient for estimating the impact on the accelerated life test results. However, since the traditional method ignores atom flow throughout segment trees, the

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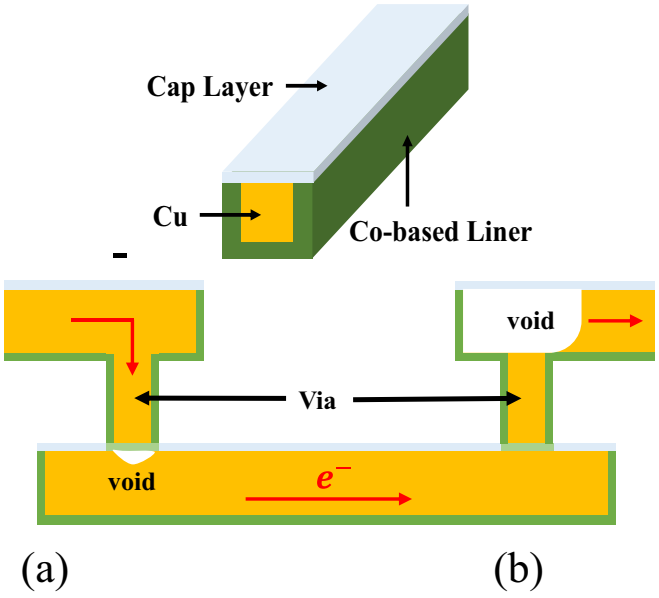


Fig. 1. (a) Cu dual damascene conductor structure, where the trench is lined with a Cobalt-based liner and the Cu is capped with either a dielectric or metallic layer. (b) A Cu wire connected with a via-below (left) and a via-above (right) [11].

lifetime of each segment is calculated separately and the interaction between adjacent segments is not included properly, the traditional approach could be pessimistic and inaccurate [13–15].

As shown in [10], both the series model and mesh model based on Black's equation lead to too pessimistic prediction of EM lifetime compared with a physics-based model. For a series model, the circuit is considered to have failed when any branch fails. For a mesh model, extra redundancy is taken into consideration [10]. It is found in [10] that the EM lifetime of IBMPG2 predicted with the series model and the mesh model is 7.82 years and 10.67 years, respectively, while the lifetime predicted by a physics-based EM model is 15.66 years. Therefore, we should use more practical models for EM evaluation, although they result in a slower calculation speed.

There are two models for electromigration: the physics-based model (transient model) and the voltage-based model (steady state model) [16,17]. The physics-based model can provide accurate stress and resistance shift evolutions, but it needs much time for simulations. Although the voltage-based model is faster, it can only provide the stress distribution on interconnect segments in steady state. It is more practical and convincing to evaluate the EM degradation with a physics-based model which is time- and workload-dependent.

In this paper, an EM model based on material transport is applied to emulate the wearout of a FinFET SRAM array. Considering the features of interconnect structures, a customized programming process is designed and applied for FinFET SRAM EM simulation. The modeling methodology is also applicable for planar CMOS SRAM, except for the fact that the cells' arraignment is a little different, which would require a different strategy for deriving the effective current density over each interconnect segment.

Four steps are performed for the degradation calculation. First, the partial differential equations (PDE) for hydrostatic stress evolution obtained from material transport are discretized with the explicit finite difference method (FDM). Secondly, the current distribution needed for solving for hydrostatic stress is extracted from Hspice simulations while considering the cell configuration, temperature, and process variations. Also, the cell array activity distribution is extracted with different workloads and input data. Next, the EM degradation of the SRAM cell array is evaluated step by step with the discretized PDE, current distribution, and activity distributions.

The novelty of this paper is reflected in the following aspects: a) a methodology is proposed involving existing equations for hydrostatic stress to find the resistance shift due to EM, in order to evaluate SRAM cell performance degradation vs. time, b) the operating current is modeled with regression to make the computation of hydrostatic stress evolution for cells indifferent positions in the array more efficient, and c) a customized algorithm for a 32Kb FinFET SRAM cell array is designed and implemented for wearout simulation of the full system, while taking into account use scenarios.

The rest of this paper is arranged as follows. Section II 2 introduces the comprehensive EM model and the FinFET SRAM cell array to be explored. Section III 3 presents the methodology for developing a compact current model during each operation using multivariate adaptive regression splines (MARS), and for simulating the cell array activity. Section IV 4 discusses the application of the EM model to the FinFET SRAM cell array with a customized algorithm. The distribution and characteristics of EM-induced degradation is shown explicitly. The influence of workload and activity distribution on EM degradation is also discussed. Section V 5 concludes the paper.

2. EM model and the FinFET SRAM cell array

2.1. Fundamental equations and validations

One dimensional material transport for an atom is expressed as [16],

$$\frac{\partial \sigma}{\partial t} = \frac{\partial}{\partial x}\left[\frac{D_a B}{k_B T}\left(\Omega\frac{\partial \sigma}{\partial x} - |Z^*|\, e\rho_{Cu} j - Q^*\frac{\partial T}{\partial x}\right)\right] \tag{3}$$

$$\vec{j_a} = \frac{D_a C_a \Omega}{k_B T}\left[\frac{\partial \sigma}{\partial x} - \frac{|Z^*|\, e\rho_{Cu} j}{\Omega} - \frac{Q^*}{\Omega}\frac{\partial T}{\partial x}\right] \tag{4}$$

where $D_a = D_0\, exp\,(-E_a/k_BT)$, D_0 is a constant, B is Young's Modulus, Ω is atom volume, e is the elementary charge, ρ_{Cu} is copper resistivity, j is current density, Q^* is the heat of transport, C_a is the atom concentration, Z^* is the effective charge number, $\vec{j_a}$ is atomic flux, and σ is the hydrostatic stress.

The explicit Forward Time Centered Space (FTCS) scheme [18] is adopted to solve the PDE system because of its easy implementation and ensured stability for the time scale of SRAM operations. The gradient of temperature and current density in each segment is neglected since they have a negligible impact on the results. After this simplification, the equations become equivalent with the Korhonen model and the other similar models [17,19–21].

Dirichlet boundary and Neumann boundary conditions are applied. The model phase and the location of nodes determine what needs to be applied to edge nodes of each branch. Given the boundary conditions and the equations, only the initial conditions are needed for the complete solution of the FTCS FDM. Initial conditions are determined by the material difference in the coefficients of thermal expansion (*CTE*). The *CTE* mismatch of the interconnect and its confinement causes thermal stress during fabrication. The initial value, which is the thermal stress distribution at $t = 0$, is expressed as [22]

$$\sigma(x, t = 0) = B(a_M - a_{Conf})(T_{ZS} - T(x, t = 0)) \tag{5}$$

where T_{ZS} is the stress free annealing temperature, $T(x, t = 0)$ is the specific node temperature at $t = 0$, and a_M and a_{Conf} are the *CTE* of the metal and confinement materials, respectively.

The EM model applied in this paper consists of three phases: the nucleation phase, the vertical growth phase, and the horizontal growth phase [23]. Hydrostatic stress evolves throughout the three phases with initial and boundary conditions. In phase I, the interconnect resistance remains unchanged before the maximum stress exceeds a threshold. After the maximum stress at the interconnect edge exceeds a threshold,

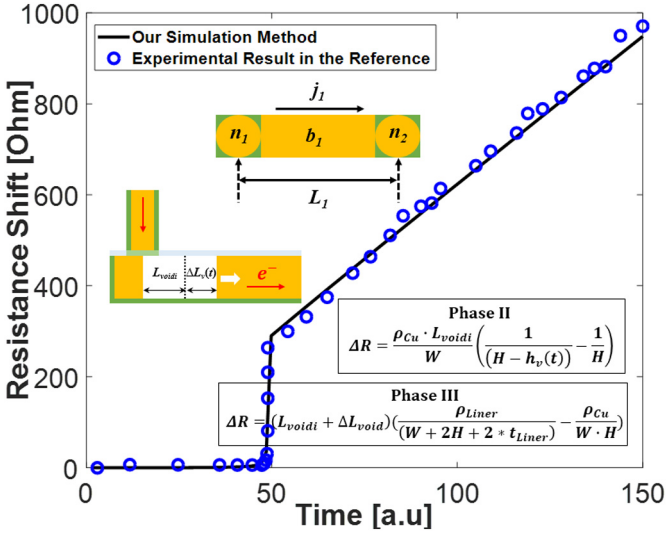


Fig. 2. Resistance trace of interconnect with $L_1 = 250um$, $j_1 = 2.0e10\ A/m^2$ [23].

the model enters phase II. The equations for resistance shift in phases II and III are listed in Fig. 2. The relation between the change of void size and the atomic flux is $\Delta L_{void} = J_a \cdot \Delta t$.

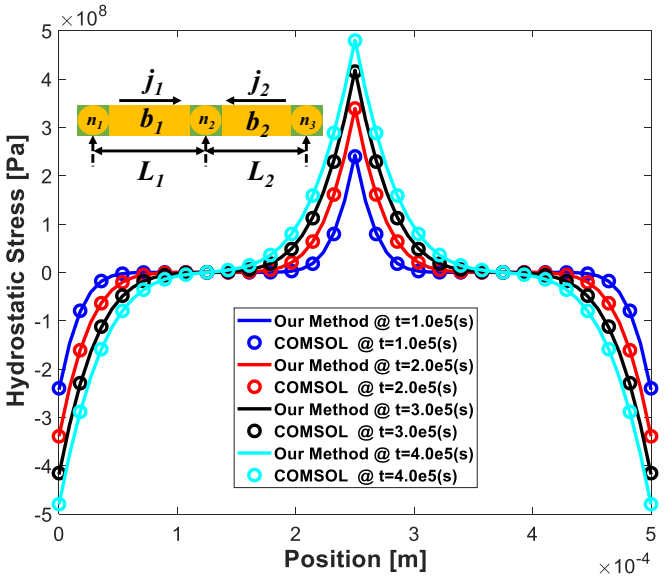
Since there isn't an experimental example available for validating hydrostatic stress and resistance evolution simultaneously, the verification of the EM model consists of a comparison with COMSOL for stress and a comparison with experimental data in the literature [23] for the resistance change.

The dimensions and injected current density of the sample structure studied for stress evolution can vary significantly. We have chosen some examples to validate the effectiveness and correctness of our computational methodology with what we believe to be reasonable values for interconnect size and the current density injected. Two examples are shown in Figs. 2 and 3. For these examples, our EM model for the stress distribution and resistance evolution matches well with COMOSL and experimental data in the literature. The parameters fitted during the comparison are applied in the computation of EM degradation in the following sections. The current density applied in the example in Fig. 3 is relatively large, but the results match well with COMSOL for smaller or larger values of current.

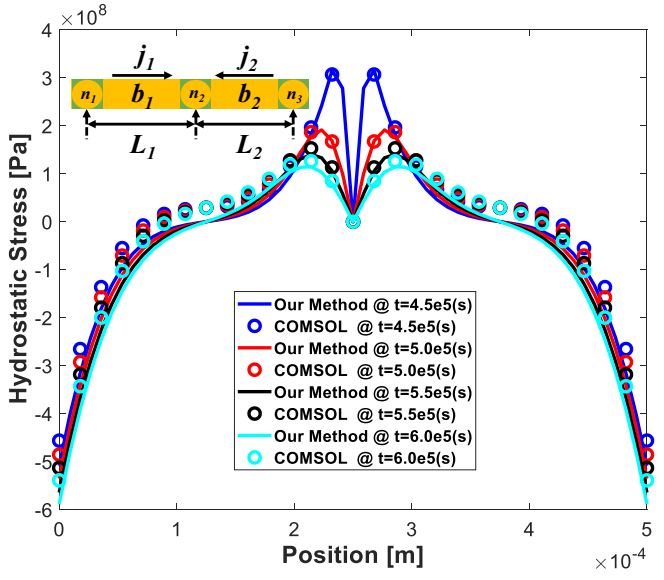
2.2. FinFET SRAM cell array

A 1024*32 cell array is studied in this paper. Overall the EM induced resistance shift is compared to the initial resistance to measure the degradation. The failure standard is set as a 10% rise over the initial resistance of a bit/bit-bar line [24]. The interconnect segment array is shown in Fig. 4(a), where the interconnects and cells have a periodic pattern. The cell configuration is adopted from ITRS-2013 for the 6-T FinFET SRAM [25]. The unit capacitance and resistance are obtained with Synopsys Raphael [26]. The cell length and width are adopted as $3P_{M1}$ and $5P_{M1}$, respectively. Calculations of hydrostatic stress and the resistance evolution in Section 4 are based on the structure shown in Fig. 4.

Fig. 5 shows the currents related to the EM calculation during SRAM operations of read0 (r0), read1 (r1), write0 (w0), and write1 (w1) for each cell. Both **read** and **write** include two steps that decide the overall current flowing through the interconnect segments. In the first step, the voltage of BL/BLB is adjusted to the corresponding value. In the second step, data is read from or written to the cells. Since the two steps are executed in order, the currents generated during precharge ($I_{pre\_r0/1}$) and read ($I_{r0/1}$) can be obtained separately, and are similar for $I_{drive1/2\_w0/1}$ and $I_{w0/1}$. I_{from_upper} and I_{to_lower} in Fig. 5(a) are marked for an



(a)



(b)

Fig. 3. The evolution of the hydrostatic stress distribution within the test structure (a) in phase I, and (b) after phase I. In this case, $L_1 = L_2 = 250\ \mu m$, $j_1 = j_2 = 2.0e10 A/m^2$, $\sigma_{ini} = 0$, and the threshold stress is chosen as $\sigma_{th} = 500\ MPa$.

explicit view of the currents (during the precharge for r0), shown in Fig. 6(b) and (d). To obtain the current flowing in each segment, the ratios corresponding to the cell and segment position, and the activity distribution of the cell array, such as the duty cycle and the probabilities that bit/bit-bar lines hold different voltage values, are applied for the current calculation.

3. Extraction of current and activity

First, the currents during the operations of r0, r1, w0, and w1 are extracted under various circuit configurations (with different values of gate length, temperature, and bitline capacitance). The relationship between circuit configuration and current value is fit with a regression

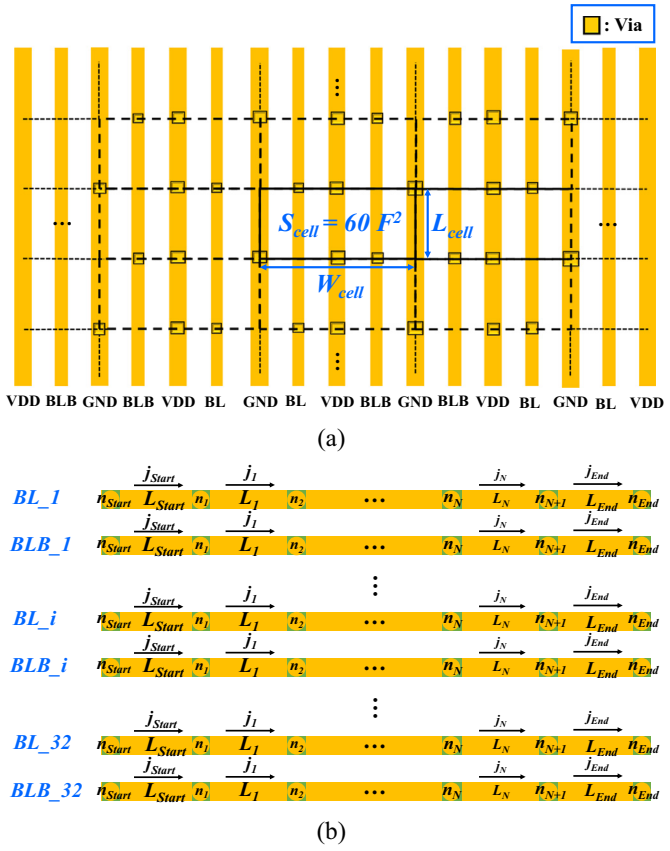


Fig. 4. (a) Interconnect segment array of an FinFET SRAM, with periodic cells shown, and (b) 32 pairs of interconnect segment arrays used for the calculation (32 columns of *BL/BLB*), where L_{Start} and L_{End} represent the interconnect lengths from the array to the precharge and write drivers, respectively.

algorithm to accelerate the simulation and for further optimization. Second, the operating activity of the cell array is emulated under various statistical workloads. Then the extracted current and activity are combined to obtain the current density flowing through each segment of each BL/BLB.

3.1. Current extraction

Current extraction is performed for each operation. Fig. 6(a) and (b) show the full circuit schematic and representative waveforms of current from upper cells to lower cells and from Precharge during r0. Circuit simulation is implemented with the Predictive Technology Model (PTM) for the 14 nm technology node [27].

For the 1024*32 cell array, the circuit in Fig. 6(a) has large number of resistors and capacitors. Simplification of the circuit facilitates the simulation flow. Considering the operating frequency of the SRAM and the capacitance/resistance range, the circuit is simplified to the one in Fig. 6(b). The resistances and capacitances in red circles are calculated as a function of cell position. For example, if the top cell has a ratio of 0, and the bottom cell has a ratio of 1, then the resistance/capacitance are equal to the cell ratio multiplied by the line resistance/capacitance. In the same circle, resistance and capacitance are shared by two cells with the same value.

Because of process variations, circuits have performance metric distributions. Validation of the circuit simplification should also consider process variations. As shown in Fig. 6(d), the sampled relative error of r0 currents (in Fig. 6(b)) due to simplification are obtained by Monte Carlo (MC) simulations with a sample size of 10 k. The process variations, including inter-die gate length and intra-die threshold voltage, are modeled as Gaussian distributions with standard deviations equal to 5% of their nominal value. The average relative error is −2.2021%, 0.2918%, 1.2000%, for the r0 currents in Fig. 6(b). The average relative error for currents during r1, w0, and w1 is also under 4%. Since the overall relative error is acceptable, the simplified circuit schematic is adopted for current extraction.

The currents during each operation are also a function of temperature, the cell's vertical position, and the unit segment's capacitance and resistance when the time gap (the time gap represents the time duration with current flows) for each current is adopted for its average value. When the effect of the EM resistance shift on currents is negligible, it's not included here. Since the current flowing through each interconnect segment is needed for calculating hydrostatic stress, the current values in different configurations (such as different vertical positions) are required. For simulations with process variations, the currents during the first step (charge or discharge on bitlines) have exact values ($I_{pre\_r0/1}$ & $I_{drive1/2\_w0/1}$), while the currents (I_{r0}, I_{r1}, I_{w0}, and I_{w1}) during the operation's second step (charge or discharge on Q or QB) have distributions which are best fit with a Normal distribution.

Four regression models for the four operations are built based on Multivariate Adaptive Regression Splines (MARS) to accelerate the simulation while providing the currents for each specific configuration of each cell in the array [28]. The training data sample size was 1 k, which provided good accuracy. Fig. 7 shows the models which were regressed and the final relative error distribution for representative currents. The average relative error is under 1% for most currents, except for one

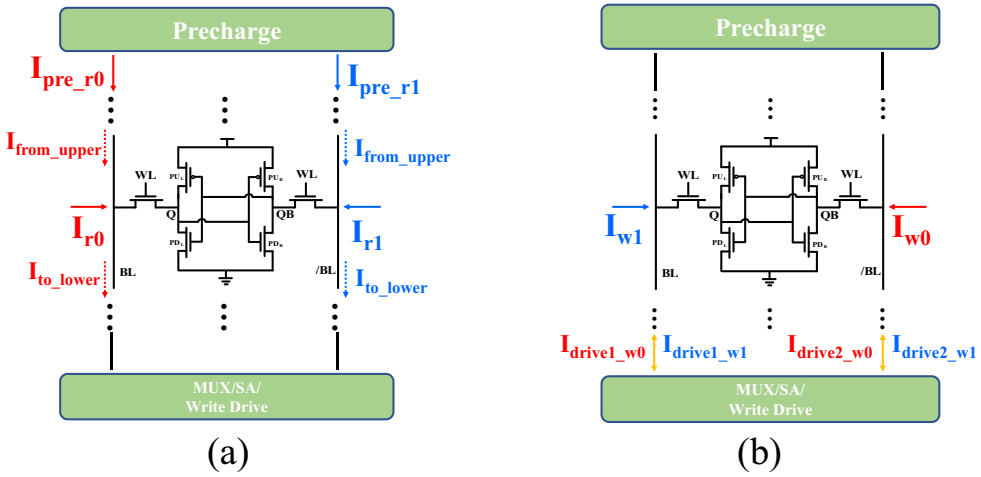


Fig. 5. Currents related to the EM calculation during (a) r0 and r1, and during (b) w0 and w1.

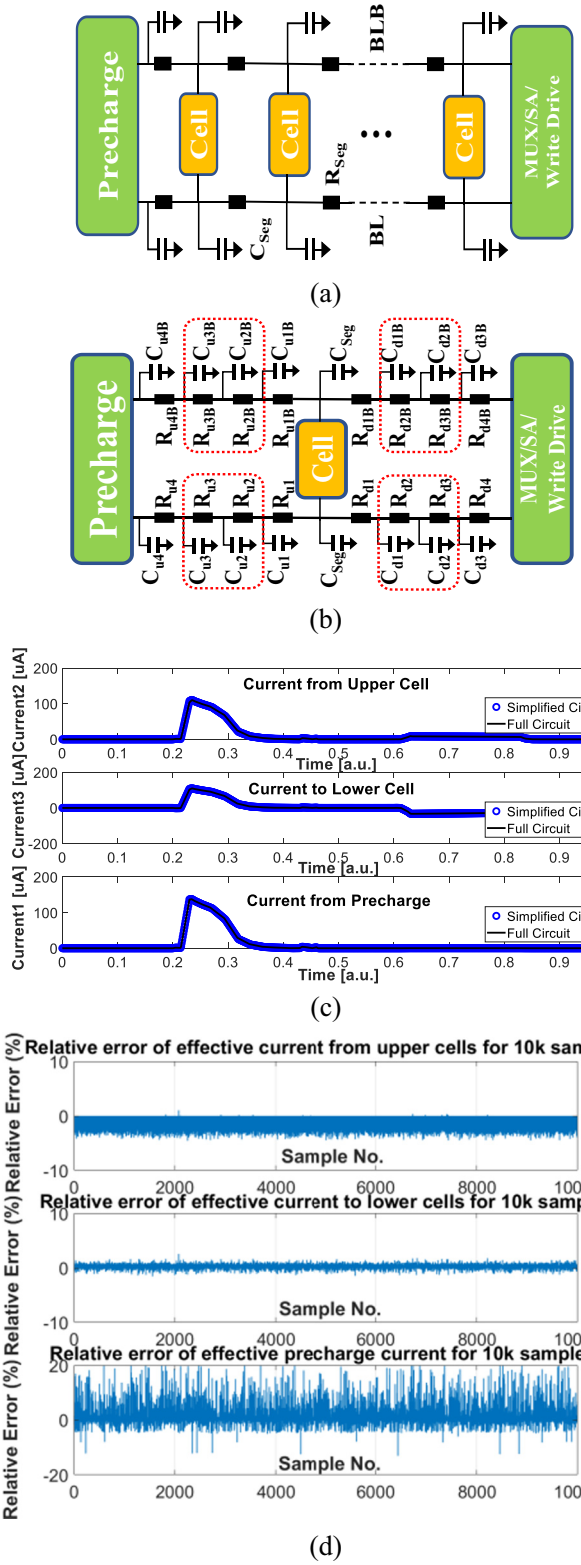


Fig. 6. Representative (a) circuit schematic of one column of cells, (b) simplified circuit schematic, (c) current flowing from upper cell, current flowing to lower cell, and current flowing from precharge for a sample cell during r0, and (d) relative error of current flowing from upper cell, current flowing to lower cell, and current flowing from precharge, simulated with the simplified circuit during the first step of r0, when compared to the currents simulated with full circuit schematic as shown in (a).

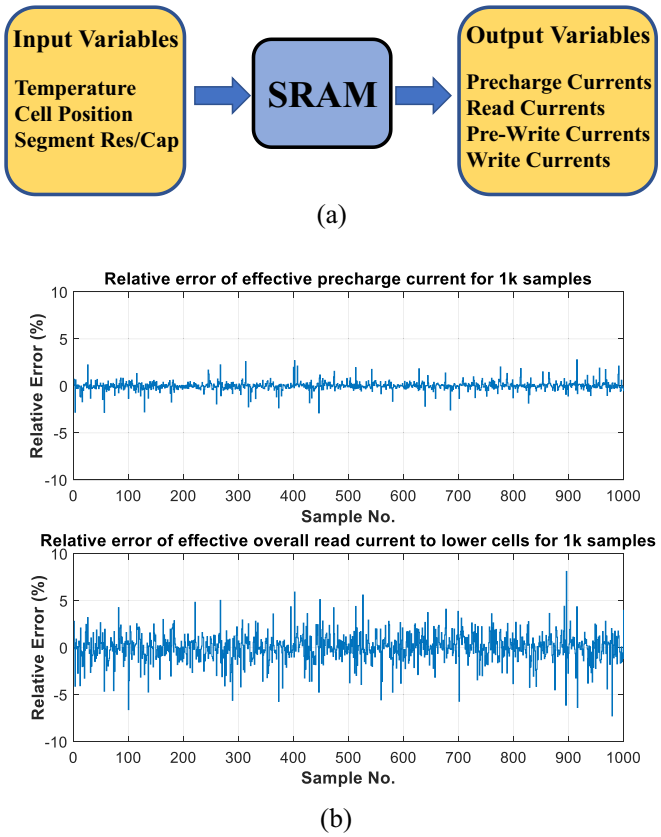


Fig. 7. (a) The model to be regressed, and (b) the relative error distribution for currents during r0.

with 6% error during **write** operations. Then the fitted MARS models and preset time gaps (effective duration with current flows) are applied together with the activity distributions in part 3.2 for EM simulation.

3.2. Cell array operation activity

In this part, the activity of the SRAM cell array is emulated with random read, write and idle operations. The overall simulation flow is shown in Fig. 8. The input is data written to the cell array together with the relative number of each type of operation: **read** (60%), **write** (20%), or **idle** (20%). The SRAM operating frequency is set as 1GHz. A delay of 10 cycles is assumed for each write operation. For one cell, its duty cycle is the probability that it stores state '1'. The input data written to the cell array is modeled as a Gaussian distribution with different mean duty cycle values (such as 10%, 20%, and 30%) [29]. In other words, analysis of various applications indicates that the duty cycle distribution within a full SRAM array can be modeled as a Gaussian distribution, and the mean value is typically less than 50%. The input address for the simulator is randomly assigned for the 1024 rows with equal probability.

Figs. 9–11 show example duty cycle distributions over the cell array, probability that BLs are 0, and the probability of w0 for each column if

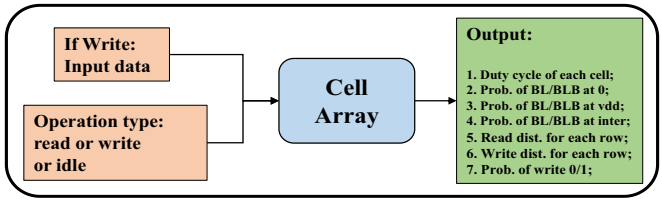


Fig. 8. Simulation flow for activity extraction.

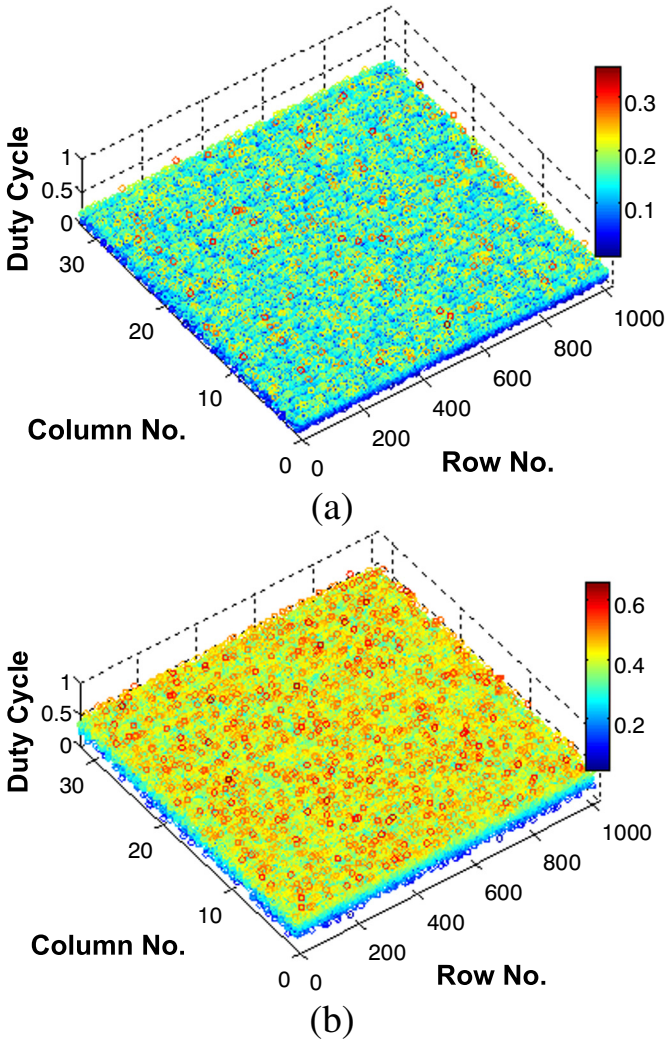


Fig. 9. Extracted duty cycle distribution with different input data (mean of distributions at (a) 10% and (b) 30%).

the operation is **write**, when the input data has a Gaussian distribution with different mean duty cycles. These parameters are extracted to calculate the current density in part C.

Obviously, the cell duty cycle distribution is decided by the input data. The probability that BLs are 0 decreases with the increase of the input data's mean duty cycle. The probability of w0 for each column also decreases with the increase of the input data's mean duty cycle. The effect of the percentage of read, write and idle out of the total number of operations is also emulated to check how these parameters affect EM degradation in Section 4.

3.3. Current density distribution through BL/BLBs

To obtain the current density through each BL/BLB segment, the current and activity extracted in Parts A and B are calculated together. Firstly, considering the high operating frequency of the SRAM, the equivalent current density under a bipolar pulse is equal to [30]

$$j = (j_+ t_+ + j_- t_-)/T_0 \quad (6)$$

where j_+ and j_- are the current density in the positive and negative direction, and t_+ and t_- are their corresponding time gaps (effective duration with current flows). T_0 is a time step selected in advance.

Secondly, the equivalent current density through each segment of BL/BLB is calculated with the sum of all possible cases when there is current flowing through the segments. The current direction is handled carefully. The probability of BL/BLB at different voltage values and the probability of w0 for each column are included. Fig. 12 shows an example of the current density over BL/BLB in the first column, with different input data distributions. Since the probability of BL/BLB at different voltage values varies inconsistently, the current density on the BL gets higher for input data probabilities ranging from 10% to 30%, while the current density on BLB gets lower.

4. Algorithm details and simulation results

This section discusses how activity and workload affect EM degradation, which sheds light on the effective evaluation of FinFET SRAM degradation due to EM.

4.1. Algorithm details

Monte Carlo (MC) simulation is performed according to the description of Algorithm 1. A sample size of 1000 32kB FinFET SRAM cell arrays was considered. The overall MC simulation takes 640 min when implemented with MATLAB on a dual-core 2.2GHz PC with 8GB memory. Since this is just a prototype, the speed can be improved significantly with C++ programming on an advanced Linux server. The time for training current models is less than 10 min. For each sample of a specific activity distribution, the resistance shift of each BL/BLB at each time point is calculated. The lifetime of each BL/BLB line is obtained which is the time when the resistance shift exceeds the predefined threshold. The threshold is chosen as a 10% rise of the overall interconnect resistance (150 Ω in our case), which denotes an obvious increase of delay. Then the lifetime distribution of the circuit is the statistical combination of all BL/BLB's. After MC simulation, the

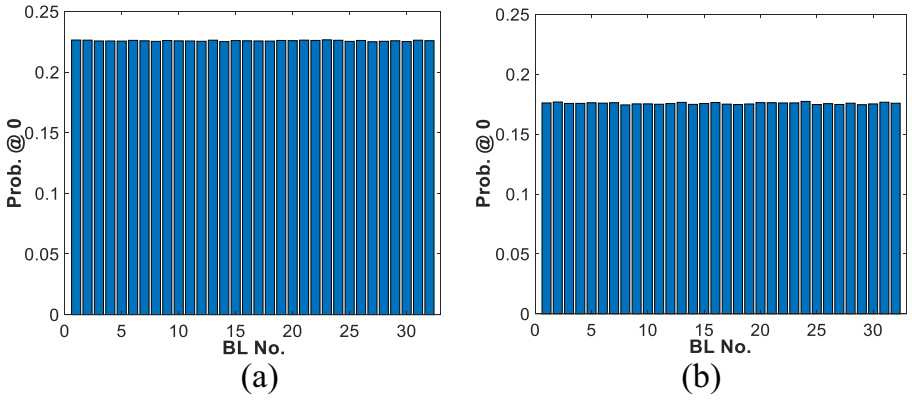


Fig. 10. Extracted probability that BLs are 0, with different input data (mean of distributions at (a) 10% and (b) 30%).

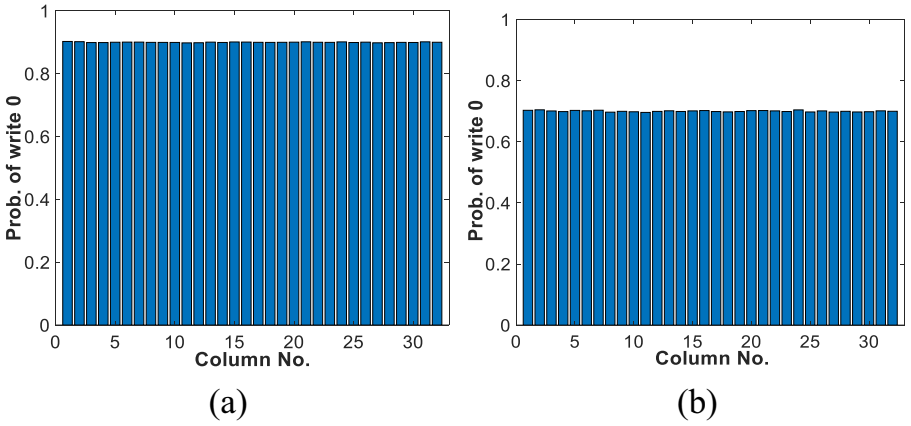


Fig. 11. Extracted probability of w0 for each column if the operation is **write**, with different input data (mean of distributions at (a) 10% and (b) 30%).

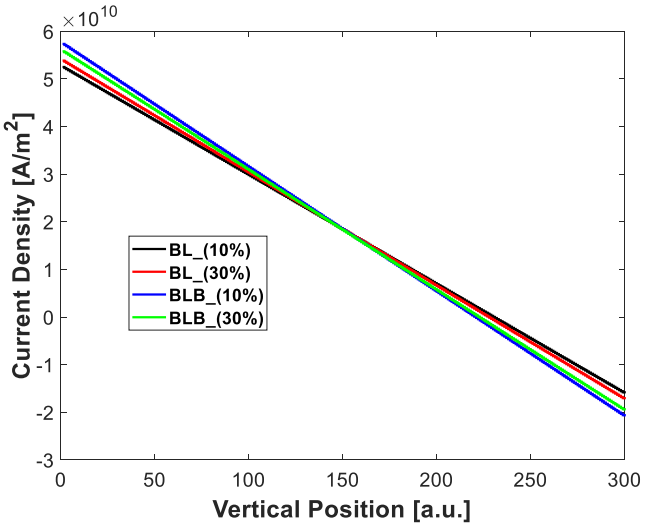


Fig. 12. An example of current density over BL/BLB in the first column, with different input data (mean signal probabilities of 10%, and 30%).

lifetime distribution related to current activity is obtained. Here, the temperature is assumed to be 321 K, which comes from thermal simulation for a FinFET-based microprocessor.

Algorithm 1. EM reliability simulation.

Input: Fitted thermal model $\mathcal{T}$, fitted current models (I_{r0}, I_{r1}, I_{w0}, I_{w1}), activity A, MC simulation sample size N_{MC}, overall simulation time step N_t.

Output: Stress distribution, resistance shift distribution, lifetime distribution.

function INITIALIZATION ($\mathcal{T}$, I_{r0}, I_{r1}, I_{w0}, I_{w1}, A)
  Return [T]: temperature matrix; [S]: hydrostatic stress matrix;
  [j]: current density distribution; [P]: Basic Parameter set;
end function

procedure EM_Relia
  $i = 0$
  while $i<N_{MC}$ **do**
    INITIALIZATION ()
    $k = 0$
    while $k<N_t$ **do**
      Update stress distribution & resistance shift
    $k = k+1$
  Get lifetime of current case
  $i = i+1$
end procedure

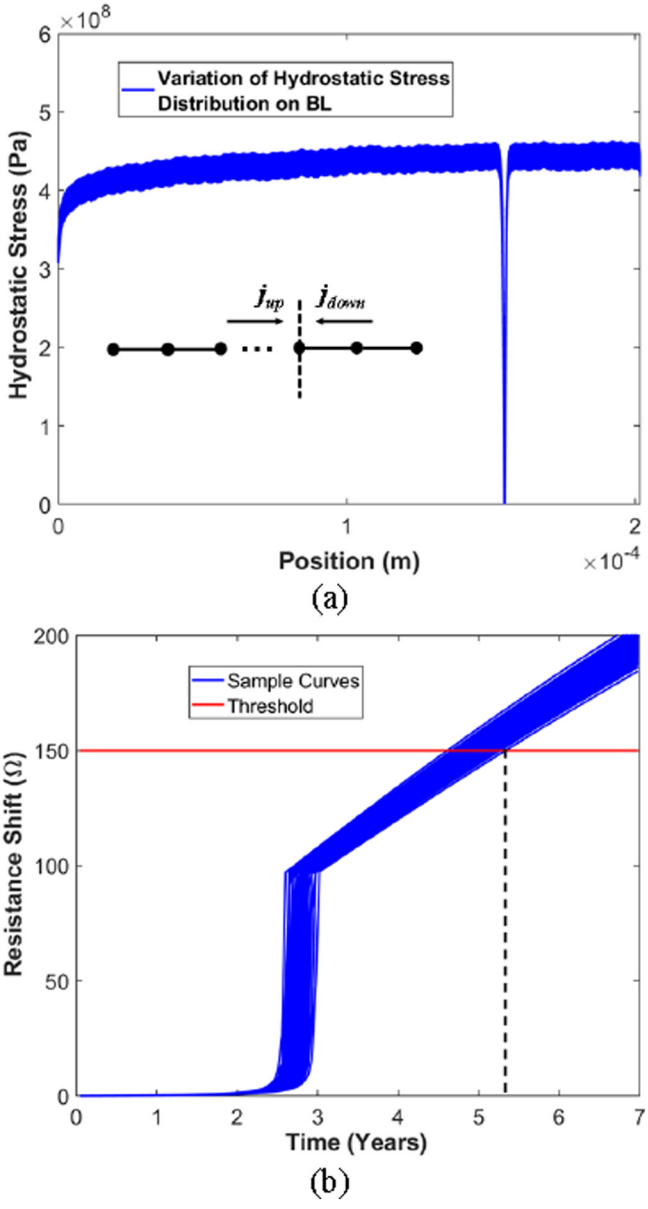


Fig. 13. (a) Variation of the hydrostatic stress distribution on a sample BL at 3.5 years (Left: Precharge side, Right: write drive side), and (b) variation of the overall resistance shift of a sample BL. The input data distribution has a mean duty cycle of 10%.

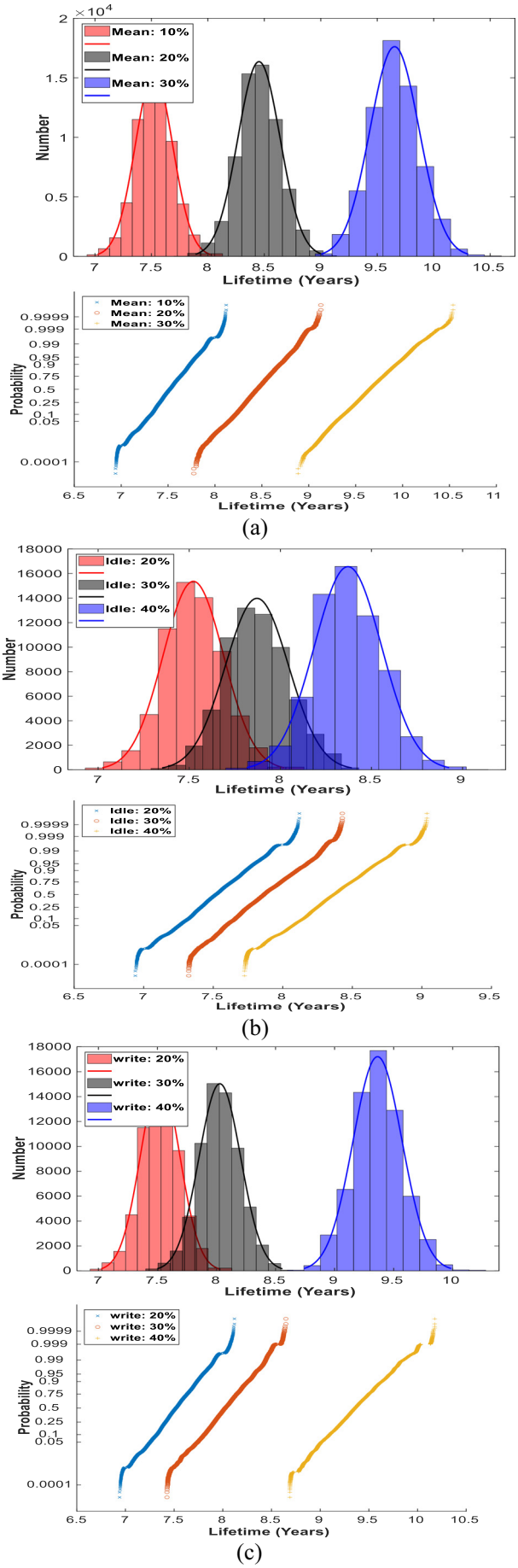


Fig. 14. Histogram and cumulative distribution plots of (a) effect of input data distribution's mean probability on the lifetime distribution, with read (60%), write (20%), and idle (20%) percentages unchanged, (b) effect of the idle percentage on the lifetime distribution, with the relative percentage ratio between read and write unchanged, and (c) effect of the write percentage on the lifetime distribution, with the idle (20%) percentage unchanged.

4.2. Simulation results

Fig. 13(a) shows the variation of the hydrostatic stress distribution on a sampled BL at 3.5 years, where the input data distribution has a mean duty cycle of 10%. It is observed that the void occurs at the position close to the write driver. Considering the current distribution on the BL/BLB shown in Fig. 12, current flows from left to right on the left side, while it flows from right to left on the right side. Since the electrons flow in the opposite direction of current, it is reasonable that the void occurs in a position where the equivalent current is zero.

Fig. 13(b) shows the variation of the overall resistance shift of a sample BL under the same workload. Based on the resistance shift of all samples, the lifetime distribution is obtained as the time when the shift exceeds a threshold.

Fig. 14(a) shows that with the increase of the input data distribution's mean duty cycle, the FinFET SRAM cell array's lifetime due to EM increases. This is mainly because the probability that BLs are 0 gets lower with a higher mean duty cycle, as shown in Fig. 10. During each read operation, the BL/BLBs are pulled up to 1 in the first step. Therefore, when more BL/BLBs are 1, the BL/BLBs are less likely to be injected with precharge current. Hence, if the mean duty cycle is higher, less current flows through the BL/BLBs and the lifetime increases.

Fig. 14(b) shows that a higher idle percentage produces a better lifetime. Obviously, circuits with more idle time are less likely to be affected by EM.

Fig. 14(c) shows that with 20% idle time unchanged, higher write percentages help improve EM reliability, which means read is more important than write for EM degradation. Read is more important because it causes more effective current to flow in the interconnect segments.

5. Conclusion

A methodology is proposed to use cell array activity to evaluate the resistance degradation due to EM for a FinFET SRAM. This work shows that operating activity is important for a FinFET SRAM cell array's reliability due to EM. First, increasing the idle percentage brings about better reliability. Second, with the increase of the input data distribution's mean duty cycle (between 0% and 50%), the cell array's lifetime distribution gets better. Third, with the idle percentage unchanged, the read operation leads to worse EM degradation than write. This enables designers to check whether the EM reliability of a FinFET SRAM under certain workloads meets requirements when running real applications.

Based on the EM modeling for the SRAM cell array, we can extend our work to study EM reliability of the SRAM cache, which consists of many SRAM cell arrays. Then we can figure out how activity and cache configurations impact its performance and EM reliability. Finally, we can optimize the design of the cache, taking into account the trade-off between reliability/lifetime and performance (such as hit rate). The relevant conclusion will be unveiled in future work.

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Declaration of competing interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

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