Monolayer MoS_2 Steep-slope Transistors with Record-high Sub-60-mV/decade Current Density Using Dirac-source Electron Injection

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Abstract**—**Two-dimensional (2D) semiconductors such as MoS_2 are promising material candidates for next-generation energy-efficient nanoelectronics. For the first time, a 2D steep-slope field-effect transistor (FET) based on novel Dirac-source electron injection (DSEI) was demonstrated where monolayer graphene (Gr) source injects cold electrons to monolayer MoS_2 channel. As an innovative steep transistor concept, this atomic-thin 2D DSEI-FET shows the minimum subthreshold swing (SS) of 29 mV/decade and, more importantly, a record-high sub-60-mV/decade current density (over 1 μA/μm) compared to any state-of-the-art 2D or three-dimensional (3D) tunneling FETs (TFETs) or negative capacitance FETs (NCFETs).

I. Introduction

2D semiconductors such as MoS_2 have been extensively explored for energy-efficient nanoelectronics due to the natural quantum confinement in an atomically thin body [1, 2]. However, the SS in MoS_2-based conventional FETs still suffers from the "Boltzmann tyranny" limit (60 mV/decade at room temperature) which sets a bottleneck to continue minimizing the power dissipation [3, 4]. Various solutions in principle can achieve a sub-60-mV/decade SS, for example, by lowering the transport factor via a band-to-band Zener tunneling effect in MoS_2 TFETs [5, 6], or by reducing the body factor via a ferroelectric gate layer with negative differential capacitance in MoS_2 NCFETs [7-9]. Yet, neither of them has been successfully demonstrated with a sub-60-mV/decade current density higher than 1 μA/μm which is a key metric for logic transistors to benefit from the steep slope [10, 11]. In this work, for the first time, we demonstrated a 2D monolayer MoS_2 steep-slope DSEI-FET. An excellent sub-60-mV/decade SS (across for three decades with the minimum SS of 29 mV/decade) and a record-high steep-slope current density (~4 μA/μm) were achieved, compared to any 2D- or 3D-channel-based TFETs and NCFETs. This is due to the "cold" electrons in Gr-enabled DSEI which possesses a more localized carrier density distribution and a shorter thermal tail. Our work revealed the great potential of 2D DSEI-FET as a new type of emerging steep-slope device concept for beyond-CMOS technology.

II. Theoretical Investigation

Gr-enabled 2D DSEI. Conventional 3D or 2D FETs (i.e., Si or monolayer MoS_2 FETs) operate on the basis of thermionic emission of charge carriers flowing from a normal source over a potential barrier (ϕ_b) within channel region, as shown in Fig. 1(a) and (b). Owing to the energy (E) dependence of the density of states (DOS), i.e., $DOS_{3D} \sim (E–E_C)^{1/2}$ for 3D materials and $DOS_{2D} \sim (E–E_C)^0$ for 2D materials, the electron density (n) in these normal sources follows the Fermi-Dirac distribution, and shows a sub-exponential decay (i.e., $n_{3D} \sim (E–E_C)^{1/2}\exp[(E_F–E)/k_BT])$ for 3D materials and an exponential decay (i.e., $n_{2D} \sim \exp[(E_F–E)/k_BT]$) for 2D materials, which both present a relatively long Boltzmann tail [12, 13]. Here E_F, E_C, k_B, and T are the Fermi energy, minimum conduction band edge, Boltzmann constant, and temperature, respectively. As a comparison, the monolayer Gr has a linear energy dispersion near the Dirac point. Because the DOS is a linear function of E (i.e., $DOS_{Gr} \sim E_{Dirac}–E$), n in Gr shows a super-exponential decay (i.e., $n_{Gr} \sim (E_{Dirac}–E)\exp[(E_F–E)/k_BT]$) and a short thermal tail which is terminated at E_{Dirac}, as shown in Fig. 1(c), where E_{Dirac} is the Dirac point energy. A quantitative comparison of the normalized carrier density, i.e., $n(E)/n(E_F)$ between MoS_2 and p-type doped Gr is obtained, which indicates a more localized distribution of n near E_F in Gr, as shown in Fig. 1(d). Considering a gate-controlled ϕ_b is created at the Gr/MoS_2 heterobilayer interface, the Gr-enabled novel DSEI can be cut off more effectively by the gate, and thus the device can switch faster by breaking the SS limit.

2D steep-slope MoS_2 DSEI-FET. The device structure and operation principle of a 2D n-type MoS_2 DSEI-FET is illustrated in Fig. 2(a), where the electron transport path is divided into three regions: Gr source region (p-type doped by applying a constant back-gate voltage (V_{BG})), Gr/MoS_2 heterobilayer region, and MoS_2 channel region. At the off state, a top-gate voltage (V_{TG}) creates a large ϕ_b at the Gr/MoS_2 interface to prevent the electron injection. As V_{TG} increases, the device operates in the subthreshold regime, and the current increases due to the thermionic injection of the hot electrons over the reduced ϕ_b. When an energy window, defined as E_{Dirac}–ϕ_b, is opened for the DSEI, the cold Dirac electrons are allowed to transport from Gr to MoS_2, which enables the sub-60-mV/decade switching until the device operates at the on state. Based on the Landauer-Büttiker formula at the ballistic transport limit [12, 13], the SS can be plotted as a function of ϕ_b–E_{Dirac} for a variety of the body factor (C, ranging from 0 to 1), as shown in Fig. 2(b). The DSEI energy window can be

found when ϕ_b–E_{Dirac} < 0, which shows the sub-60-mV/decade SS even at C = 0.2. By estimating the Fermi level shift (or doping level, E_F–E_{Dirac}) of Gr [14], the SS as a function of V_{TG}–V_{Dirac} can be obtained, as shown in Fig. 2(c), where V_{Dirac} is the Dirac point voltage. As V_{TG} increases, both the normal-source electron injection with a near-60-mV/decade SS and the novel DSEI with a sub-60-mV/decade SS are predicted in succession as the 2D MoS_2 DSEI-FET turns on, giving rise to a "double-minima" feature of the SS in the subthreshold regime.

III. Experimental Demonstration

Device fabrication. A 2D MoS_2 DSEI-FET was fabricated based on a Gr/MoS_2 heterobilayer, as shown in Fig. 3. Both the monolayer Gr and monolayer MoS_2 were confirmed by Raman spectroscopy and atomic force microscopy (AFM). Ti/Au (10 nm/90 nm) electrodes were patterned and deposited for the configurations of the back-gate normal-source Gr FET, MoS_2 FET, Gr/MoS_2 FET, and the top-gate Dirac-source MoS_2 DSEI-FET, followed by atomic layer deposition (ALD) of an Al_2O_3 layer (30 nm). After opening a top gating window by wet etching, a room-temperature ionic liquid (DEME-TFSI) was applied to provide a localized high-efficiency electrostatic gating through the electric double layer (EDL) effect [15].

Device characterization. Drain current density (J_D) was measured as a function of drain voltage (V_D), V_{BG}, and V_{TG} for various FETs. First, Ohmic contacts were confirmed through linear *IV* relationships in the J_D-V_D output characteristics of the back-gate FETs, as shown in Fig. 4(a). Their J_D-V_{BG} transfer characteristics were compared in Fig. (b), where the SS was still constrained by the thermionic limit due to the dominance of the normal-source carrier injection. Then, the room-temperature J_D-V_{TG} transfer characteristics of the top-gate MoS_2 DSEI-FET were measured at different V_{BG} levels, which possess an excellent on/off ratio of ~10^7, as shown in Fig. 4(c). Especially, a DSEI-induced sub-60-mV/decade switching was obtained at V_{BG} = –80 V (i.e., the Gr source was doped into p-type), and the minimum SS were obtained as 49 mV/decade in a forward sweep and 29 mV/decade in a backward sweep, as shown in Fig. 4(d). By extracting the SS as a function of J_D, the sub-60-mV/decade switching sustains for about one decade in the forward sweep and about three decades in the backward sweep, as shown in Fig. 4(e) and (f). The extracted SS as a function of V_{TG} was also consistent with the theoretical anticipation (see Fig. 2(c)). Due to the novel DSEI-induced steep slope, the trans-conductance ($g_m = \partial J_D/\partial V_{TG}$) was significantly improved, and its efficiency (g_m/J_D) shows the maximum over 400 V^{-1} which is about one order of the magnitude higher than the limit (38.5 V^{-1}) in the conventional transistors [16], as shown in Fig. 4(g-i). As V_{BG} increases, the conventional normal-source electron injection becomes dominant, and the minimum SS rises and stabilizes at ~210 mV/decade in the forward sweep and ~90 mV/decade in the backward sweep, as shown in Fig. 4(j). Both the sub-60-mV/decade SS and the double-minima feature were also observed in other MoS_2 DSEI-FETs, suggesting a good reproducibility, as shown in Fig. 4(k) and (l). With the increasing T, both the on-state J_D ($J_{D,on}$, obtained at V_{TG} = 3.5 V) and the DSEI-dominated J_D ($J_{D,DSEI}$, obtained at the minimum SS) show a clear increase, being consistent with the thermionic carrier transport behavior, as shown in Fig. 5.

Performance benchmarking. The 2D MoS_2 DSEI-FET in this work was benchmarked with other state-of-the-art beyond-CMOS technologies. Compared to the 14 nm Si-based FinFET CMOS technology [17], the 2D MoS_2 DSEI-FET shows the near-60-mV/decade and sub-60-mV/decade SS in succession as the device switches from off to on state, owing to the injection of the normal-source hot electrons and Dirac-source cold electrons, respectively, as shown in Fig. 6(a). The sub-60-mV/decade SS as a function of J_D was compared with other steep-slope transistors, including TFETs [18-26], NCFETs [8, 27, 28], and one-dimensional (1D) DSEI-FETs [12] based on a variety of channel materials, as shown in Fig. 6(b). The 2D MoS_2 DSEI-FET possesses the ultimately thin channel (~0.65 nm for monolayer MoS_2) and especially a record-high steep-slope current density (~4 μA/μm) compared to any TFET and NCFET technologies based on 2D or 3D channel materials so far. This is due to the novel DSEI mechanism which sustains during the switching until the end of the subthreshold regime.

IV. Conclusion

In this work, we demonstrated the first 2D atomic-thin steep-slope MoS_2 DSEI-FET which showed the outstanding sub-60-mV/decade SS, excellent on/off ratio, and record-high steep-slope current density compared to any 2D- or 3D-channel-based TFETs or NCFETs. With the novel DSEI mechanism, the 2D DSEI-FET has been proved as a new type of emerging steep-slope transistor concept for beyond-CMOS technology.

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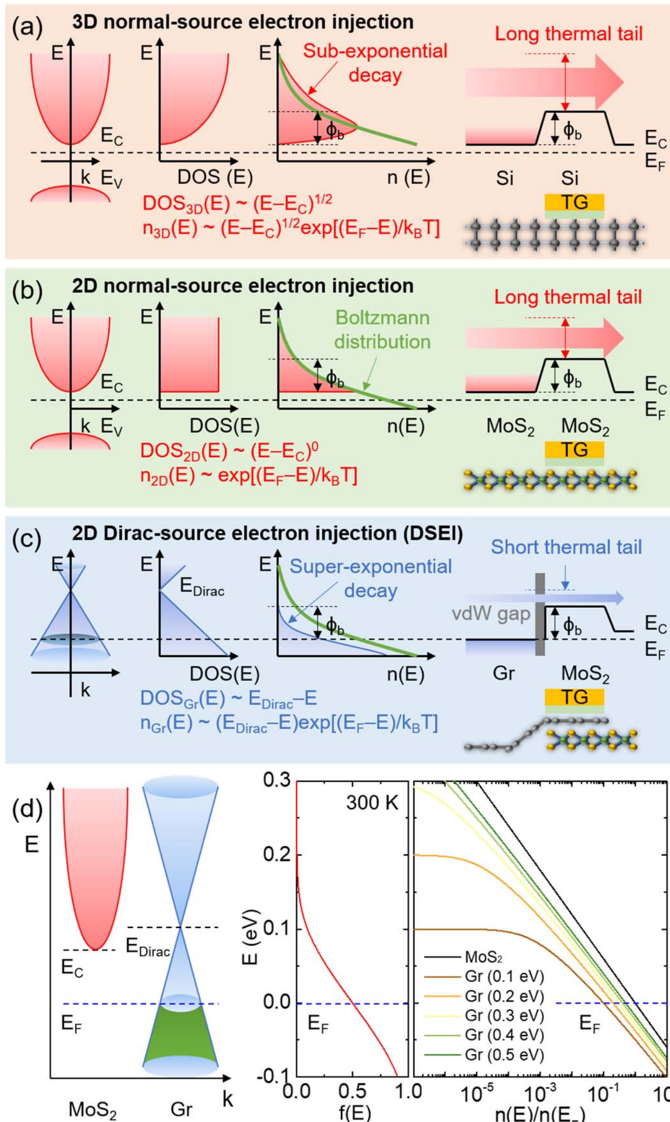

Fig. 1. (a, b, c) Comparison of energy band diagrams of 3D and 2D normal-source electron injection in conventional Si and MoS_2 FETs, and 2D DSEI in a Gr/MoS_2 heterobilayer, including *E-k*, *E*-DOS, and *E-n* diagrams. The Gr-enabled DSEI has a short thermal tail terminated at E_{Dirac}, and can be cut off more efficiently by a gate-controlled ϕ_b at the van der Waals (vdW) interface. (d) Calculated *E* as a function of the Fermi-Dirac distribution ($f(E)$) and $n(E)/n(E_F)$. Here $E_F = 0$ eV for both MoS_2 and Gr. Gr is p-type doped and E_{Dirac} ranges from 0.1 to 0.5 eV.

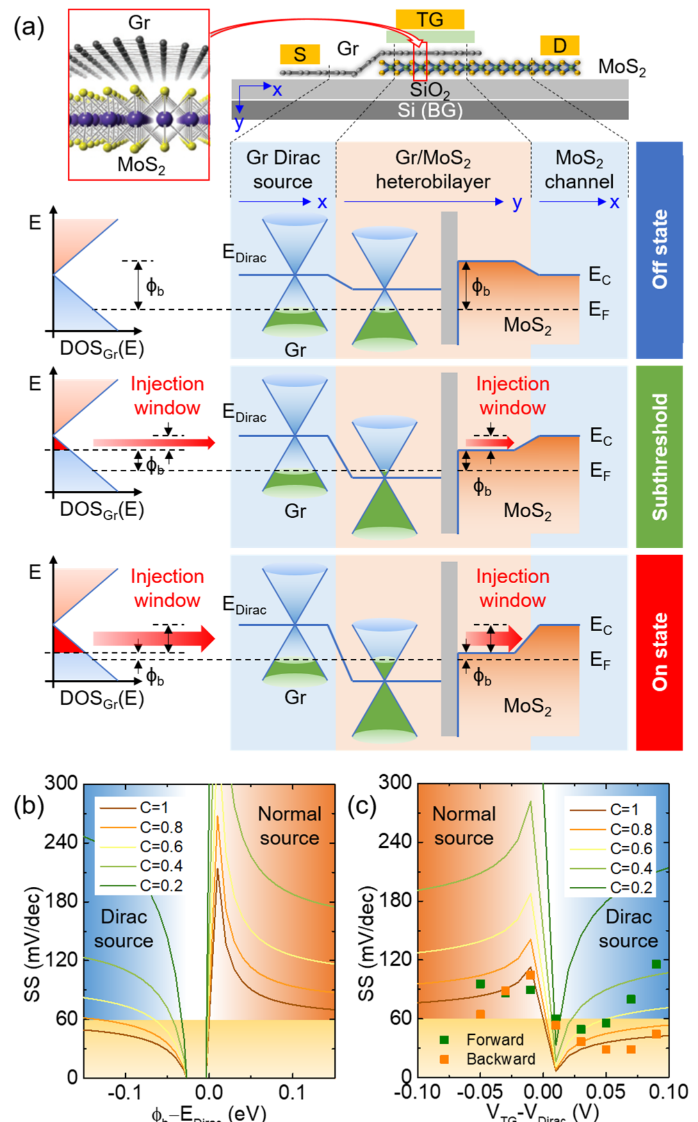

Fig. 2. (a) Device structure of a 2D MoS_2 DSEI-FET and its energy band diagrams along the electron transport path at the off state, subthreshold, and on state. The red arrows indicate the DSEI and its energy window. (b, c) Calculated SS (lines) as a function of ϕ_b–E_{Dirac} and V_{TG}–V_{Dirac} at different *C* levels, compared with the experimental results (symbols). The dominant regimes of normal-source and Dirac-source electron injection are illustrated by orange and blue backgrounds. A top-gate capacitance of 1 μF/cm^2 is used for calculation.

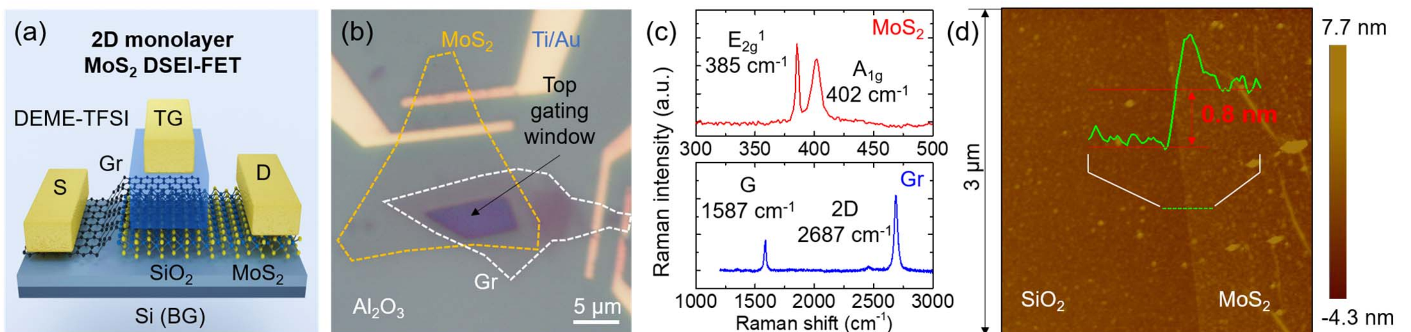

Fig. 3. (a) Schematic illustration of a 2D MoS_2 DSEI-FET, where S, D, TG, and BG denote the source, drain, top gate, and back gate, respectively. (b) Optical microscopy image of the device after Al_2O_3 deposition. A top gating window is opened within the Gr/MoS_2 overlapping area for a localized gating effect through an ionic liquid. (c) Raman spectra for the monolayer MoS_2 and monolayer Gr. (d) AFM characterization for the monolayer MoS_2.

Fig. 4. (a, b) J_D-V_D output characteristics and J_D-V_{BG} transfer characteristics of the back-gate Gr FET, MoS_2 FET, and Gr/MoS_2 FET. J_{BG} is the back-gate leakage current density. (c) J_D-V_{TG} transfer characteristics of the top-gate MoS_2 DSEI-FET under various V_{BG}. J_{TG} is the top-gate leakage current density. Black and red arrows indicate the forward and backward sweeps, respectively. (d) DSEI-induced sub-60-mV/decade switching at V_{BG} = –80 V in the forward and backward sweeps. Blue line is the 60-mV/decade thermionic limit. (e, f) Extracted SS as a function of J_D in the forward and backward sweeps under various V_{BG} levels. Dash lines as guides for the eye indicate the double-minima feature of the SS at V_{BG} = –80 V. (g-i) Comparison of g_m and g_m/J_D among the back-gate Gr FET, MoS_2 FET, Gr/MoS_2 FET, and top-gate MoS_2 DSEI-FET. (j) The minimum SS as a function of V_{BG} in the forward and backward sweeps with lines as guides for the eye. (k, l) Reproducibility proven by multiple MoS_2 DSEI-FETs. The sub-60-mV/decade SS and the double-minima feature are illustrated with lines as guides for the eye.

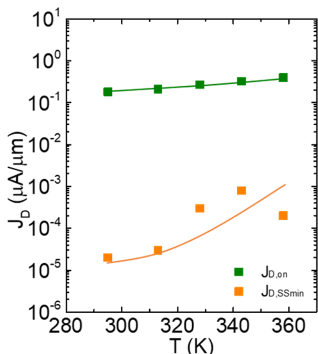

Fig. 5. Extracted $J_{D,on}$ and $J_{D,SSmin}$ as a function of T with lines as guides for the eye.

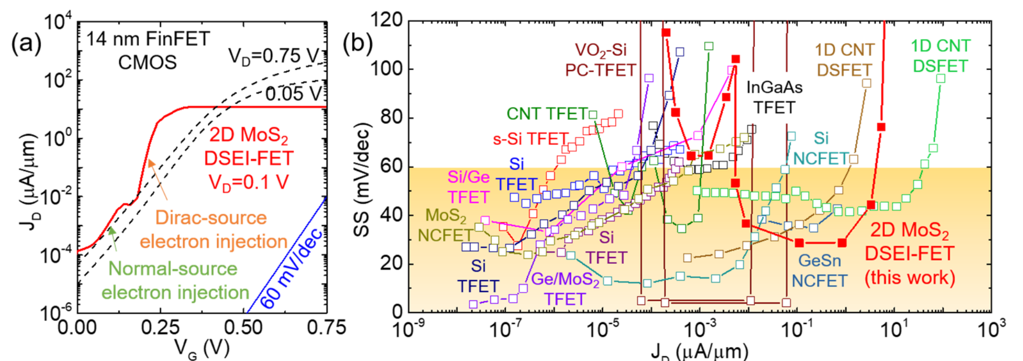

Fig. 6. Benchmarking of the 2D MoS_2 DSEI-FET with other state-of-the-art steep transistors, including (a) 14 nm FinFET CMOS technology, and (b) 2D or 3D TFETs, NCFETs, and 1D DSEI-FETs based on various channel materials. Our work possesses a record-high steep-slope current density (~4 μA/μm) compared to any 2D or 3D TFETs or NCFETs.