Demonstration of MOCVD-grown β-Ga_2O_3 MESFETs with Insulating Mg-Doped Buffer Layers

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Introduction: The high breakdown field (8 MV/cm) and availability of bulk substrates makes β-Ga_2O_3 promising for future high power switching applications. One of the main challenges for β-Ga_2O_3 based lateral device technology is the unintentional low-mobility channel at the substrate/epitaxial layer interface, which is due to Si impurities present on the substrate surface. In this report intentional doping with Mg (deep acceptor) is shown to be very effective for compensation of the parallel channel, resulting in low subthreshold leakage in transistors. The dependence of leakage and trap-related dispersion characteristics on the distance between the Mg-doped layer and channel was investigated. Our results demonstrate that Mg-doping is an effective method to realize insulating low-dispersion buffers.

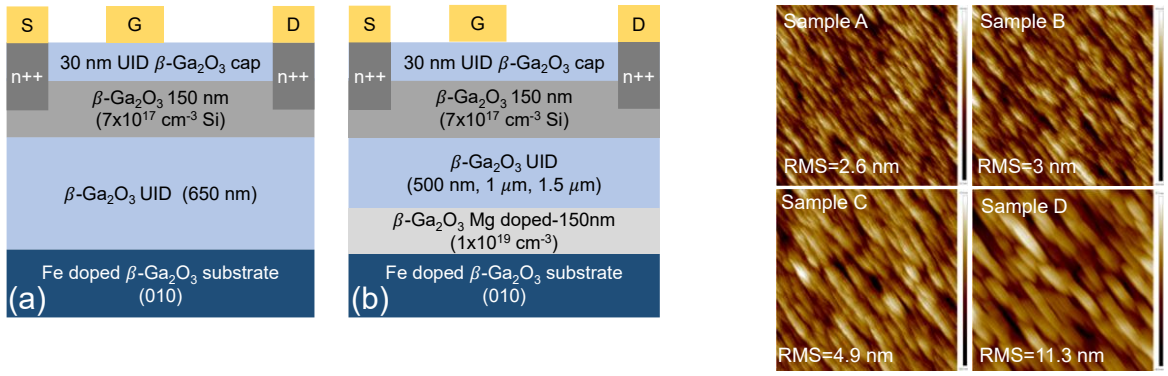
Epitaxial and device structure: The MOCVD grown epitaxial structures are shown in Fig.1 (a) and (b). The control sample (sample A) consists of a 500 nm unintentionally doped (UID) β-Ga_2O_3 layer grown on an Fe doped (010) substrate followed by the channel and cap layer. For Mg doped samples, 150 nm Mg doped ($1x10^{19}$ cm^{-3}) β-Ga_2O_3 buffer layer is grown on the substrate followed by UID β-Ga_2O_3 buffer layer, channel layer and cap layer. Three different thickness of UID β-Ga_2O_3 buffer layer (500 nm – sample B, 1 μm- sample C and 1.5 μm- sample D) were investigated. Mg doping is carried out using Cp_2Mg as the metal organic precursor[1]. The channel layer consists of 150 nm β-Ga_2O_3 with a targeted doping density of $7x10^{17}$ cm^{-3}. Source/drain regions were realized using Si ion implantation ($5x10^{19}$ cm^{-3}) followed by ohmic metallization using Ti/Au (30/ 100 nm). Device isolation was carried out using BCl_3/Ar based dry etching to form a 250 nm deep mesa structure. Schottky gates were defined and deposited using Ni/Au/Ni (30/50/20 nm) stack. Fig.2 shows the surface morphologies of all the 4 samples. Mg doping was found to result in increased surface roughness with the 1.5 μm UID buffer sample (sample D) showing an RMS of 11.3 nm.

Device characteristics: Hall mobility of 121 cm^2/V-s, 123 cm^2/V-s, 127 cm^2/V-s and charge density of $4.6x10^{12}$ cm^{-2}, $5.6x10^{12}$ cm^{-2} and $6.1x10^{12}$ cm^{-2} were obtained in samples B, C, D respectively, showing that the Mg diffusion does not significantly impact transport characteristics. Fig. 3 (c) shows the transfer charactersitics of samples A-D. All the Mg doped samples (B-D) showed good pinch off while sample A (no Mg buffer) did not. The charge profile (obtained from C-V) shown in Fig.3 (b) confirms the presence of a parallel channel in sample A, in contrast to a depleted charge profile in the buffer in all the Mg-doped samples (B,C,D). This shows that the inclusion of Mg-doped buffer layers effectively compensates the Si donors present at the substrate growth interface. The samples with thick buffer layers (samples C, D) showed relatively high gate leakage resulting in a low on off ratio of 10^4, while Sample B was found to show low gate leakage and high on/off ratio of 10^7. The subthreshold slope was found to increase from 195 mV/dec in sample B to 860 mV/dec in sample D (Fig. 3 (c)).

Low dispersion was observed under pulsed conditions (pulse width-5 μs, period-5 ms) for sample B, while samples C and D showed larger dispersion (Fig.4 (a)-(d)). The degradation in on-resistance is shown in Fig.4 (d) as a function of the applied drain quiescent point. The increased current collapse in samples C and D may suggest the formation of additional defect states in the thick UID buffer region grown on top of the Mg doped layer. Additonally, the surface morphology in samples C and D was relatively rough, which may also cause increased dispersion from surface states. Fig.5 (a) shows the the isolation leakage characteristics across a 2 μm spaced isolation structure, sample B is found to show the lowest isolation leakage. Since the chlorine based etch for the mesa layer results in significant damage [2], isolation leakage was found to be low for sample A, even though sample A does not show pinch off (Fig.3 (c)). Source leakage currents measured in transistor devices were compared for samples A-D (Fig.5 (b)). Sample A without Mg doping is found to show severe leakage even at low drain biases, while low leakage currents are obtained in the Mg-doped samples. Sample B (500 nm UID layer) showed over 2 orders of reduction in source leakage when compared to C and D, suggesting that the UID layer contributes significantly to subthreshold leakage.

In conclusion, Mg doping by MOCVD enabled insulating buffers with good transport and device characteristics, high on/off ratio and low dispersion under pulsed conditions. The control of buffer leakage is critical to enable lateral β-Ga_2O_3 transistors for power switching applications. This work was funded by AFOSR GAME MURI (Grant FA9550-18-1-0479, Program Manager Dr. Ali Sayir) and NSF (ECCS-1809682).

[1] Z. Feng et.al, *Appl. Phys. Lett.* ***117****, 222106 (2020). [2]* Joishi et.al, *IEEE TRANSACTIONS ON ELECTRON DEVICES, VOL. 67, NO. 11, NOVEMBER 2020*



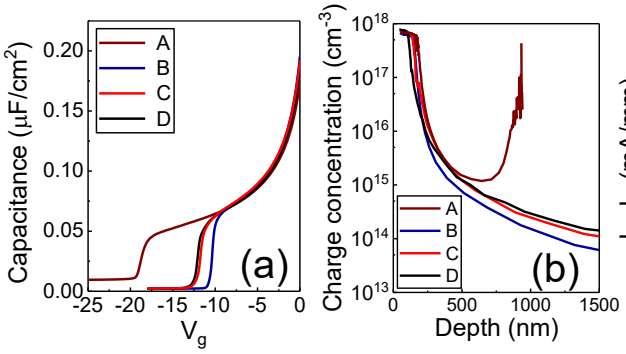


Fig.3 (a) Capacitance-voltage profiles (C-V, 100 kHz) (b) Extracted charge profile from C-V measurement. (c) Transfer characteristics for each epilayer grown. Dotted lines in (c) correspond to gate currents with the same color code.

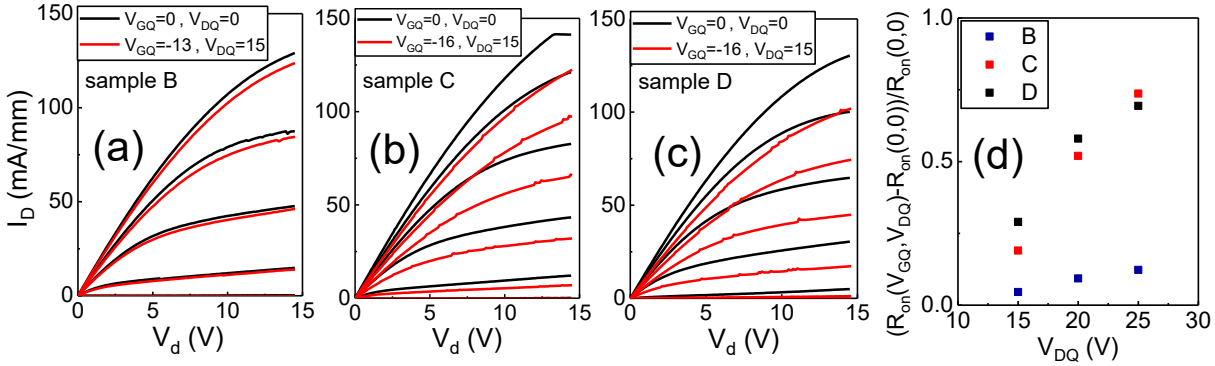


Fig.4 Pulsed I-V characteristics (pulse width-5 μs, period-5 ms) of devices with L_{gd}=5 μm, L_g=1.5 μm, L_{gs}=1 μm, (a) 500 nm UID buffer, (b) 1 μm UID buffer, (c) 1.5 μm UID buffer, (d) On-resistance degradation Vs drain quiescent.

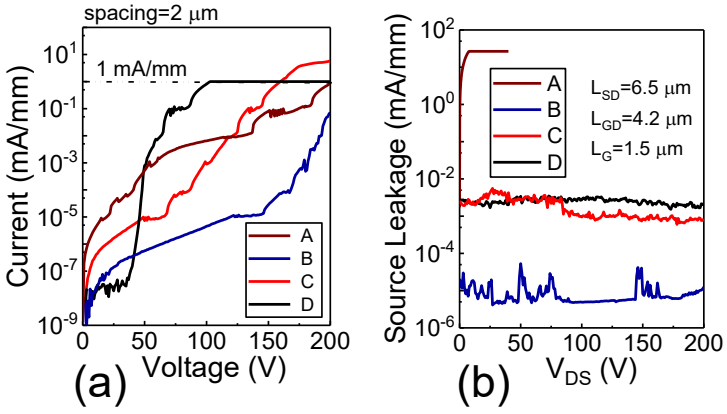


Fig.5 (a) Isolation leakage current comparison in samples A-D (b) Source leakage comparison measured as a function of drain voltage in transistor devices (V_g=$V_P - 4\,V$, where V_P is the pinch off voltage).