Wide and parallel LED-based optical links using multi-core fiber for chip-to-chip communications

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Abstract: We demonstrate >200 optical lanes in 0.5mm diameter imaging fiber with a speed-optimized GaN LED array, and independently, NRZ links of each LED to 10Gb/s over meters, extrapolating to >2Tb/s at a density >10Tb/mm^2.

1. Introduction

Advanced ICs typically have a wide internal bus running at a few Gb/s. However, given the limited number of pins, data is exchanged externally using SerDes running at much higher speeds. The SerDes-based I/O consume a great deal of power, often require FEC, have limited reach, and add latency. For decades, optics was seen as a potential solution to this bandwidth bottleneck, with devices such as quantum well modulators providing a wide parallel optical interface to ICs. However, devices that could be fabricated at high yield in arrays, operate at low currents, are "quantum impedance-matched" to transistors for low power operation, and could withstand the high operating temperatures were not available [1].

Recently GaN microLED displays have been demonstrated with millions of pixels and driven by CMOS backplanes using a lift-off procedure. We have optimized these devices for operation up to 10Gb/s, far greater than any LED on-off modulation demonstrated in the past [2]. Unlike semiconductor lasers, these devices operate over a -40˚C to 150˚C temperature range and show excellent reliability at high temperature. We have mated these CROME (Cavity-Reinforced Optical Micro-Emitter) arrays with CMOS-compatible lateral p-i-n photodetectors and used imaging fibers to make very wide optical interconnects operating in the visible. In this paper we demonstrate an array of more than 200 devices at a 30µm pitch coupled simultaneously through a 0.5mm imaging fiber. Since high-speed drivers are not yet ready in an array format, the CROME arrays were driven at low speeds. However, the same CROME was packaged with an external driver and showed excellent link characteristics up to 10Gb/s. The receiver was a CMOS-compatible lateral p-i-n structure with a discrete TIA and limiting amplifier. We plan to fabricate arrays of drivers and detectors to drive the entire array at high speed simultaneously and interface this to a standard parallel bus, like HBI, AIB, or BoW. This technology could enable new architectures, such as disaggregated systems, large combinations of XPUs for ML and faster and more extensive memory access.

2. Experiments

The CROMEs were speed-optimized microLEDs grown on a sapphire substrate with emission at about 420nm. A 16x16 element array was fabricated where the n-side was connected across rows and the p-side connected across columns. The spacing between the 10µm diameter devices was 30µm in both directions. The devices needed a 3V bias and about 0.8V modulation voltage and had an external quantum efficiency of about 5%. The high-speed devices were identical, but with individual contacts. We used a12Gb/s Anritsu PPG/BERT and a 6GHz HP network analyzer to test the small signal and link integrity of the CROMEs. Ideally, these devices would be lifted off and bonded to drivers, which is a standard process for microLED displays and would have a back reflector or possibly a collector or a microlens structure. However, in this case the tests were all done on the original sapphire substrates with no collection optics and butt-coupled.

On the receive side, detectors were fabricated in SOI substrates with 130nm device layer and 400nm buried oxide layer. The detectors had lateal interdigitated p-i-n contacts, with the p and n regions about 1µm wide and with 2.5µm spacing in between, and a total detector area of 30µm x30µm. The p and n stripes were matched to the source and drain structures of XFAB 130nm CMOS process. The configuration is extremely low capacitance per unit area, calculated to be <10fF for a device of this size. The absorption length of the light in silicon is about 0.2µm, thus even the thin device layer provides significant absorption. In fact, the measured quantum efficiency was about 50%, with the buried oxide giving a resonance at approximately the operating wavelength. An 11Gb/s Hilight HLR11G1 TIA generated 50 Ohm matched output. Fig.1a shows the 3dB electro-optical bandwidth of the LED source as a function of current density and for various sizes. As a comparison 3dB bandwidths of selected references are shown as well as devices made in a standard wafer without the speed optimization. Fig. 1b shows the 10Gb/s eye, with about 6dB of equalization. High speed modulation could be obtained down to currents of about 10µA on suitably sized devices with a higher sensitivity TIA.

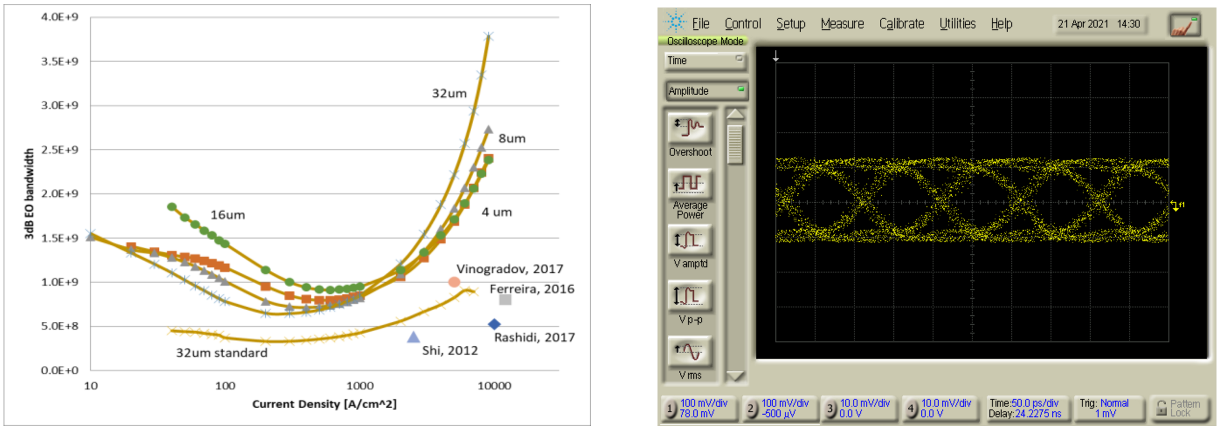

Fig. 1. On the left, 3dB electro-optic bandwidth of the high speed CROME, with comparison points [3-6]. On the right, 10Gb/s PRBS eye using in-house lateral p-i-n detectors with commercial hybrid drivers and TIAs.

The 0.5mm diameter fiber used was "imaging fiber" from Schott with approximately 5000 cores, with each core 4um in diameter. This fiber is optimized for borescope or endoscopy, and transmits the image of the array. Similar to previous work [7], the fiber was butt-coupled and the output of the fiber imaged with a camera. Since the diagonal of the rectangular array is about 650µm across, not all the 256 elements could be seen through the fiber. Fig. 2 shows the image at the output of the fiber, with about 230 devices visible. The measured was limited by noise, so for a more accurate measurement, a higher power blue laser was tightly coupled to a single core. The output of the imaging fiber was magnified and various points on the image sampled. Fig. 2b shows that the crosstalk between two adjacent cores of the fiber is about 27dB. In the case of the array, we would expect the crosstalk to be even lower since there are multiple dark cores between the lit ones.

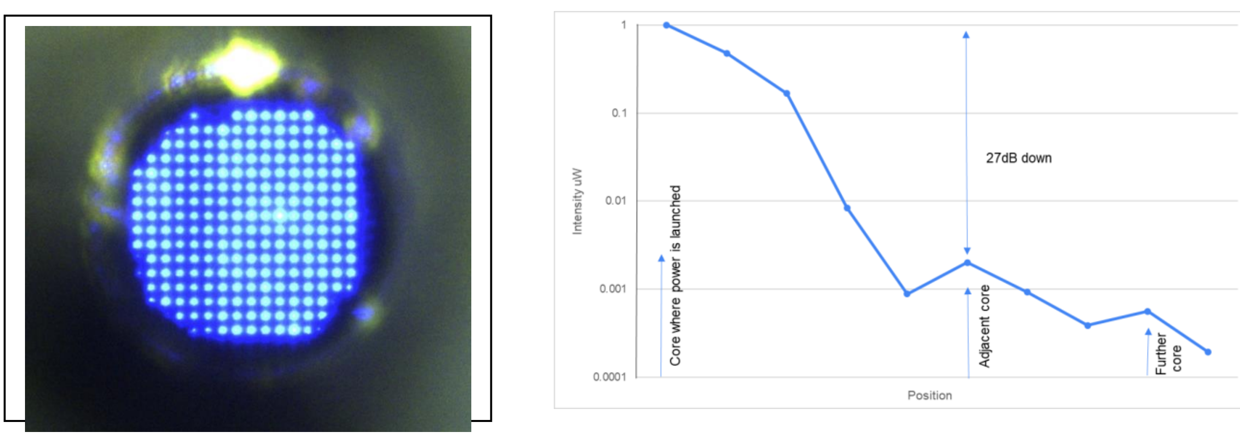

Fig. 2. On the left, the array shines through the imaging fiber. On the right, the fundamental crosstalk in the fiber is measured by illuminating one core with a laser and measuring power in other cores.

To accurately measure the effects of the fiber, different lengths of low NA fiber were used for dispersion penalty measurements and is shown in Fig 3 along with rough theoretical calculation of the expected modal and material dispersion of the glass. A 3dB penalty caused by material chromatic dispersion is observed at 3 meters.

One advantage of this highly parallel data transmission is that the clock can be sent along with the data eliminating the need for clock recovery. For this, low skew is essential. To get a rough measurement, two adjacent CROMEs were driven from the data and inverted-data output of the pattern generator, and different amounts of RF delay were added to one channel, with the summed signal measured on a single large commercial detector. The speed of the large detector limited the measurement to 2Gb/s. Fig. 3b shows the measured skew as a function of the length difference between the two arms, indicating no measurable skew as the fit goes through the origin.

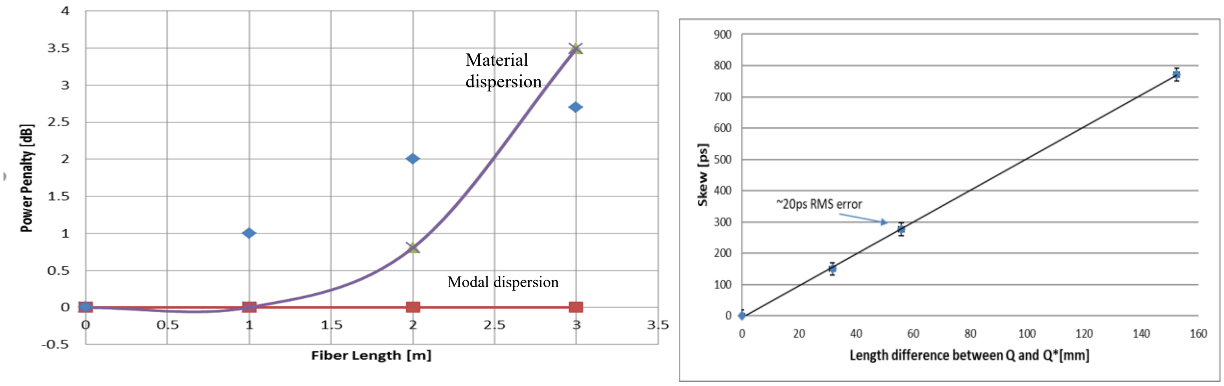

Fig. 3. On the right, the measured dispersion penalty of 10Gb/s signal through the fiber (dots), along with theoretical material and modal dispersion. Three meter links at 10Gb/s show about 3dB penalty. On the left is skew measurement at lower 2Gb/s speed, showing no measurable skew.

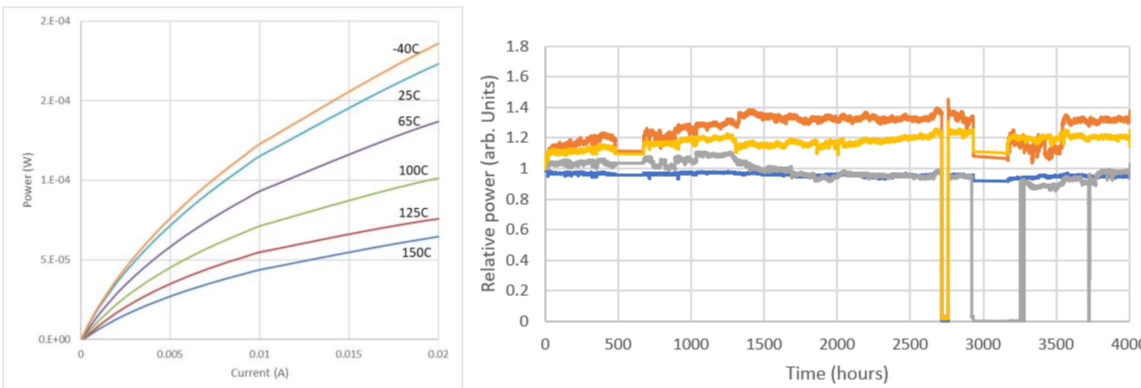

Fig. 4: Light output over temperature, collected into a low NA optical system. There is about 4dB change in power from -40˚C to 150˚C. A number of devices were run at 1.5KA/cm2 for 4000 hours at 100˚C and don't show significant degradation. The large step changes were due to tester issues where data was not being recorded.

Finally, the devices were measured at -40˚C to 150˚C, using dry ice for cooling and a heated stage. The CROME outputs do not vary dramatically with temperature, and there is no significant changes in S21 over temperature. Fig. 4 shows the power output of a CROME into a low NA optical system as a function of temperature. Fig. 4B shows an initial lifetest of a few of these devices at 100˚C and up to 4000 hours, with no significant degradation.

We believe this technology could prove very useful for the demanding chip to chip applications.

3. References

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