GridNet: Fast Data-Driven EM-Induced IR Drop Prediction and Localized Fixing for On-Chip Power Grid Networks*

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ABSTRACT

Electromigration (EM) is a major failure effect for on-chip power grid networks of deep submicron VLSI circuits. EM degradation of metal grid lines can lead to excessive voltage drops (IR drops) before the target lifetime. In this paper, we propose a fast data-driven EM-induced IR drop analysis framework for power grid networks, named *GridNet*, based on the conditional generative adversarial networks (CGAN). It aims to accelerate the incremental full-chip EM-induced IR drop analysis, as well as IR drop violation fixing during the power grid design and optimization. More importantly, *GridNet* can naturally leverage the differentiable feature of deep neural networks (DNN) to *obtain the sensitivity information of node voltage with respect to the wire resistance (or width) with marginal cost. GridNet* treats continuous time and the given electrical features as input conditions, and the EM-induced time-varying voltage of power grid networks as the conditional outputs, which are represented as data series images. We show that *GridNet* is able to learn the temporal dynamics of the aging process in continuous time domain. Besides, we can take advantage of the sensitivity information provided by *GridNet* to perform efficient localized IR drop violation fixing in the late stage design and optimization. Numerical results on 36000 synthesized power grid network samples demonstrate that the new method can lead to $10^5\times$ speedup over the recently proposed full-chip coupled EM and IR drop analysis tool. We further show that localized IR drop violation fix for the same set of power grid networks can be performed remarkably efficiently using the cheap sensitivity computation from *GridNet*.

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1 INTRODUCTION

The on-chip power delivery network (PDN) is a key global interconnects for physical implementation as it affects performance (IR drop, timing) as well as area and cost (routability, layout density, metal stack). At the same time, electromigration (EM) remains the top killer for copper-based interconnects in current and near-future advanced VLSI technologies. The International Roadmap for Devices and Systems (IRDS) [2] and the International Technology Roadmap for Semiconductors (ITRS) [1] predict that the allowable current density continues to decrease due to EM while the required current density to drive the gates continues to increase. As a result, the EM-related aging and reliability will become worse for current 7nm and below technologies.

For practical VLSI chips, the on-chip power supply or power-ground (P/G) networks are most susceptible to EM failures due to large and unidirectional current densities [6, 7, 11, 33]. From EM perspective, interconnect wire is usually a tree containing multiple segments with continuous metallization of one metal layer. Due to EM aging and failure effects, the voltage drop of PDN which meets the design requirement at the design time may become worse and leads to time violations as time goes by. As a result, PDN network design has to consider EM-induced aging and IR drop changes at the target lifetime to make them more robust.

In the past few years, research efforts focusing on so-called physics-based EM analysis tool for power grid network analysis method have been explored [9, 10, 12, 27]. However, all those methods need to solve the partial differential equations (PDE) of hydrostatic stress in the multi-segment interconnect wires. Due to the interplay between the stress and IR drops, a coupled time-varying EM and IR drop analysis is needed for accurate EM-induced time-varying IR drop analysis [27], which is very expensive (even without EM analysis) for full-chip PDN analysis.

The on-chip PDN networks typically go through many iterations between PDN designs, IR analysis and floorplan/placement updates before the final EM signoff analysis. Typically PDNs at this stage are well designed and sized to meet the IR drop (both static and dynamic IR drops) requirement. But IR drops at a few nodes may still fail for the target lifetime due to EM aging and failure processes. At this design stage, engineering change order (ECO) revisions or updates for the PDN layout will be carried out. Hence, there is a need for fast incremental EM-induced IR drop analysis for ECO like fixing for the PDN layout via proper sizing of some wire segments [8]. We want to point out that such fast EM-induced IR drop analysis is different than the traditional fast static and dynamic IR drop analysis methods [14, 17, 21, 28] as those methods mainly target at accelerating the design time dynamic IR drop analysis tool such as ANSYS RedHawk based on the power and timing information of the standard cells.

On the other hand, deep neural networks (DNN) have propelled an evolution in machine learning fields and redefined many existing applications with new human-level AI capabilities. DNNs such as convolution neural networks (CNN) have recently been applied to many cognitive applications such as visual object recognition, object detection, speech recognition, natural language understanding, and etc. due to dramatic accuracy improvements in those tasks [20]. Recently, generative adversarial networks (GAN) [16] gained much traction as it can learn features (latent representation) without extensively annotated training data. GAN-based methods have been applied for VLSI physical designs such as generation of various noise maps to facilitate the IR-drop noise sensor placement [22], for layout lithography analysis [30] and sub-resolution assist feature generation [4], for analog layout well generation [29]. However, the proposed GAN-based design and analysis techniques are mainly targeted for the statistical and static image generations (analysis). Less works have been explored to learn time-series data.

In this article, we present a new data-driven fast EM-induced IR drop analysis framework, called *GridNet*, for full-chip power delivery networks to address the need for fast incremental IR drop prediction for sensitivity based power grid optimization and ECO fixing. Contributions of this paper are as follows:

- We propose a fast data-driven EM-induced IR drop analysis framework based on the conditional generative adversarial networks (CGAN). *GridNet* treats the EM-induced time-varying voltage of power grid networks as the data series

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images which are conditional outputs of the given electrical features of wire resistance and current density of all wire segments. We show that GAN model can be adopted to learn temporal dynamics in the aging process of power grid networks by using the continuous time as one of the conditions.
- More importantly, we show that *GridNet* can not only perform fast if-then analysis for EM-induced IR drop estimation, but also *provide important sensitivity information of node voltage with respect to the wire resistance (or width) with marginal cost*. This is obtained by leveraging the differentiable feature of DNN networks as we can easily extend differentiable loss function of DNN networks for the input data as well.
- For our DNN model, we select resistance of all the wire segments, current sources attached at certain nodes as the electrical modeling features assuming the mesh-structured power grid networks with given voltage sources. Since we capture the IR drop in view of incremental circuit analysis, our model can be used on different PDN design with different workloads, different wire width and length without retraining as long as the main power grid structure and voltage sources remain unchanged.
- Once *GridNet* is trained, we show how to obtain the cheap sensitivity information from current DNN framework via the built-in automatic differentiation operations. Then we demonstrate how to perform a localized ECO and optimization efficiently to fix IR drop violations for late stage power grid designs.
- Numerical results on a number of synthesized power grid networks demonstrate that the new method can lead to five orders of magnitude speedup over recently proposed full-chip coupled EM and IR drop analysis tool. We further show that localized IR drop fix for the same set of power grid networks can be performed in a few seconds using the fast sensitivity computation from *GridNet*, which is extremely efficient.

This paper is organized as follows: Section 2 reviews the related works. Section 3 reviews one of the state-of-the-art EM-induced IR drop analysis methods, which serves as the baseline of the *GridNet* model. Section 4 presents the details of our GAN based EM-aware IR drop prediction method. Section 5 introduces the fast fix strategies for IR drop violations. Experimental results and discussions summarized in Section 6. Section 7 concludes this paper.

2 RELATED WORKS

We summarize a few related literatures on IR drop analysis, EM-induced IR analysis and mitigation schemes.

2.1 Machine learning based IR drop analysis and estimation

IR drop analysis (either static or dynamic) is concerned with voltage drop estimation from given current or power sources, which can be time-varying for dynamic analysis. A number of numerical techniques have been well developed and can perform IR drop analysis well on power grids, such as hierarchical methods, random walk methods, Krylov-subspace methods, multi-grid techniques, and vectorless verification methods.

To further speed up the IR drop analysis, several machine learning based IR drop estimation/prediction methods have been proposed [14, 17, 21, 28]. Those methods typically aim to replace the standard full-chip IR drop analysis tool such as ANSYS RedHawk, via data-based learning and feature selections. For instance, Lin *et al.* [21] proposed full-chip dynamic IR drop analysis based on some power and physical features extracted from cells and layouts. Fang *et al.* [14] tried to improve the scalability by training the models for localized region of layout. Xie *et al.* [28] proposed a CNN-based model transferable across different designs that is able to incorporate design-dependent features during preprocessing. Ho *et al.* [17] focused on incremental IR drop prediction and mitigation. It uses more electrical and physical features for the training based on the gradient boosting framework.

2.2 EM-induced IR analysis and fixing works

Since EM failure can lead to wire resistance increase and even open circuits, it can cause the increase of IR drops over time. As a result, it is very important to perform the EM analysis and eventually EM-induced IR drop analysis towards the user-specified target lifetime. A number of full-chip EM analysis for power grid networks have been proposed recently [10, 18, 25, 26]. These methods can predict the EM lifetime of the power grid and obtain failed trees. Specifically, Huang *et al.* proposed first physics-EM model based full-chip EM analysis method [18, 19]. This method indeed considers interaction between the EM and IR drops of power grids, but the compact EM model are less accurate. Chatterjee *et al.* proposed finite difference method (FDM) based full-chip EM analysis tool [10, 25] to get better accuracy. However, such method still primarily considers the EM stress without considering impacts from wire resistance changes of power grid networks. Cook *et al.* proposed a finite difference analysis method, which was accelerated by Krylov subspace based reduction technique [12]. This method can be applied to general multi-segment interconnect wires with time-varying current and temperature. However, this method still considers only the EM stress and ignores the EM and IR drop interaction in power grid networks.

Recently, Sun *et al.* [27] proposed a full-chip EM-induced IR drop analysis, which considers dynamic interplay between the hydrostatic stress and electronic current/voltage in a power grid network. This method solves the coupled time-varying partial differential equations in time domain accurately and obtains the stress evolution in multi-segment interconnect trees. It is compatible with the synthesized power grid networks from commercial design tools and can show the resulted IR drop and EM failure hotspots at the target lifetime. However, the simulation can be very slow and hence not practical to use for fast EM fixing. This is one of the major issues that motivate our work.

On the other hand, there are a number of works proposed recently on wire segment sizing of power grid networks in order to fix the EM failures and IR drop considering the multi-segment interconnect wires. Zhou *et al.* [31, 32] proposed a power grid network sizing method based on the multi-segment EM immortality check criteria. It automatically considers all the wire segments and their interactions in an interconnect tree. However, the EM immortality constrained optimization is still conservative as it requires all the interconnect trees to be immortal, i.e., void nucleations are not allowed. Chang *et al.* [8] proposed a machine learning based EM violation waiver system, which investigates every EM violation and take an expert decision to either ignore (waive-off) the violation or resolve it (must-fix) in the design. However, this system cannot take the violation fix action. Moudallal *et al.* [23] directly optimized EM-induced IR drops on the time-varying power grid networks due to the EM aging process. This method is based on a gradient descend optimization and aims to size the individual wires to meet the target IR drop criteria. However, large amount of computation is required.

3 PRELIMINARIES FOR FULL-CHIP EM-INDUCED IR DROP ANALYSIS

EM aging process typically leads to resistance increase or even open wire segments over time. However, for on-chip mesh-structured power grid networks, due to its inherent redundancy, a few wire failures may not immediately result in significant IR drop increase. But as more wires nucleate, the IR drop will eventually lead to timing violations. As a result, the power grid networks become time-varying networks with time-varying IR drops due to the EM induced aging process [10, 18]. On the other hand, the failed wire segments alter

the current distributions of all the interconnect wires, which may further accelerate the failure process. Hence, one has to consider the interplay between the two physics: the electronic and hydrostatic stress in the interconnect wires. In this work, we show how it can be integrated with commercial EDA tools to achieve the EM signoff analysis.

In this section, we briefly review the coupled electronic and stress analysis method on the full-chip power grid EM check, *EMspice* [3, 27], which represents the latest development for EM-induced IR drop analysis. This method is used for the baseline for the proposed IR-drop incremental prediction method. *EMspice* takes power grid netlists from Synopsys IC Compiler (ICC) flow, and tells which wires will fail, their resistance changes and resulting in increased IR drops of the power grids over the aging time.

The entire EM check in *EMspice* consists of several steps. In the first step, the power grid information is constructed from Synopsys ICC during the physical synthesis process for a specific design. Second, the power grid and corresponding branch current are passed to the EM immortality filter to remove all the immortal wires. The tool considers the wire immortality for both nucleation and incubation phases. Thirdly, it is to solve the stress and IR drop of interconnect wires in a coupled way. The coupled solver consists of a finite difference time domain (FDTD) solver for EM stress [10, 12] and a linear network DC IR drop solver. Lastly, all information will then feed into the EM check framework graphical user interface (GUI) for interactive user analysis.

In the third step, the coupled FDTD EM solver and linear network IR drop analysis can be described as

$$\begin{aligned} \mathbf{C}\dot{\sigma}(t) &= \mathbf{A}\sigma(t) + \mathbf{P}I(t), \\ \mathcal{V}_v(t) &= \int_{\Omega_L} \frac{\sigma(t)}{B} d\mathcal{V}, \\ \mathbf{M}(t) \times u(t) &= \mathbf{P}I(t), \\ \sigma(0) &= [\sigma_1(0), \sigma_2(0), ..., \sigma_n(0)] \text{ , at } t = 0 \end{aligned} \tag{1}$$

where $\mathbf{M}(t)$ is the admittance matrix for the power grid network, which is time-varying due to the fact that wire resistance changes with EM failure effects. $\mathbf{P}$ is a $b \times p$ input matrix, where p is the number of inputs, i.e., the size of current sources $I(t)$. $u(t)$ represents the nodal voltages of the network and $I(t)$ are the current sources from the function blocks of the chips. $\mathbf{C}, \mathbf{A}$ are $n \times n$ matrices. And n is the number of nodes. Note that $\sigma(0)$ denotes the initial stress at $t = 0$. For each new simulation step, the stress from previous simulation step is used as the initial condition, iteratively.

The above equations in Eq. (1) are coupled and must be solved together. Linear network IR drop solver passes time-dependent current densities and P/G layout information to the FDTD EM solver. Once the voids are formed, IR drops in the power grid will change and the current at each time step will be different. The FDTD EM solver provides the IR drop solver with new resistance information, particularly, wires with voids. Since these two simulations are coupled together, wire current and resistance on each mortal wire are dependent on each other. Note that $\mathbf{C}, \mathbf{A}$ matrices dependent on wire structures are time-independent in the coupled equation. Such coupled analysis on long target lifetime can be extremely time consuming for very large power grid networks [27]. As a result, it is indeed necessary to build a fast EM-induced IR drop estimation for incremental wire changes for IR drop ECO process.

4 FAST DATA-DRIVEN INCREMENTAL EM-INDUCED IR DROP PREDICTION

4.1 Overall workflow of the *GridNet* framework

Fig. 1 shows the overall workflow of the proposed *GridNet* framework. The workflow consists of two phases: training and inference. The training phase is shown in Fig. 1(a), the yellow block shows how the power grids are generated. Then in the red block, we use *EMspice* [27] to predict the EM-induced IR drop for synthesized power grid network using coupled EM-IR analysis. In the blue block, *GridNet* receives the EM-induced voltage from 0 to T_{target} aging years as well as the power grid. It extracts electrical and other information features, the training process is shown with dashed arrows. Fig. 1(b) illustrates the inference phase and the sensitivity-based power grid fixing flow. One of the two outputs from *GridNet* is the EM-induced voltage at all the nodes at a specific aging year. And the other is the sensitivity information: sensitivity of nodal voltages with respect to the input resistances. These resistances can be obtained as a by-product from the differentiable CGAN model as we will show later. The sensitivity information will be utilized for fixing IR drop violations efficiently in the chip design flow. After incrementally updating the power grid, the new EM-induced voltage is predicted by the *GridNet* model. If IR drop violations still remain unaddressed, the designer can just iteratively perform the same round of incremental prediction and fixing until all IR drop violations are fixed.

4.2 Feature selections for *GridNet*

Given a mesh-structured power network, if we only look at the node voltage, and input current sources, and according to Eq. (1), we can formulate the time-varying model essentially as following

$$\mathbf{M}(t) \times u(t) = \mathbf{P}I(t), \tag{2}$$

where $\mathbf{M}(t)$ is a modified nodal analysis (MNA) matrix, $I(t)$ is a column vector whose elements are current and voltage sources, and $u(t)$ contains both nodal voltages and dependent current variables. As a result, for the DNN-based modeling, the input features should include both $I(t)$ and $\mathbf{M}(t)$, which can be represented by the resistance vectors of wire segments in the power grid networks. The resistance of a wire depends on its length and cross-sectional area that is proportional to wire width. Since we deal with mesh-structured power grids, the topology of wire connections are implicitly presented if all the wire resistance or features are pre-ordered (as a vector) based on some counting order. As a result, the *GridNet* model is able to deal with different workloads, i.e., $I(t)$ and initial wire resistances (different $\mathbf{M}$ at $t = 0$ under the same power grid structure).

4.3 Training data preprocessing and representation

The preprocessing extracts the electrical features and geometries from raw layouts. After the preprocessing, the workload samples will be represented in a customized scheme.

Data preprocessing. Given a specific design, Synopsys ICC takes a synthesized gate-level netlist and a standard cell library as input, and then automatically create the circuit layout. In the preroute (design planning) step, one important procedure is performing power network synthesis. As shown in Fig. 2(a), the power and ground network are generated based on the constraints that the user defines. It consists of VDD power nets, VSS ground nets, and two external supplies. The results are later used to examine the voltage drop, resistance and EM. Fig. 2(b) shows the voltage drop from the same power grid and the unit is mV. Since our goal is to obtain EM-induced IR drop which considers aging effect, we dumped the power grid information including layout geometry, layer, via, as well as branch currents for later simulation.

Having sufficient amount of training data is a crucial requirement for machine learning approaches. The GAN-based EM-induced IR drop prediction requires a lot of power grid samples and their corresponding ground truth EM-induced IR drop along the aging time. However, synthesizing a large amount of designs and dumping their power grid information is not realistic. We first synthesized three power grid designs, and then for each design we generated 10000 different workloads respectively. They network samples have the same topology as the synthesized designs. Although they have the

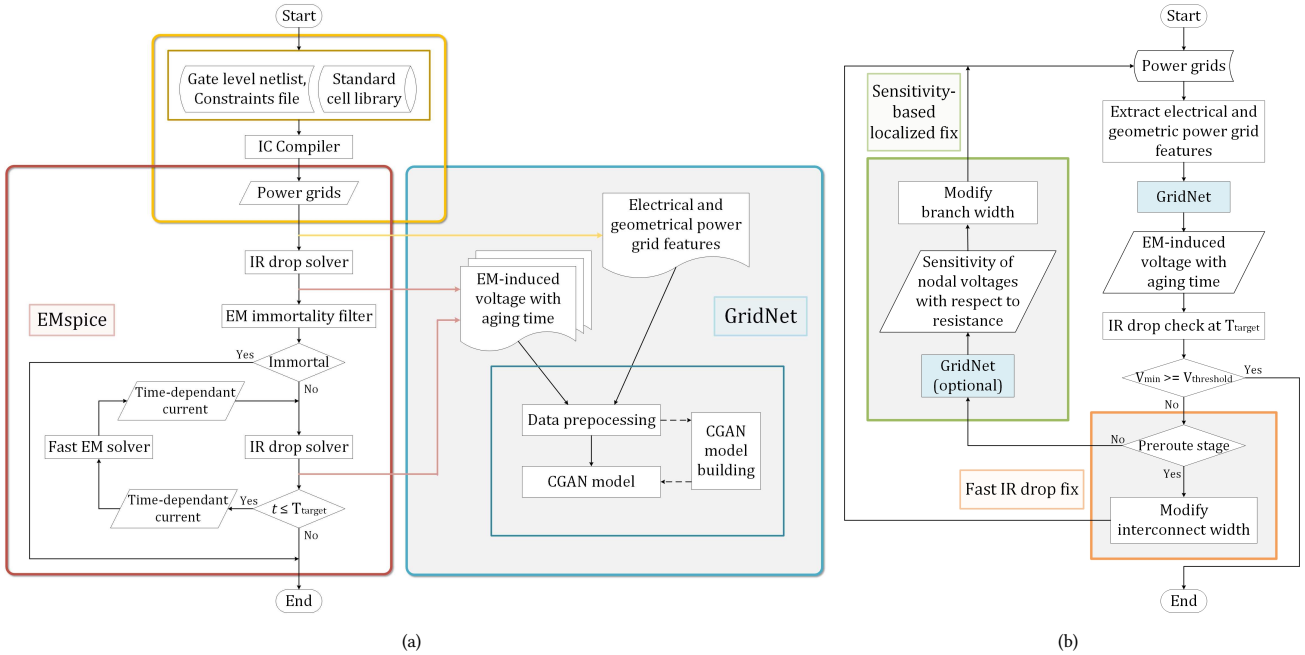

Figure 1: Proposed *GridNet* framework: (a) Training flow; (b) Prediction flow and grids fix flow with *GridNet*.

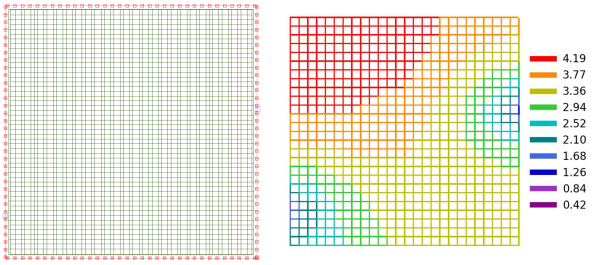

Figure 2: (a) Power and ground networks of Cortex-M0 DesignStart; (b) Voltage drop map of the power network of (a).

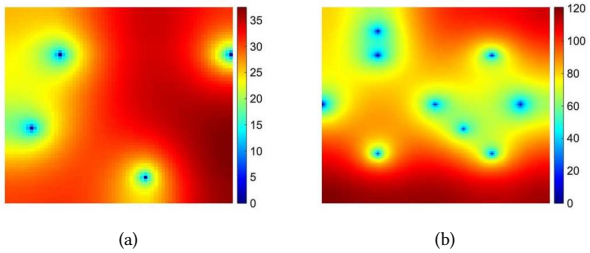

Figure 3: Compact IR drop image of power grid networks (a) *Design 2*: 4k nodes; (b) *Design 3*: 16k nodes

same number of power strips, they differ in the branch width and length, thus the wire can be sized properly later on for EM-induced IR drop fixing.

Data representation. Representation of data has a tremendous impact on the GAN behavior. To preserve the geometric and spatial relationship, we first encode the power grid workloads and voltages into matrices and then convert the voltage matrix into red-green-blue (RGB) channels of images, as illustrated in Fig. 3. Each pixel stands for one node, the length and width information are discarded, while the relative position of each node and its voltage value are kept. Such compact representation will dramatically reduce the image size compared with the representation from Fig. 2(b), which will further speed up the training process.

As the pixels in our images are not RGB colors but real voltage values instead, they usually do not change dramatically, e.g., the maximum voltage value is 1.05V and most values fall in the range [0.7 1.05]. The channels of input are real resistance and current, thus they have the same numerical problem. Such a small numerical range is not suitable for neural networks. As a result, we rescaled all data in the training to the range between -1 and 1.

4.4 The proposed GridNet architecture

GAN is a neural network model widely used in unsupervised machine learning tasks. A traditional GAN is composed of two separate deep neural networks, one is generator G and the other is discriminator D, there is no control on modes of the data being generated. In the CGAN model, the generator learns to generate a fake sample with a specific condition rather than a generic sample from unknown noise distribution.

For our problem, *GridNet* does not generate voltage maps from the random noises, instead, the inputs are the selected electrical and implicit geometrical features of the power grid networks and aging time. In order to implicitly learn the distribution of the voltage and map it to the corresponding 2D voltage image, we use a CGAN as backbone for our model shown in Fig. 4. As we can see, to make the GAN model to learn the temporal dynamics of EM-induced IR drops, we propose to use the time variable as the continuous condition for both generator and discriminator, which was demonstrated to be effective for financial market risk analysis [15].

Take a power grid design with 120 rows and 120 columns as an example, there are five channels of input for the generator: the column resistance image $img_{col} \in \mathbb{R}^{119\times120\times1}$, the row resistance image $img_{row} \in \mathbb{R}^{120\times119\times1}$, the current source image $img_{cur} \in$

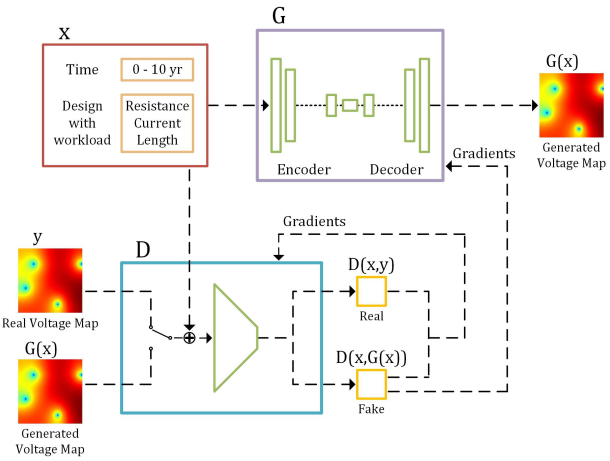

Figure 4: The proposed CGAN architecture for EM-induced voltage prediction

$\mathbb{R}^{120\times120\times1}$, wire length l, and aging time t. t and l are expanded into $\mathbb{R}^{128\times128\times1}$ by channel-wise duplication, respectively. In addition, the three images are all expanded to the same size, such that img_{col}, img_{row}, img_{cur}, l and t can be concatenated depth-wise. The resulted input x given to the generator is a $128 \times 128 \times 5$ tensor with all entries normalized as described in previous section. We employ an encoder-decoder architecture as our generator that is widely used in image-to-image applications. The input is downsampled through a series of convolutional layers until a bottleneck layer, at which the latent features are extracted and then reversely upsampled through transposed convolutional layers. The generator is trained to extract useful latent features from input and then reconstruct the output voltage map basing on these information.

The output of the generator is a voltage map, which is denoted as $G(x)$. Either the generated $G(x)$ or the real EM-induced voltage image y is fed into the discriminator D alternatively together with its corresponding workloads and aging time x as the condition input. The output of the discriminator is denoted as $D(G(x), x)$ or $D(y, x)$ depending on whether the generated or the real EM-induced voltage image was inputted. In the training process, we use the Wasserstein Distance [5] as the measurement of the difference between the real and the generated EM-induced voltage image distribution to take advantage of higher stability and convergence possibility.

4.5 Fast sensitivity calculation using the automatic differentiation in DNNs

One important observation for all the deep neural networks including GAN model is that they are all differentiable with respect to the model weights so that training can be performed by sensitivity/gradient information via the automatic differentiation scheme, specifically the back-propagation algorithm.

In this work, we leverage the existing automatic differentiation to compute the sensitivity information between the output and all of input resistance through *GridNet*. To be specific, we can compute the partial derivatives of one output voltage map with respect to every input resistance in one back propagation (same cost of one inference) of the generator DNN network using the Tensorflow tf.gradents API, which is exactly the same technique employed in the training process. The only difference here is that the derivative is taken with respect to the input of the generator instead of the trainable variables in the model. In other words, one has to perform one inference using *GridNet* to compute sensitivity for k resistances for one output node. Our sensitivity calculation is similar to the adjoint network based approach [13], however, this method requires two simulations of the *EMspice* for the original and adjoint networks for each output node. In our case, we do not require computing the sensitivities for all the output nodes, instead, we only focus on a few nodes that are subject to IR drop violations, which makes the sensitivity computation even more efficient.

5 FAST LAYOUT FIXING FOR EM-INDUCED IR FAILURES

Power network is usually synthesized at an early stage of chip design flow. Given a power gird, it is possible that it is vulnerable at the target time T_{target}. In other words, the maximum IR drop exceeds the voltage drop threshold $V_{drop_{th}}$, thus the design flaws need to be fixed. Specifically, the EM-lifetime of the power grids refers to the time at which an EM-induced voltage failure is expected to happen. There are two failure scenarios: vulnerable in the initial state; robust initially, but has EM-induced voltage violations at T_{target}.

In this section, we present two fast localized fixing methods based on the proposed *GridNet*. The proposed methods are targeted for ECO like process to fix a few IR drop violations. In section 5.1, we introduce a method that uses a relatively rough estimation to expediently fix IR drop failures at the preroute stage. In section 5.2, we present another way, on the contrary, the method only takes the second failure scenario into account. It benefits from the gradient information obtained from *GridNet*, We assume that only a few EM-induced IR drop violations will occur at T_{target} during the later power grid design stages such as EM signoff. This is typically the situation as the power grid network has been well designed at the synthesis step with EM failure considerations.

5.1 Fast localized IR drop fixing

The first localized fix method tries to size whole interconnect tree one at time until we meet the IR drop constraint at the targeted lifetime. Specifically, after a power grid network is synthesized, multiple voltage violations may occur at T_{target}. With *GridNet*, we can easily obtain all the nodal voltages at T_{target}. In addition, *GridNet* is able to provide the EM lifetime of the power grid.

Starting from the original power grids, widening one interconnect tree can have inevitable effects on nearby trees, namely, fixing several critical trees may be sufficient to fix voltage violations on all trees within this local area. Therefore, there is no need to widen all vulnerable trees at the same time, which would result in large design overhead. In our method, if voltage violations happen, the interconnect with the largest IR drop will be widened by a scaling factor s, where $s > 1$ and it is determined by experiments.

According to Moudallal *et al.* [23], the voltage drop is a monotonically increasing function with respect to aging time given a certain grid sample, thus we only need to look at T_{target} without considering any time in between.

The modified power grid information is then fed into *GridNet* to get the newly predicted nodal voltages at T_{target}. We iteratively predict voltages and widen one tree at a time until the IR drop of all nodes are bounded within $V_{DD} - V_{drop_{th}}$.

According to the design rules and the minimum allowed space for standard cell placement and routing, the interconnect wire must be modified in a manner under some specific constraints. In our method, we specify that each wire can be widened under those design rules, but they have a maximum allowed value.

5.2 Sensitivity based localized IR drop fixing

As we discussed, the sensitivity information of node voltage with respect to the wire resistance can be obtained as by-product from the CGAN model of *GridNet* for each given input design using simple back propagation as mentioned in Section 4.5. Typically the candidate wires (and its wire segments) are the wires with or close to void

nucleations. As a result, those wires are good candidates for fixing as they are the ones causing the EM-induced IR drop failures.

Specifically, we assume that we have n violation nodes whose nodal voltages are represented by v_i, $i \in \{1, .., n\}$ and m wire segments whose with are represented by w_i, $i \in \{1, ..., m\}$. Then we can compute the following partial sensitivity matrix $\mathbf{S}_{n\times m}$:

$$\mathbf{S}_{n\times m} = \begin{bmatrix} \frac{\partial v_1}{\partial w_1} & \frac{\partial v_1}{\partial w_2} & \cdots & \frac{\partial v_1}{\partial w_m} \\ \frac{\partial v_2}{\partial w_1} & \frac{\partial v_2}{\partial w_2} & \cdots & \frac{\partial v_2}{\partial v_m} \\ \vdots & \vdots & \ddots & \vdots \\ \frac{\partial v_n}{\partial w_1} & \frac{\partial v_n}{\partial w_2} & \cdots & \frac{\partial v_n}{\partial w_m} \end{bmatrix} \tag{3}$$

Let $\Delta\mathbf{V} = [\Delta v_1, ..., \Delta v_n]$ represent the voltage drop changes we expected to meet IR drop constraint at T_{target} and $\Delta\mathbf{W} = [\Delta w_1, ..., \Delta v_m]$ be the required first order width changes to make the voltage drop change. Then we have

$$\Delta\mathbf{V} = \mathbf{S} \times \Delta\mathbf{W} \tag{4}$$

To solve $\Delta\mathbf{W}$, we perform the least square regression as follows:

$$\begin{aligned} \mathbf{S}^T\Delta\mathbf{V} &= \mathbf{S}^T\mathbf{S} \times \Delta\mathbf{W} \\ \Delta\mathbf{W} &= (\mathbf{S}^T\mathbf{S})^{-1}\mathbf{S}^T\Delta\mathbf{V} \end{aligned} \tag{5}$$

We note that the required width changes $\Delta\mathbf{W}$ may also be subject to the design rules as there is upper bound for the width. Once we update the width changes to the power grid network, we will run *GridNet* to verify IR drop at T_{target}. If there are still IR drop violations, more sensitivity based fixing will be performed until there is no IR drop violation. The final design will be validated by *EMspice*.

6 EXPERIMENTAL RESULTS AND DISCUSSIONS

6.1 Experiment setup

The proposed EM-induced IR drop prediction model for power grids (*GridNet*) has been implemented in Python using the *TensorFlow* library. The voltage violation fixing methods are implemented in Python. The experiments were carried out on a Linux server with 2 Xeon E5-2698v2 2.3GHz processors and Nvidia Titan X GPU.

In order to validate our work, we start from the power grid of the Cortex-M0 DesignStart processor. It is a 32-bit processor that implements the ARMv6-M architecture. This processor is synthesized using Synopsys Design Compiler, and is placed and routed with Synopsys 32/28nm Generic Library. The power grid of Cortex has two layers, and there are 1k nodes in total.

Power grid information obtained from Synopsys ICC is then fed into the power grid parser. The information includes but is not limited to structure, node location, wire layer, wire length, current source, voltage source and resistance values. The netlist format extracted from the grids agrees with IBM power grid benchmarks [24]. In order to obtain enough power grids for training, we generate lots of synthesized IBM-format power grid networks so that different workloads can be tested and verified.

We train our DNN model using three different designs/topologies and each of them has a dataset containing 12000 pairs of (workloads and aging time, EM-induced IR drop) samples. *Design 1* comes from Cortex-M0, *Design 2* and *Design 3* are shown in Fig. 3(a) and Fig. 3(b), respectively. The temperature used in the experiment is 373K, the IR drop threshold $V_{drop_{th}}$ is $10\%V_{DD}$ and the target EM lifetime T_{target} is set to 10 years. For each workload, we collect the EM-induced IR drop results obtained by *EMspice* at 11 discrete aging time instants (0 to 10 years). We randomly select 15% workloads for testing and the remaining 85% are assigned for the training set. During the training phase, all samples are randomly permuted at the beginning of every epoch.

6.2 EM-induced IR drop prediction results

6.2.1 Accuracy. Once the *GridNet* model is trained, the generator is preserved and serves as the model for inference. The model can take any power grid workload with the same topology as input and give the predicted EM-induced voltage at a specified aging year. The predicted results from *GridNet* are compared with the baseline, which are the simulation results from *EMspice*. To evaluate the estimation error, we employ the root-mean-square error (RMSE) and as the metrics

$$RMSE = \sqrt{\frac{\sum_{i=1}^{N}(y' - y)^2}{N}} \tag{6}$$

where y' and y are the predicted and real voltage value, respectively. N is the total number of nodes. We evaluate our trained *GridNet* model on the testing set which was set aside during the training phase. The workloads in the testing set were randomly generated in the same way as the training set was produced. The random generation process guarantees that there is no overlap between these two datasets. The details and results are shown in Table. 1.

Table 1: Prediction results of different designs

circuit	# nodes	# voltage sources	V_{DD} (V)	RMSE (mV)
Design 1	1024	2	1.05	5.697
Design 2	4096	4	1.05	6.100
Design 3	16384	9	1.05	3.922

A total number of 1800 different workloads are tested for each design. For each workload, 11 voltage images at 0 to 10 discrete aging years are generated. As can be seen from Table 1, comparing all 19800 generated EM-induced voltage images with the baseline on *Design 1*, *GridNet* achieves an average RMSE of 5.697mV, which represents about 0.57% error for 1.05V power supply.

We randomly pick one testing workload from *Design 2* and compare the EM-induced voltage estimation at different aging years with the baseline in Fig. 5. Fig. 5(a) shows the predicted and real voltages at 0, 6 and 10 years, respectively. Since there is no obvious difference can be seen, we zoom in the upper right corner of the design and use Fig. 5(c) to demonstrate the prediction error. Initially, the error distributes evenly, while at the end of 6th year the error grows larger at two spots. The maximum error at 10 years is only 0.04mV, which indicates a good prediction. Fig. 5(b) illustrates the EM-induced IR drop increasing process. The left figure shows that from 0 to 6 years, the IR drop at some spots increases faster than the other nodes. When comparing the right figure to the left, we can find that the spots are spreading over time. The reason is that there are nucleated voids nearby and the EM aging process leads to the resistance increase.

We further compare the predicted EM-induced IR drop with baseline on *Design 1.1* and *Design 1.2*. To validate whether our model can successfully predict the IR drop of unseen power grids, all the testing data is separated from training data. The error statistics are shown in Table. 2, where *std* stands for standard deviation.

Design 1.1 is a power grid with one mortal interconnect and the initial maximum IR drop is 58.75mV. After one year, the resistance of the mortal interconnect begin to increase due to EM and the value is changing over time. After 10 years, the maximum IR drop becomes 59.54mV, which means the EM lifetime meets the 10 year target. In contrast, the predicted IR drop in the initial state and after 10 years are 57.93mV and 59.95mV, respectively. Fig. 6(a) presents the correlation between the predicted EM-induced IR drop and baseline from 0 year to 10 years, with one year interval, e.g., the purple dots indicate IR drop at 10 years. The errors of all predicted values are less than 3.5mV. The average error is 4.04×10^{-4}mV, with standard deviation of 7.52×10^{-4}mV.

Design 1.2 is a power grid with 6 mortal interconnects and its EM-lifetime is just 3 years. Initially, the real maximum IR drop is

Table 2: Error statistics of Design 1.1 and Design 1.2

circuit	initially				at 3th aging year				at 10th aging year			
	mean (μV)	max (mV)	std (μV)	RMSE (mV)	mean (μV)	max (mV)	std (μV)	RMSE (mV)	mean (μV)	max (mV)	std (μV)	RMSE (mV)
Design 1.1	0.8165	3.4879	0.6115	1.0199	0.7382	2.5299	0.6999	1.0170	-0.3939	1.1503	0.8030	0.8941
Design 1.2	18.8496	3.8722	0.9303	2.1058	31.1950	12.8284	1.2347	3.3547	82.7170	27.0619	2.5941	8.6685

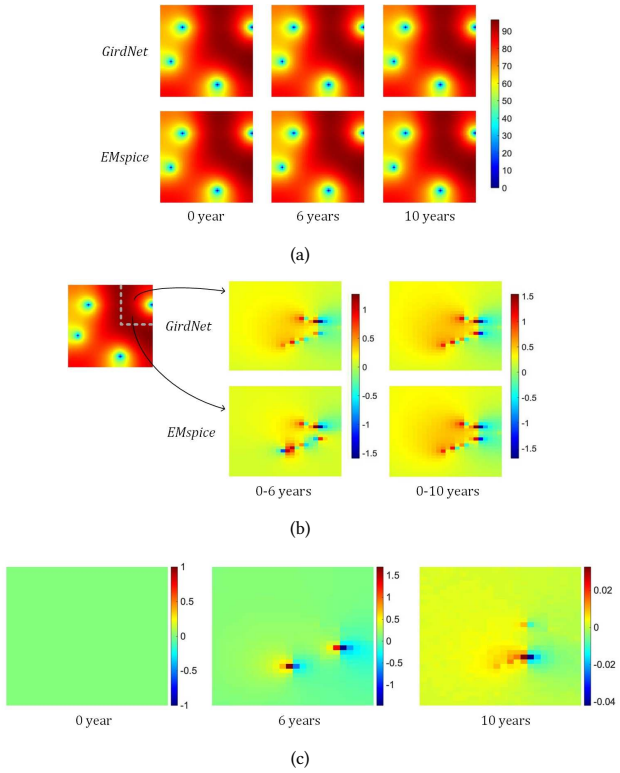

Figure 5: Comparison of inference results from *GridNet* and *EMspice*. (a) IR drop distribution at different years; (b) increased IR drop due to EM; (c) predicted voltage error.

84.47mV whereas the predicted maximum IR drop is 82.34mV. After 3 years, the EM-induced values become 84.58mV and 85.56mV for the baseline and predicted values respectively. From the 4th year, wire resistance starts to increase, which will have large impacts on the whole grid. As a result, both the baseline and predicted one have the maximum IR drop larger than 110.83mV, resulting in a power grid failure. Finally, at 10th year, the baseline and the predicted IR drop value are 133.99mV and 127.39mV, respectively. From Fig. 6(a) and Fig. 6(b), we can see that the correlations for different years in the first figure have similar patterns. On the other hand, the second figure looks different, the data for the first few years are concentrated in the lower part and the data for last few years are distributed throughout the whole figure. The reason is that the EM effect is more clearly reflected in *Design 1.2*, which has larger resistance increase.

The error histogram in Fig. 7 shows the error distribution of the predicted results. In Fig. 7(a), most of the predicted results are concentrated near the center, which agrees with the above analysis. As for Fig. 7(b), the error distribution for different years varies, because there are relatively large changes in the nodal voltages due to EM. When we look at the details of each year, we can find that the error still follows the uniform distribution. For instance, at 10th year, 87.79% of the nodes have errors between 8.13mV and 13.8mV.

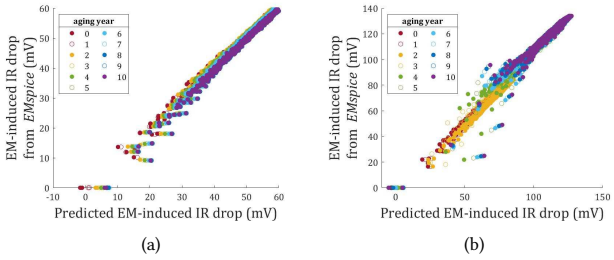

Figure 6: Predicted IR drop versus baseline of (a) Design 1.1; (b) Design 1.2.

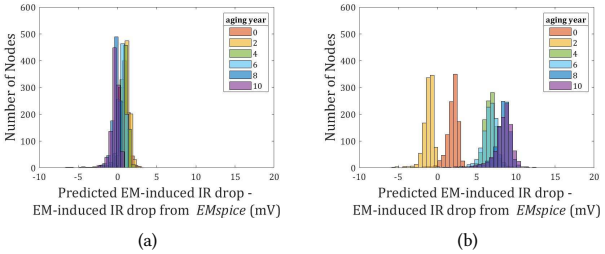

Figure 7: Error histogram of (a) Design 1.1; (b) Design 1.2.

We further do accuracy study on the EM lifetime prediction for power grid networks. We randomly select 700 mortal designs/workloads from the testing sets, the lifetime prediction results are shown in Fig. 8. Among the designs, the prediction from *GridNet* is consistent with the baseline for 83% cases. If we allow two year prediction errors, then it agrees with the baseline in 90.86% cases. The accuracy degradation is due to the fact that lifetime is more related to the minimum voltage rather than all nodal voltages.

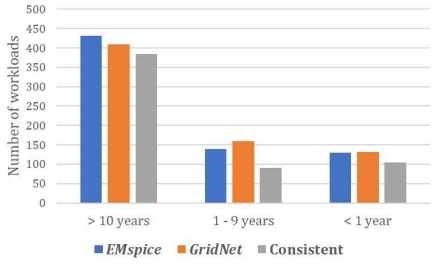

Figure 8: Predicted lifetime versus baseline.

6.2.2 Prediction speedup analysis. In what follows, we provide a comparison of speed between *GridNet* and the baseline *EMspice* on EM-induced voltage analysis. We randomly pulled the designs from both training and testing set from *Design 1*, which contains 1k nodes. Both our *GridNet* model and *EMspice* were tested to generate the voltages from initial state until 10 years. Specifically, the simulation time step of *EMspice* is set to one month. The experiments were

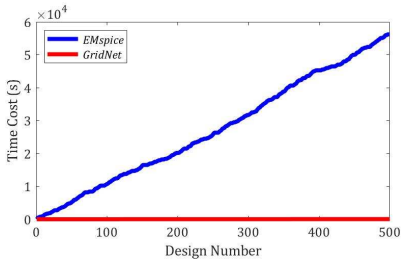

Figure 9: Prediction performance comparison between *EMspice* and *GridNet*

performed on the same server and the accumulating time cost on 500 designs are plotted in Fig. 9.

The total computing time on the 500 designs are 31.26h and 10.0s for *EMspice* and *GridNet*, respectively, indicating that about 11232 or $10^4\times$ speedup over *EMspice*. For *EMspice*, the time cost on the estimation of a single design varies from 0.57s to 427s depending on the EM immortality condition. For *GridNet*, however, the inference speed is steadily around 5ms for all the designs. The computing cost of *GridNet* is invariant to immortality conditions, which makes it much more suitable for larger scale designs and leads to a better scalability.

As for larger designs, the speedup becomes even more significant since the simulation time for *EMspice* grows considerably. For instance, for *Design 3* which has 16k nodes, obtaining the EM-induced IR drop result at the 10th aging year takes more than 1.5h. If applying the proposed *GridNet*, the inference time will be around 10ms, which indicates that the speedup will be more than 5×10^5.

6.3 Results from the fast IR drop fixing scheme

Now we show how to perform a quick IR drop fixing based on *GridNet*. We employ two strategies for the IR drop fixing. Here we mention the first one.

The result of the fast IR drop fixing method using prediction results from *GridNet* are listed in Table 3. The last column in this table and following table indicate CPU times used for the fixing process including data processing and inference costs of *GridNet*. There exist some benchmarks which do not satisfy the target EM lifetime with their original width configuration. In this case, we widened the most vulnerable interconnects to make the tree less likely to fail. As we can see, in *Design 1.a* example, there are 9 mortal wire in the beginning. At the same time, the minimum voltage of the power grid is 0.9201V, which is a 12.37% voltage drop, meaning that the EM lifetime is 0. Following the method discussed in Section 5.1, after the first time width adjustment, the number of mortal wires reduce from 9 to 7, however, the maximum voltage drop is 10.8% which still does not meet our design requirement. In the second iteration, we keep modifying the same interconnect, after that, the number of mortal trees is reduced to 6, with a 1.93% area increase compared to the original design. In the third iteration, another interconnect is widened, after modification, there still exists 5 mortal wires, however, all the voltage drops in the initial state are within 10%, and after 10 years, the minimum nodal voltage is 0.9461V, which meets the 10 year target.

Table 3: Results of fast IR drop fixing method

circuit	# mortal wires	original lifetime	# iter	# widened wires	area increase	total time
Design 1.a	9	0 yr	3	2	3.31%	0.6644s
Design 1.b	3	8 yr	1	1	0.45%	0.2865s
Design 2.a	6	3 yr	2	2	1.75%	1.6461s
Design 2.b	4	6 yr	2	1	1.08%	1.3643s

6.4 Sensitivity-based localized fixing results

Table 4 shows results from the sensitivity-base localized fixing scheme. In *Design 1.c* example, the predicted lifetime of the power grid network is 9 years. This gird has 3 mortal wires initially and 2 predicted IR drop violations at T_{target}. After finding the violations and using the sensitivity information from *GridNet*, we find that all the 3 branches with void nucleations have to be widened. It turns out that just one iteration, the modified network meets the 10 year lifetime target. This result is also verified by the simulation results from *EMspice*. *Design 1.d* is a power grid with 6 mortal wires and its predicted lifetime is 7 years. At T_{target}, there are 13 IR drop violations and the minimum voltage is 0.9435V. In the first iteration, 2 branches are widened according to Eq.(5). Afterwards, the minimum voltage is increased to 0.9442V and the number of violations is reduced to 8. Then the second iteration is performed, after which only 3 violations left. Finally the third iteration leads to a minimum voltage of 0.9452V. During the iterations, 5 branches are widened in total.

Table 4: Results of sensitivity-based localized fixing

circuit	# mortal wires	# violations at T_{target}	# iter	# modified branches	area increase	total time
Design 1.c	3	2	1	3	0.446%	1.62s
Design 1.d	6	13	3	5	0.765%	3.91s
Design 2.c	4	3	1	2	0.151%	1.07s
Design 2.d	7	9	2	6	0.352%	1.86s

According to the results in Table 4, the sensitivity-based localized fixing method is very efficient in fixing the IR drop violations in localized style. Since this method enables localized branch fixing rather than whole interconnect modification, it keeps most branches unchanged, thus is more suitable to perform in the IR and EM signoff stages of physical design flow. Compared with Table 3, we can see that sensitivity based method leads to less area overhead compared to the first IR drop fixing method as we can select most profitable segments to size.

On the other hand, due to the maximum allowable power routing space and other design rule constraints, IR drop reduction can be achieved by modifying only the branches with void nucleations or the branches close to the wires with void nucleations. As a result, more expensive global wire fixing or optimization method may still be needed.

7 CONCLUSION

In this paper, we have proposed *GridNet*, a fast data-driven EM-induced IR drop analysis framework for power grid networks based on the CGAN model. It is able to speed up the incremental full-chip EM-induced IR drop analysis in sensitivity-based optimization and IR drop violation fixing during the power grid design and optimization. We demonstrated that the *GridNet* can be adopted to learn temporal dynamics in the aging process of power grid networks by using the continuous time as one of the conditions. Numerical results on a number of synthesized power grid networks validated that the new method can lead to five orders of magnitudes speedup over recently proposed full-chip coupled EM and IR drop analysis tool. More importantly, by leveraging the differentiable feature of the *GridNet* model, we can easily obtain the sensitivity information of node voltage with respect to the wire resistance (or width). We then demonstrated two efficient localized strategies to fix IR drop violations for late stage power grid designs. Numerical results showed that the localized IR drop violation fixing is remarkably fast by utilizing the sensitivity information from *GridNet*.

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