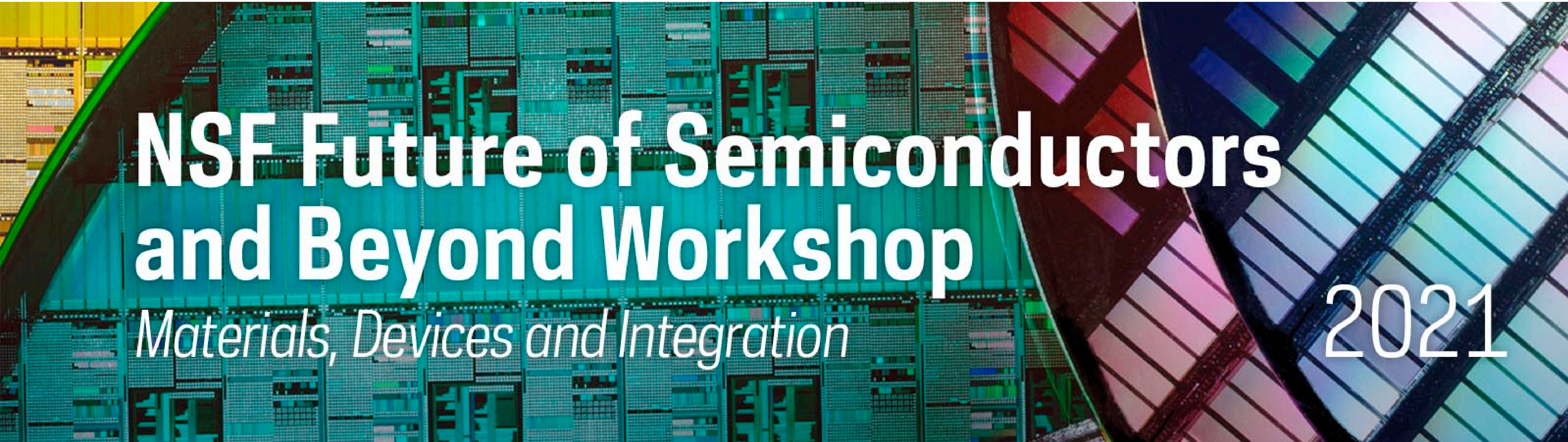
New Strategies in Nanoelectronic 3D Heterogeneous Integration

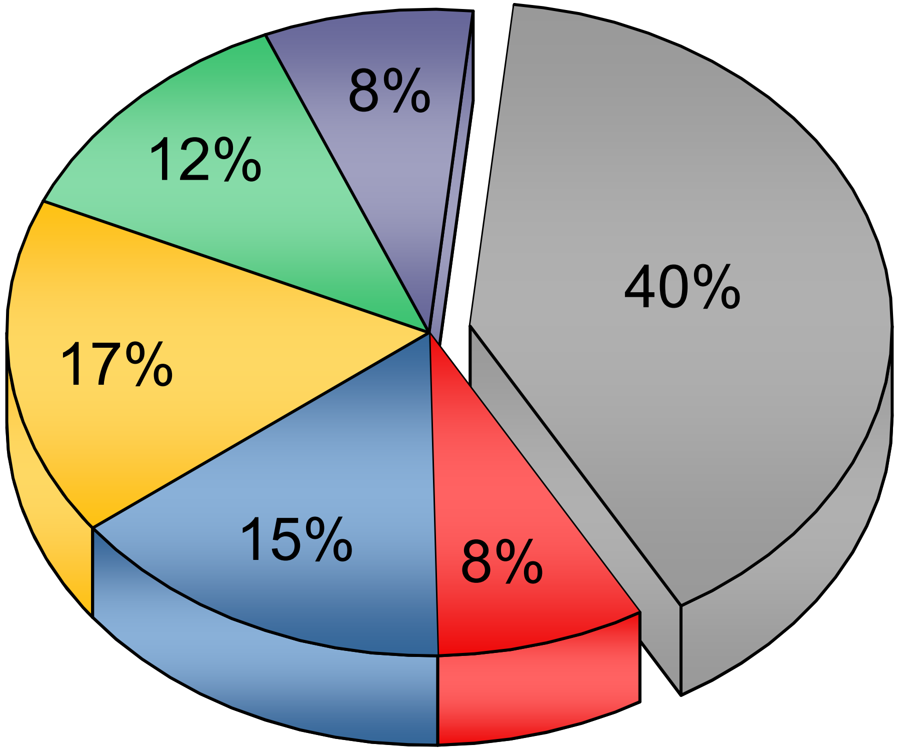
Prof. Chris Hinkle
University of Notre Dame



Compute performance gain comes from ……

Compilers
Power Management
Microarchitecture

- ❖ Software Advancement
- ❖ Integration of system components
- ❖ Architectural Efficiency



Process Technology

- ❖ Higher performance, denser logic transistors
- ❖ Back-end-of-line RC reduction

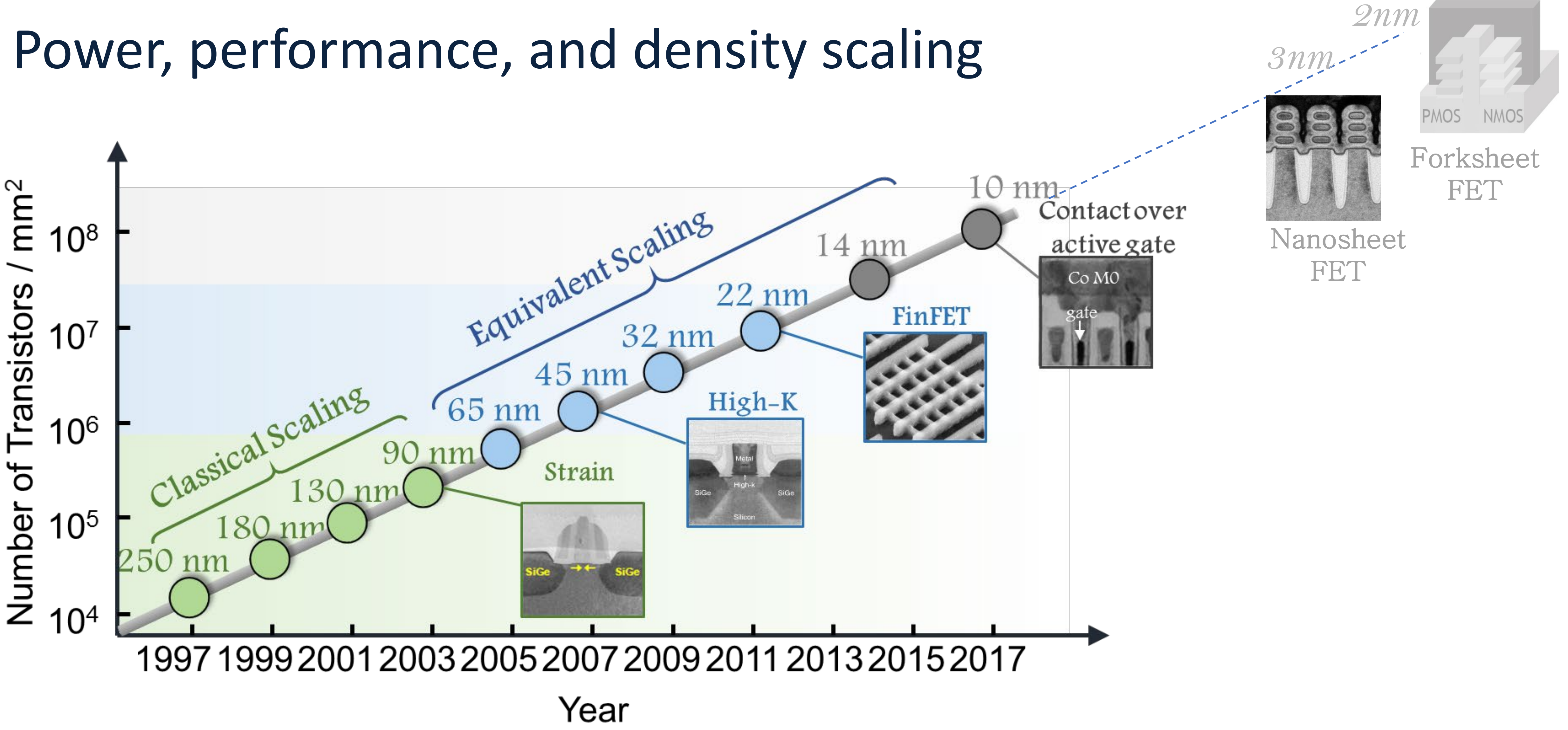
Additional Die Size
Additional TDP

- ❖ Bigger Die
- ❖ Increased thermal design point

60% of compute performance gain over last decade came from semiconductor innovation

Source: Lisa Su (AMD), ERI DARPA Summit, 2019

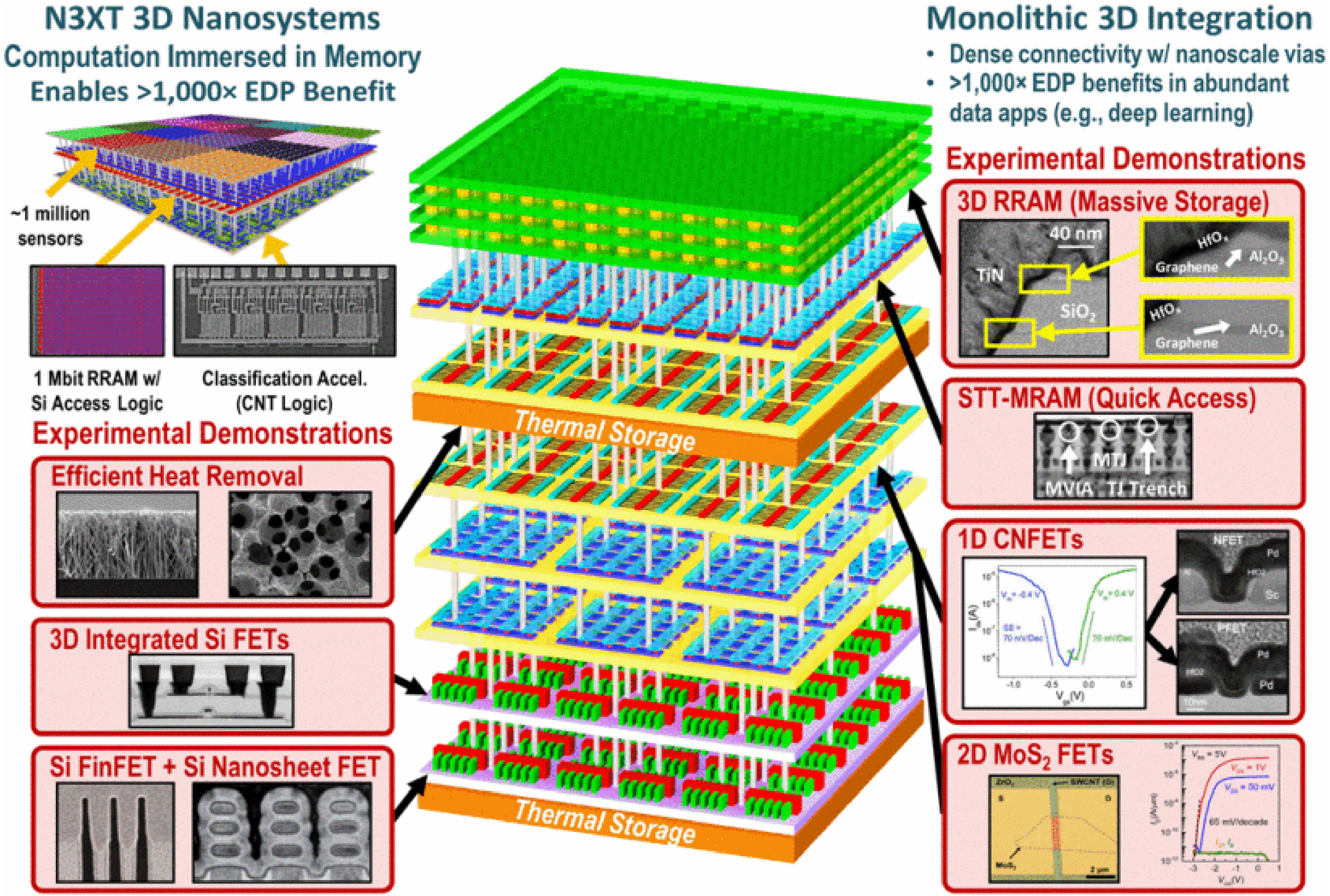
Power, performance, and density scaling



Transistor density scaling continues enabled by materials, device and process innovation
Backend wiring RC delay improvements with new metals and liners

S. Salahuddin, K. Ni and S. Datta, "The era of hyper-scaling in electronics," Nature Electronics, 2018

3D compute-memory integration



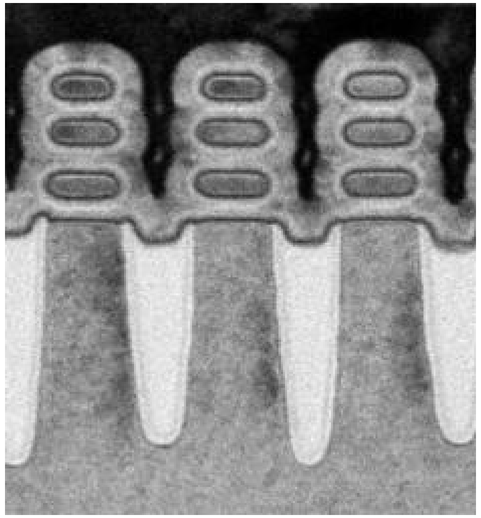
Hwang, Wan, Mitra, Wong
IEEE International Symposium on Circuits and Systems (ISCAS), 978 (2018)

Massive system-level EDP improvement. Enables compute-in-memory, neuromorphic, dynamical systems.

Challenges to overcome

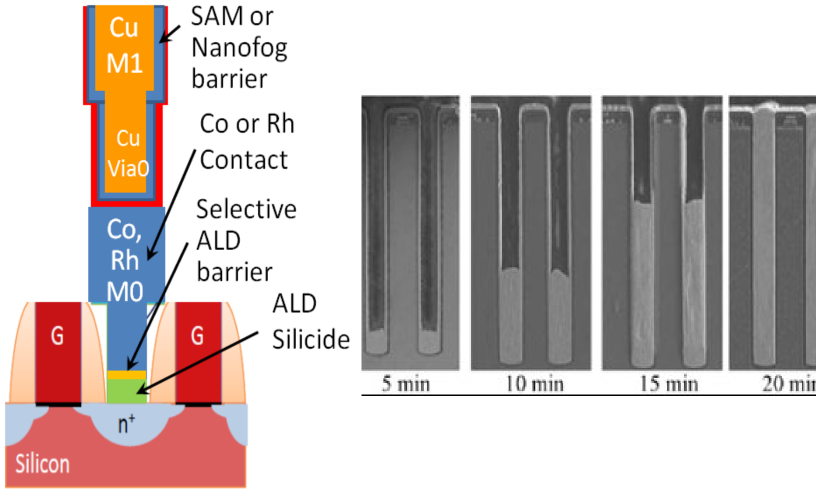
- Low Thermal Budget for Deposition and Processing
- Interface with dissimilar materials
- Non-ideal deposition surfaces
- Challenging geometries
- Selectivity
- Scalability

  - Grain boundary / Bulk / Interface Defects
  - Degraded Transport
  - Dopant incorporation/activation
  - Contact resistance



Nanosheet FET

Self-aligned Contacts & Vias



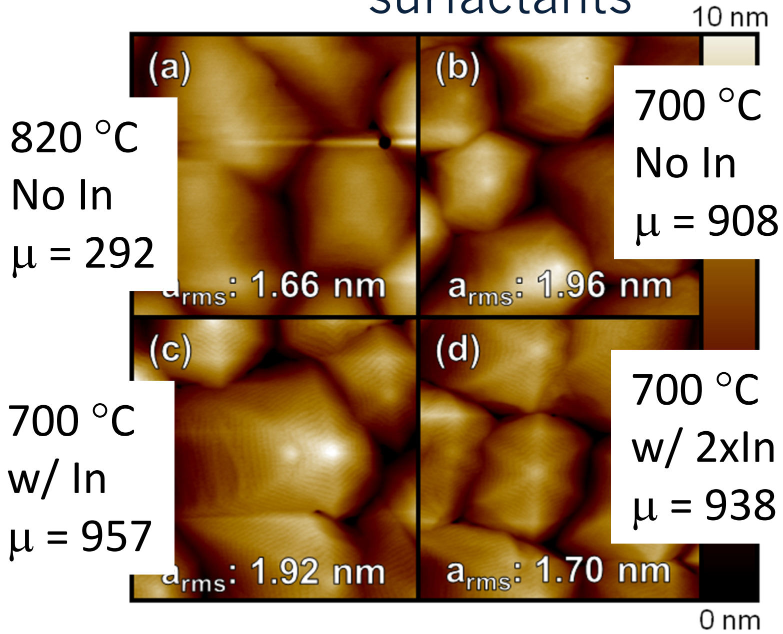
- Hyper Selective ALD of silicide
- Hyper-Selective Co (and Ru) ALD

Kummel (UC-San Diego), George (Colorado)

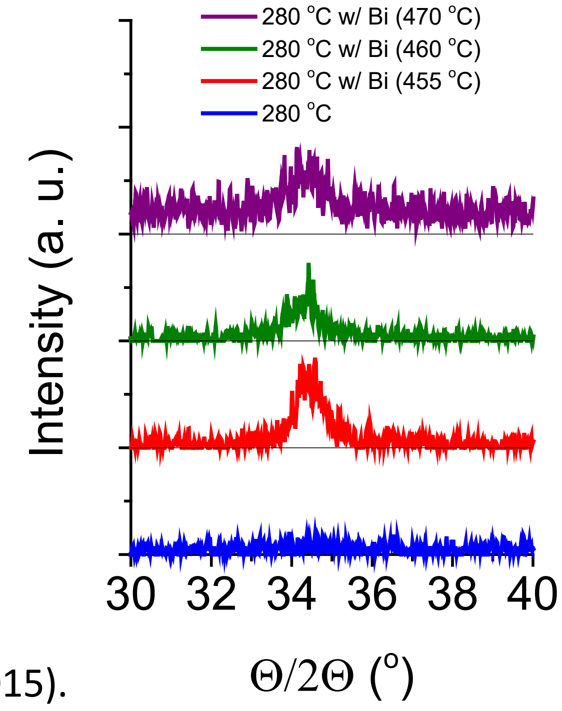
Crystalline semiconductors at BEOL temps

GaN

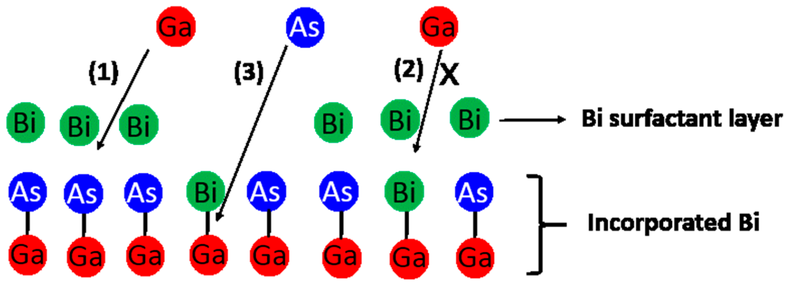
Aggressive use of surfactants



Kaun, Mishra, Speck, et al., SST 30, 055010 (2015).

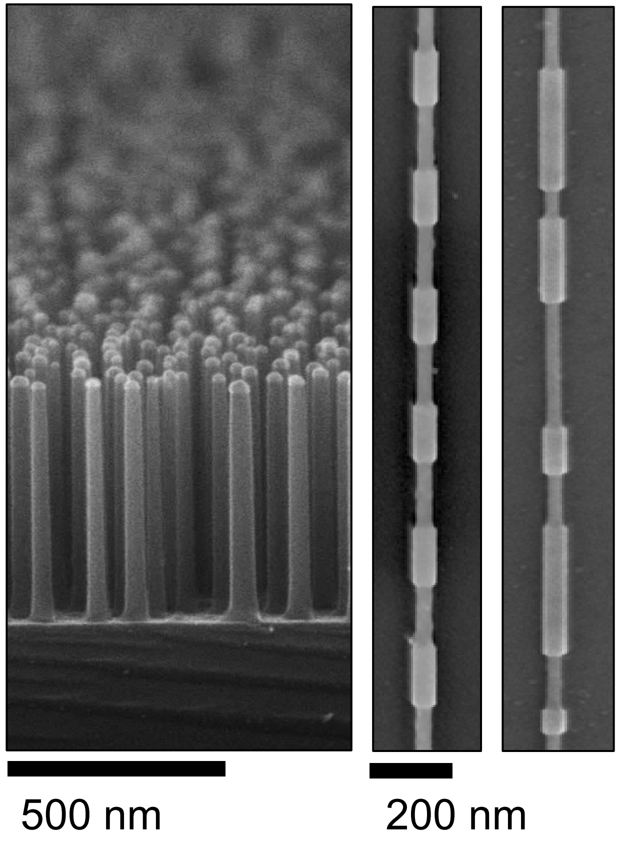


Zhou, Hinkle
Notre Dame



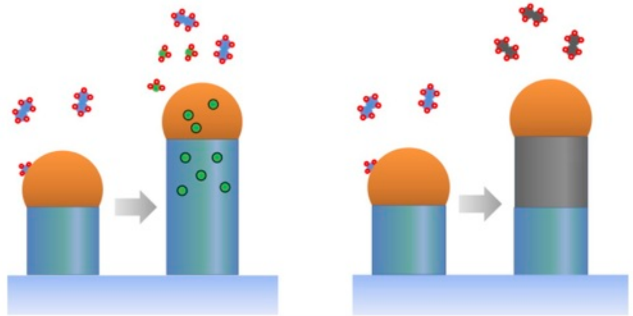
Wang, et al., Crystals 7, 63 (2017).

VLS



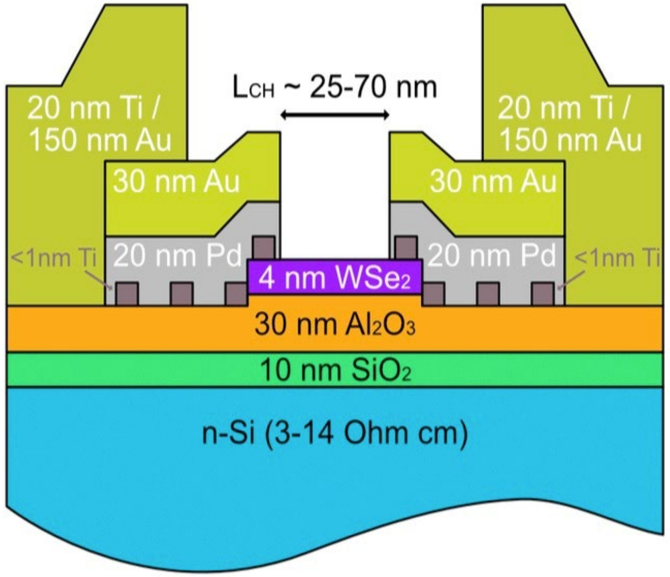
Michael Filler
Ga Tech

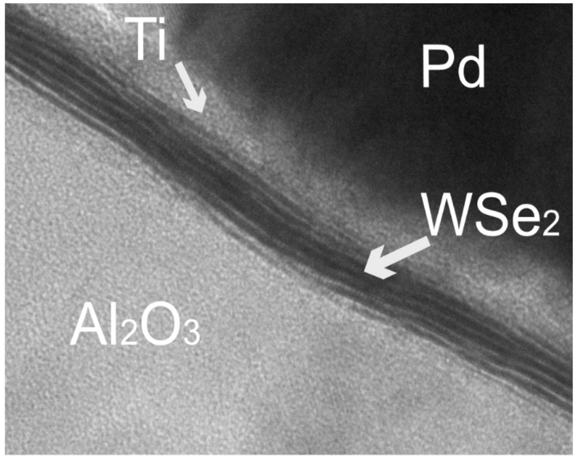
Laser Anneals
Plasma Enhanced Depositions

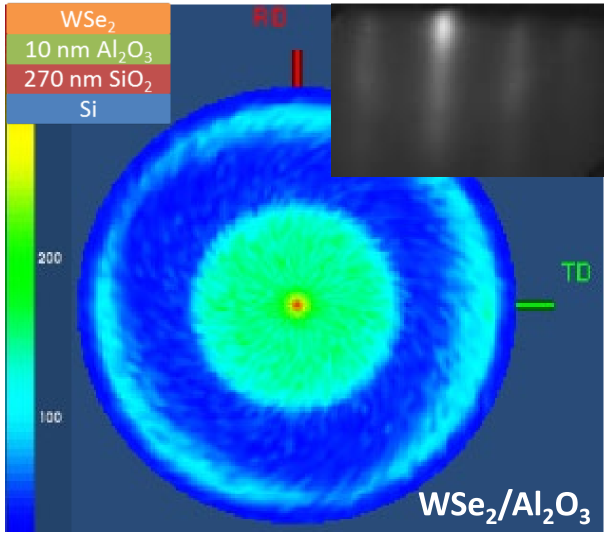


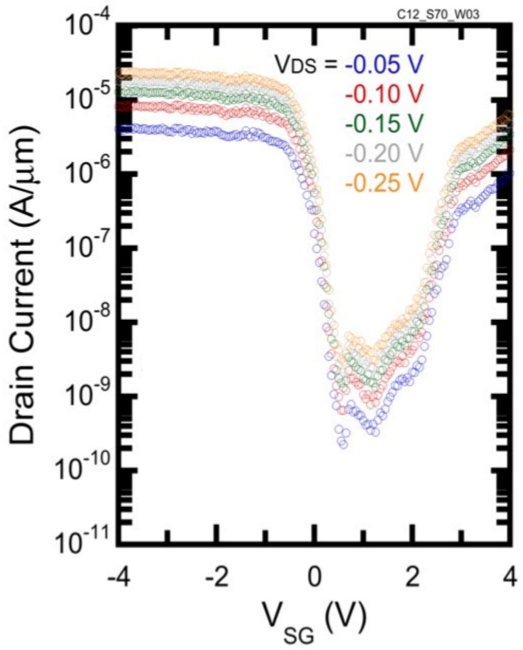
van der Waals materials

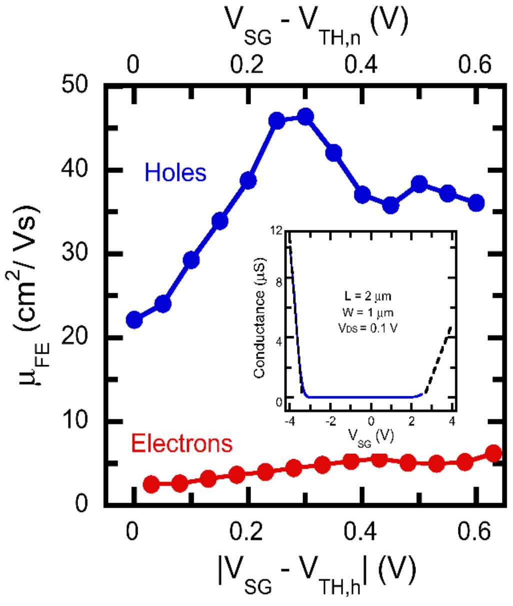
Crystalline WSe_2 on amorphous oxides at 500 °C







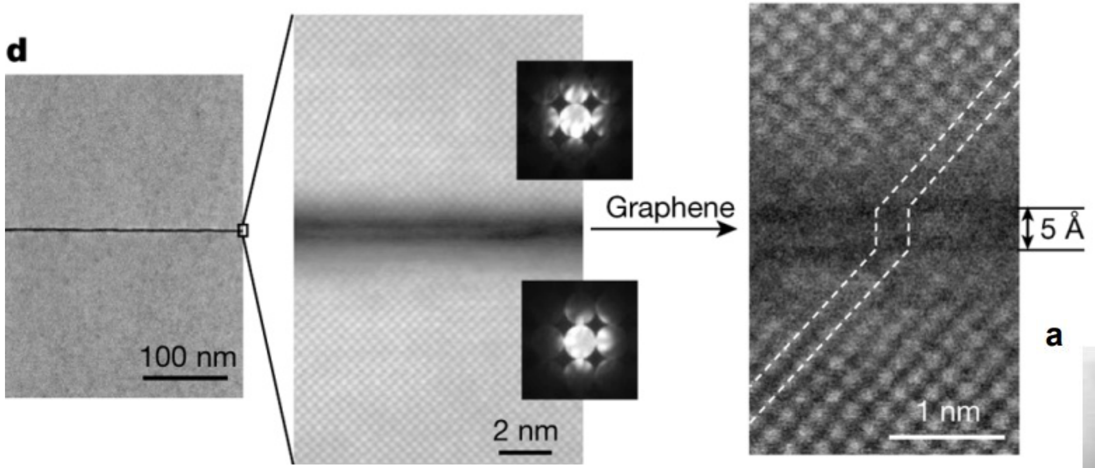




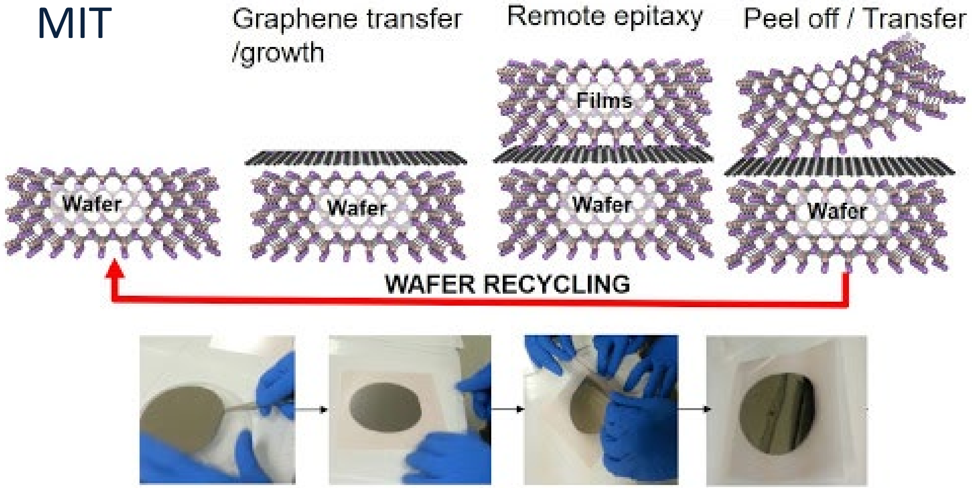
Hinkle and Seabaugh

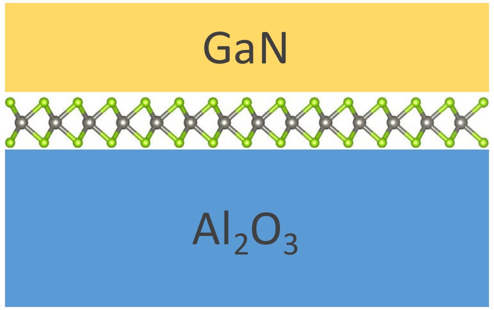
npj 2D Materials and Applications 3, 2019

3D semiconductors grown on 2D materials



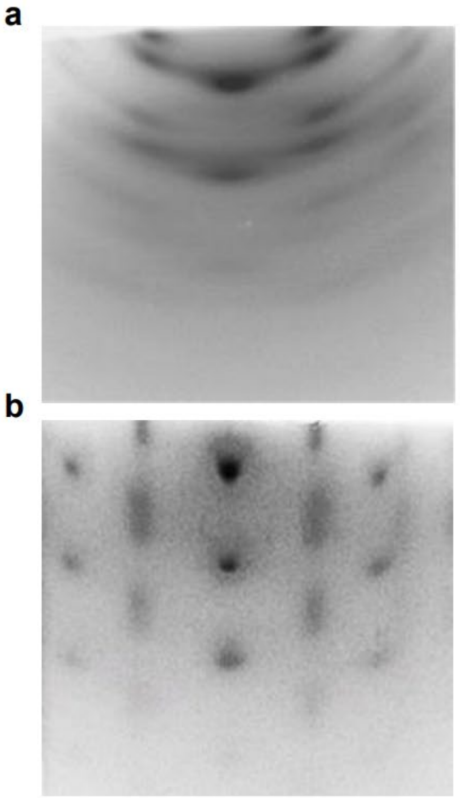
Jeehwan Kim
MIT

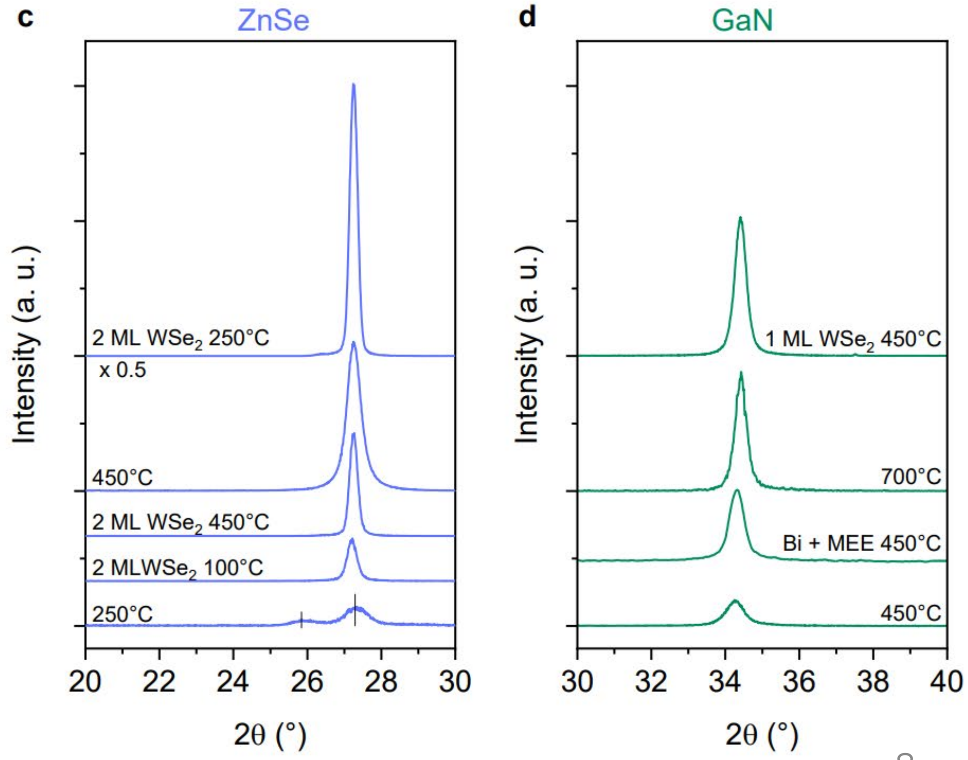




Equivalent to ~250 °C thermal budget gain

Hinkle
Notre Dame





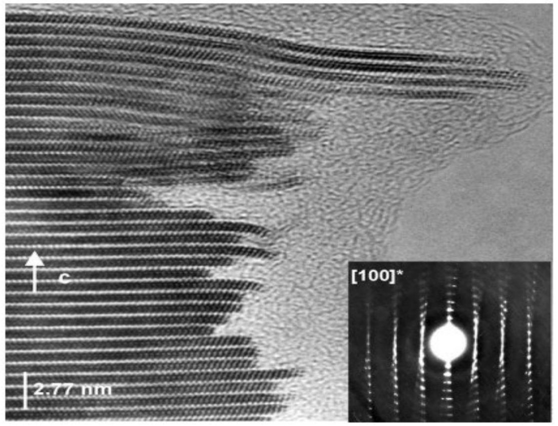
Y Kim *et al.* *Nature* **544,** 340–343 (2017) doi:10.1038/nature22053

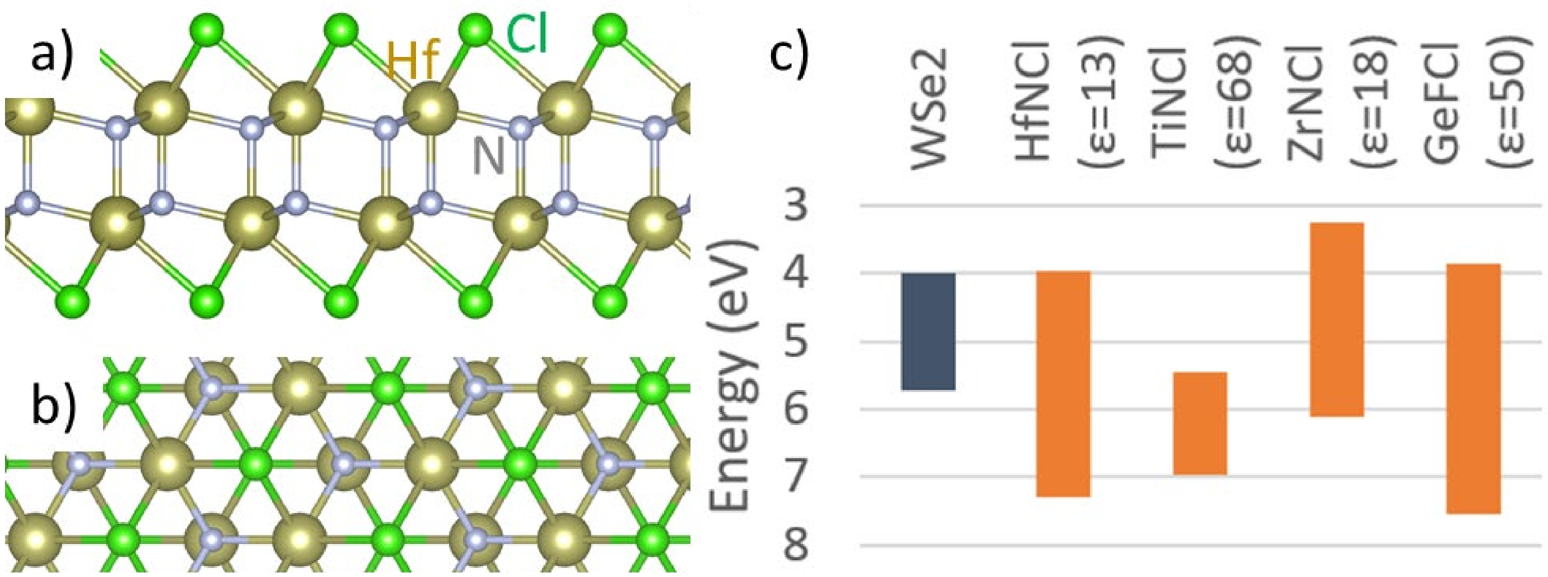
New 2D insulators

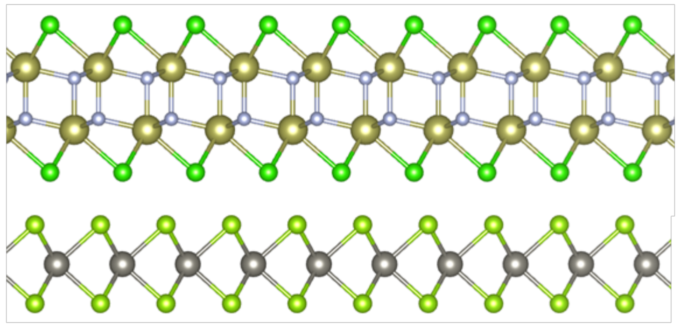
- Layered dielectrics with large dielectric constants and band offsets

HfNCl, ZrNCl, HfNF, ZrNF, GeClF, SiClF

J. Oró-Solé et al. / Materials Research Bulletin 41 (2006) 934–940







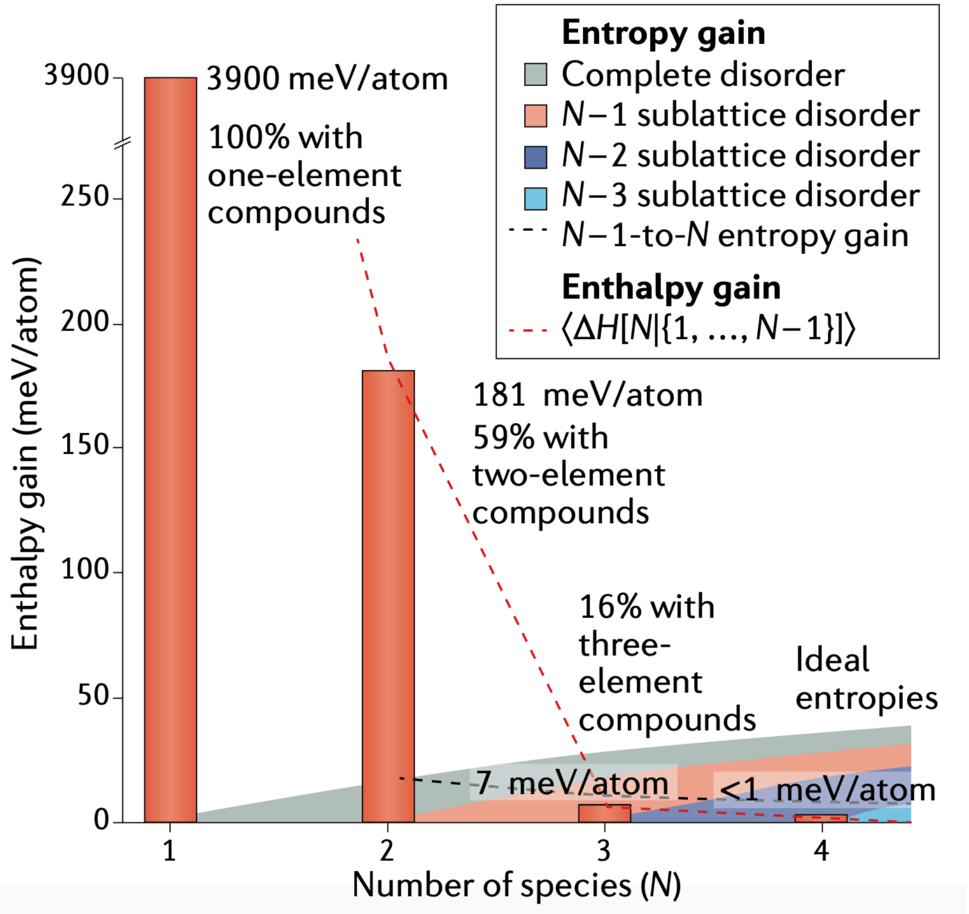
HfNCl

WSe_2

Entropy for new materials synthesis and discovery

$\Delta G = \Delta H - T\Delta S$ $\Delta S = -k_b \sum_i x_i \ln x_i$

John Heron (Michigan)
Jon-Paul Maria (Penn St)

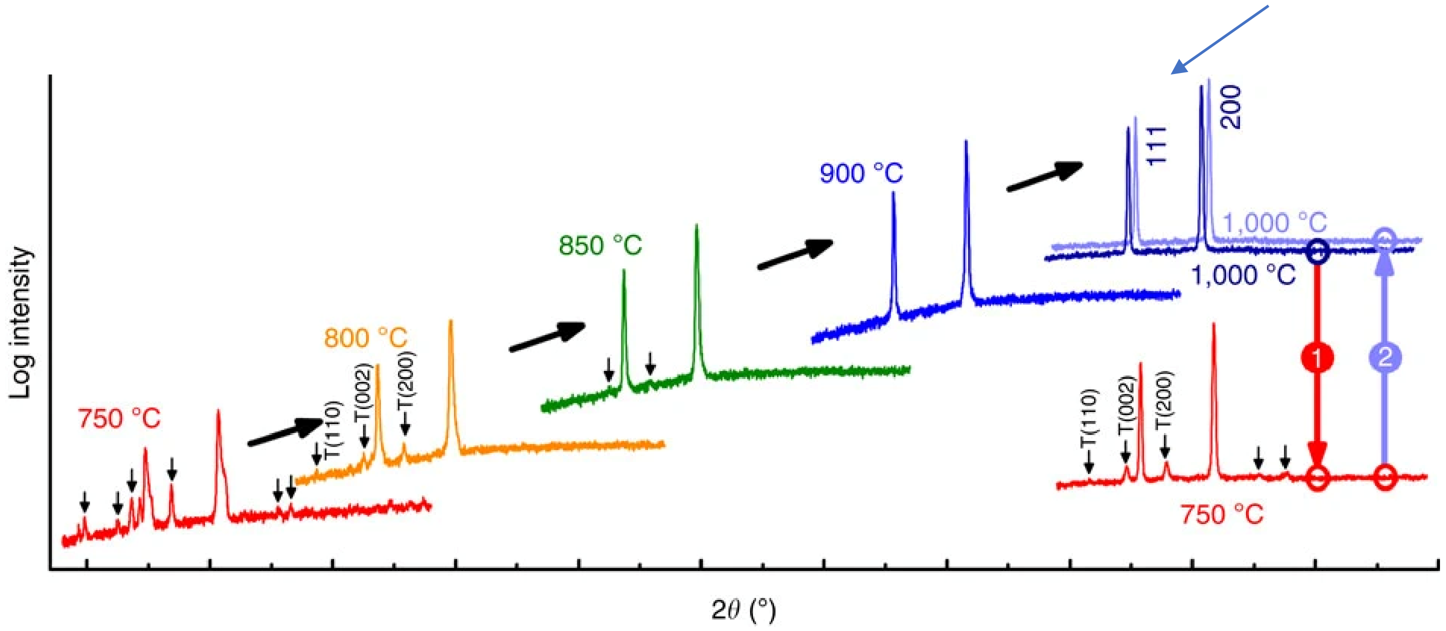


Oses *et al.*, Nature Rev. Mater. **7**, 13344 (2017)

Enthalpy gain (Δ**H**) decays with *N* and asymptotes while entropy gain (Δ**S**) scales as ln *N* (equimolar) leading to a cross over.

Entropy-stabilized oxides realized in 2015

Single phase (MgCoNiCuZn)O



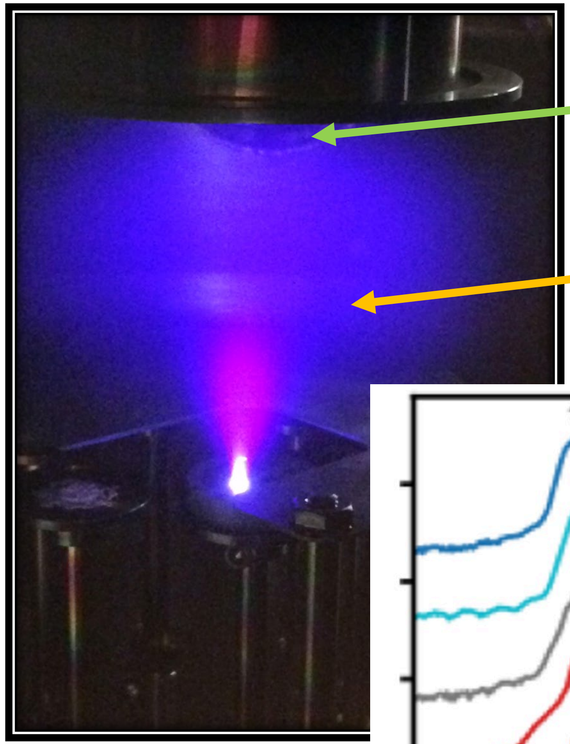
Stable at room temperature through quenching

Rost *et al.*, Nature Comm. **6**, 8485 (2015)

Entropy for new materials synthesis and discovery

$$G = H - TS \qquad S = -k_b \sum_i x_i \ln x_i$$

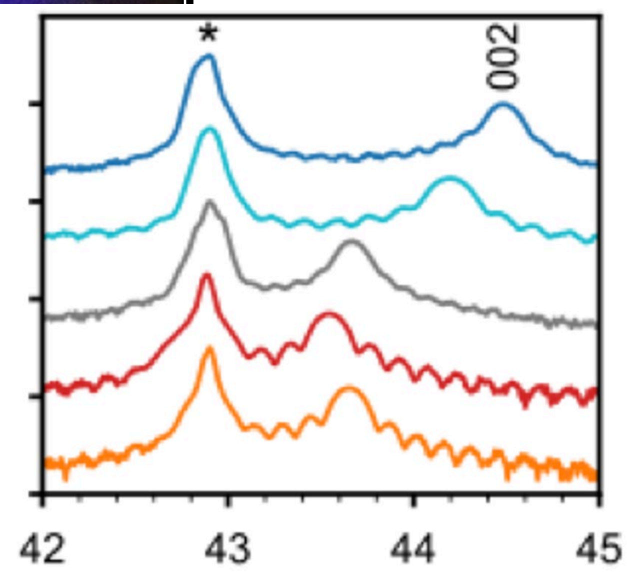
BEOL compatibility



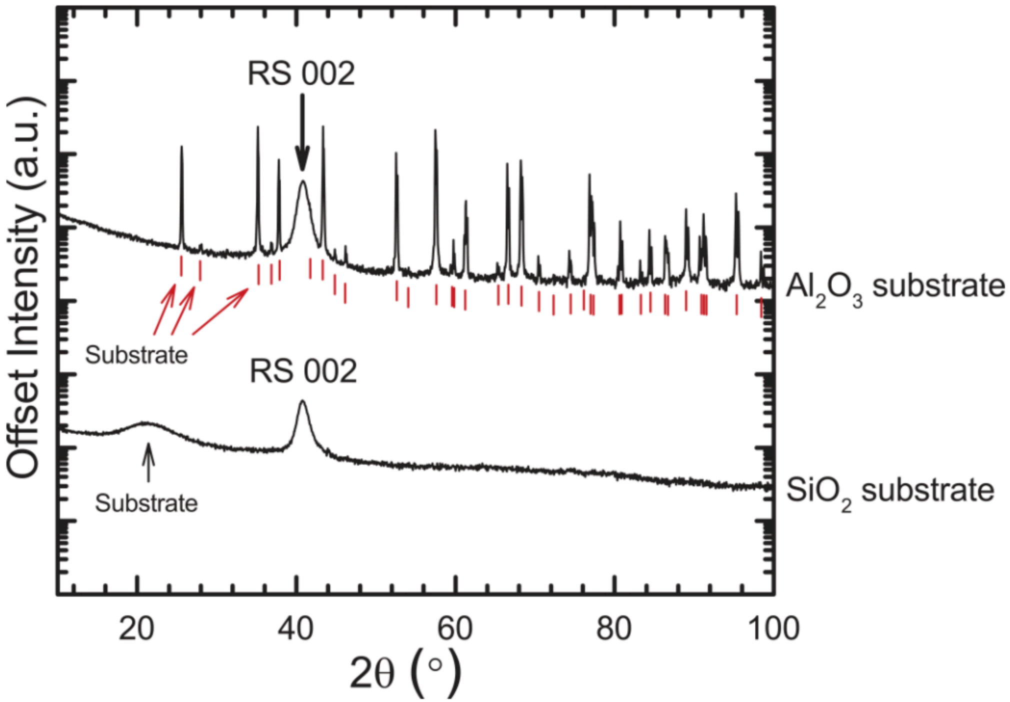
T_{sub} < 300 °C

T_{flux} > 10^3 °C

Growths at 250 C



Synthesis favors PVD deposition with inherent large effective quenches



Synthesis shows substrate diversity – stabilized on crystalline and amorphous substrates

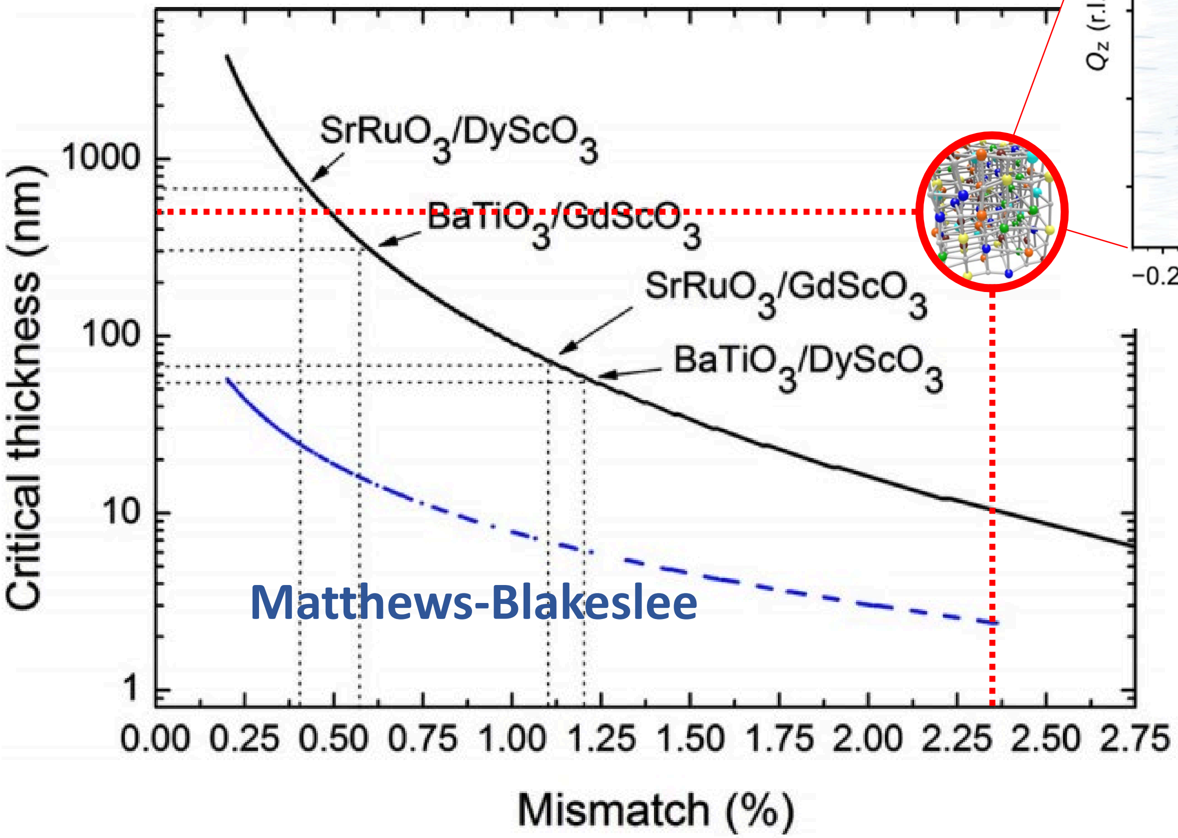
Thermal stability of (MgCoNiCuZn)O at least to 1000 °C at 50 mTorr

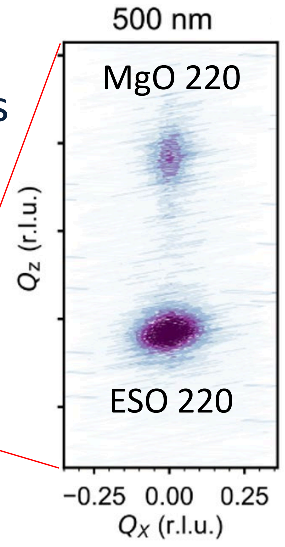
Meisenheimer *et al.*, Sci. Rep. **7**, 13344 (2017)
Kotsonis *et al.*, Phys. Rev. Materials **3**, 104420, (2020)

Anomalous structural behavior

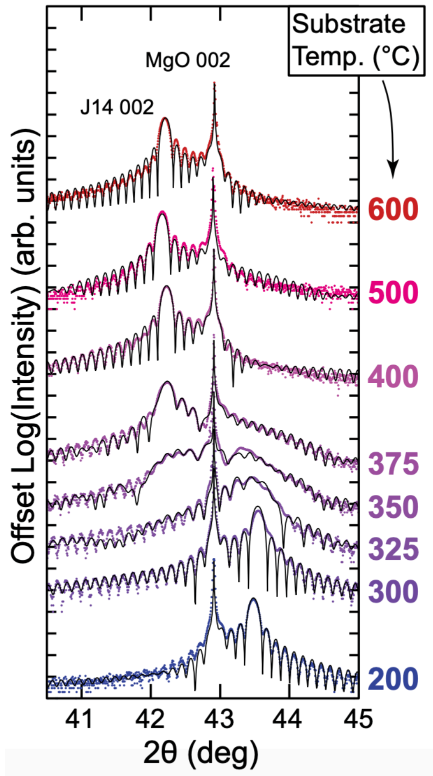
Potential Mitigation of Misfit Dislocations

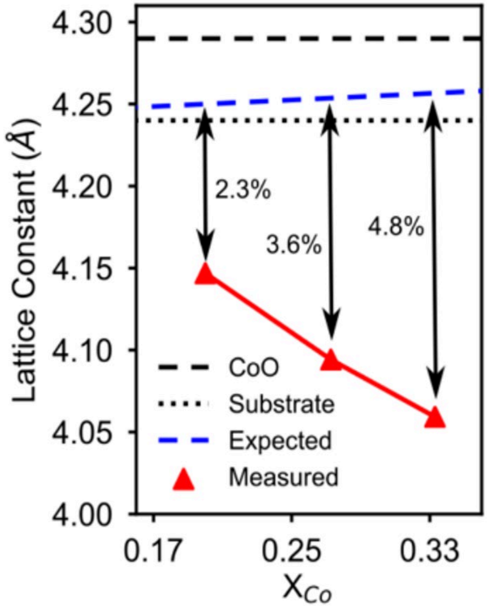
Low temperature ESO (MgCoNiCuZn)O rocksalt films still coherent at 500 nm

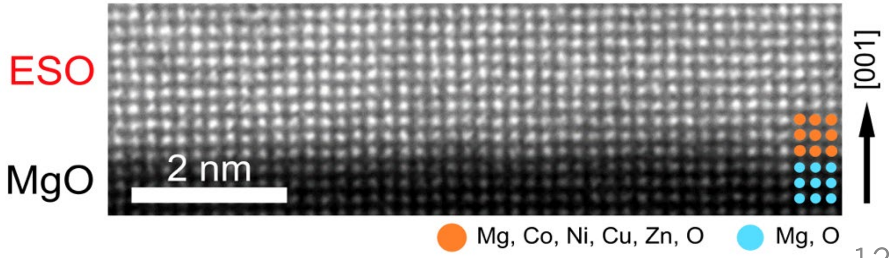




Large tunability with composition and deposition parameters while maintaining high crystallinity

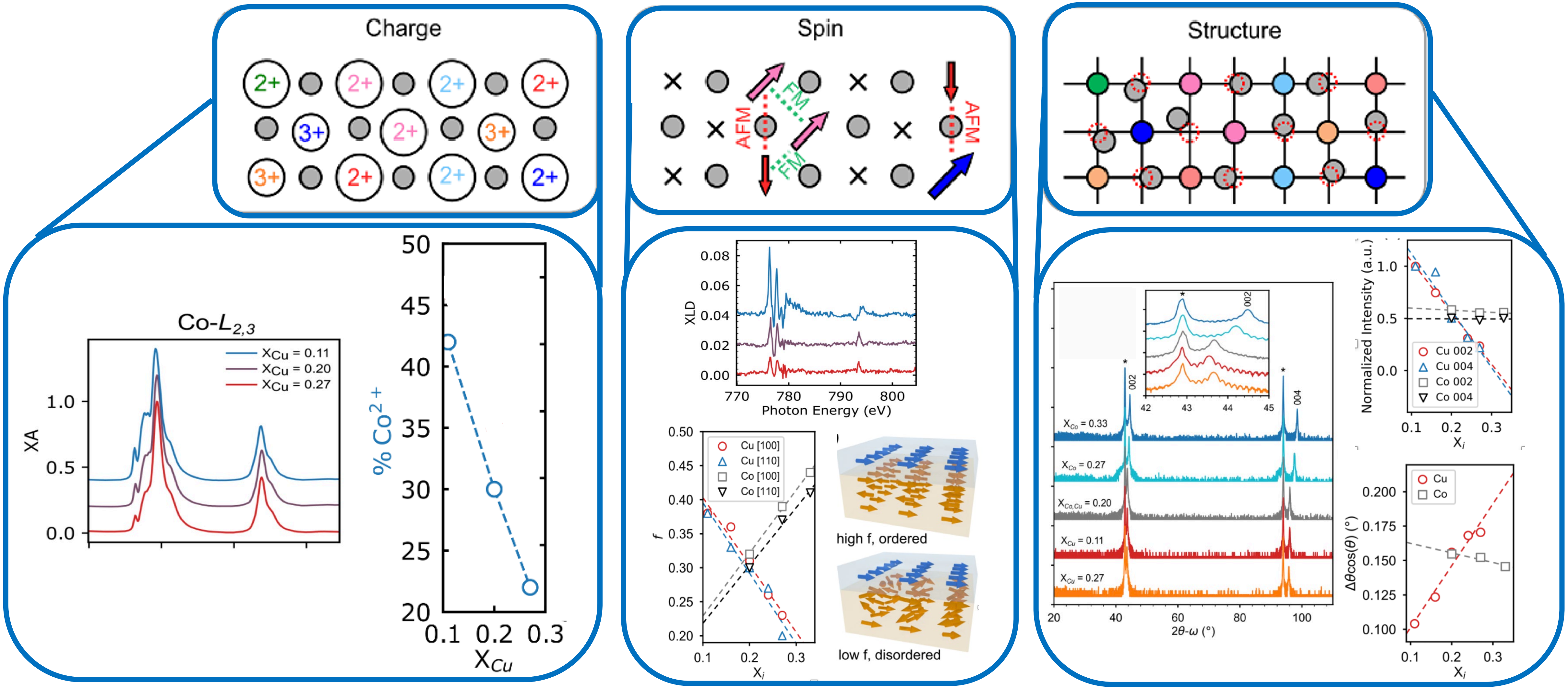






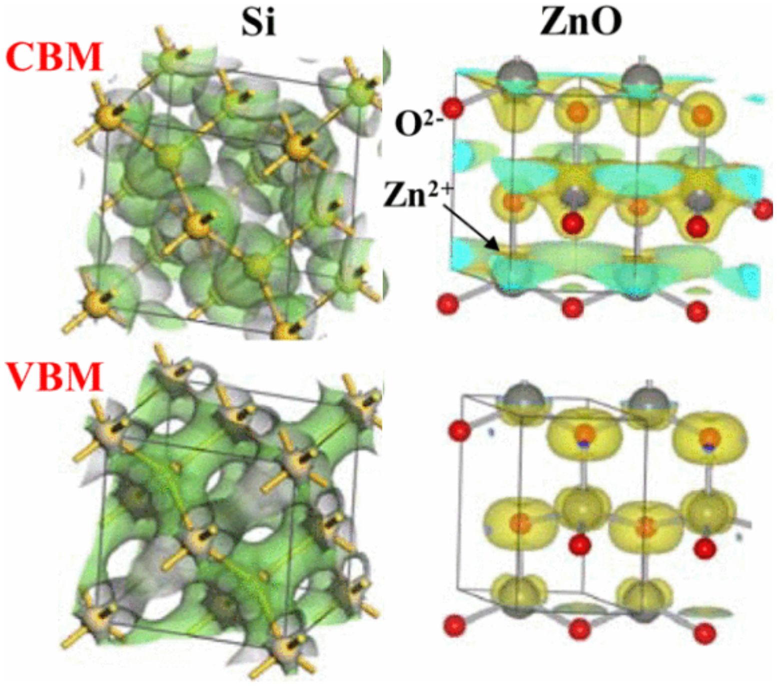
Chen *et al.*, Appl. Phys. Lett. **91**, 252906 2007; Meisenheimer *et al.*, Sci. Rep. **7**, 13344 (2017); Meisenheimer *et al.*, Phys. Rev. Materials **3**, 104420 (2019); Kotsonis *et al.*, Phys. Rev. Materials **3**, 104420, (2020)

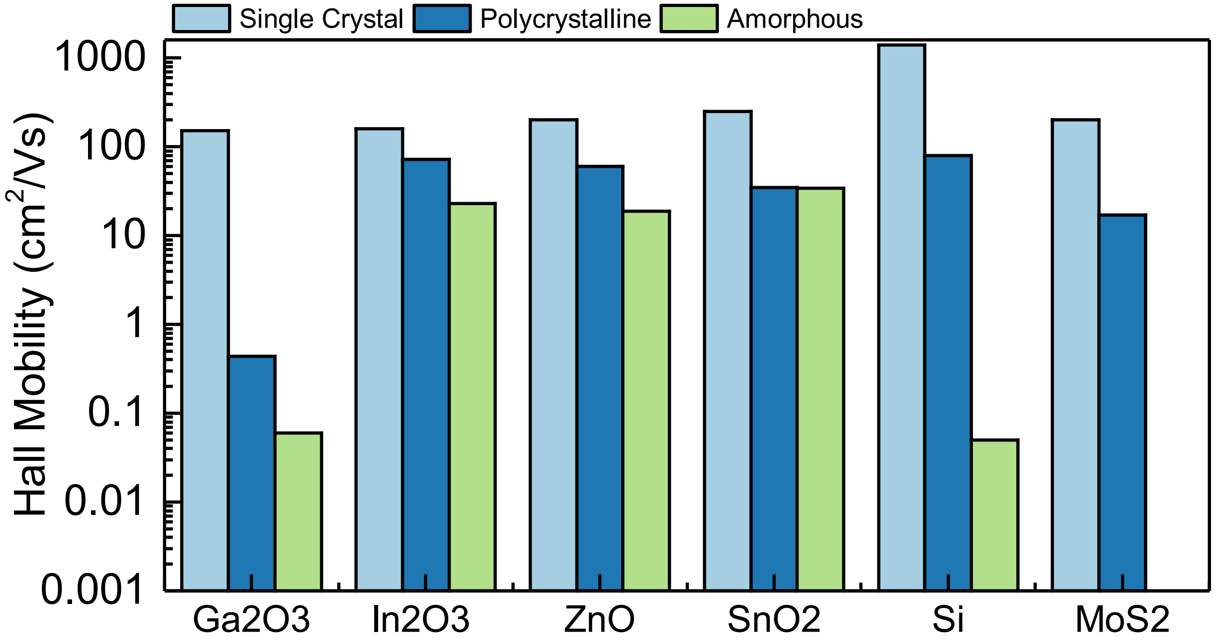
New configurations and interplay for emergent functions



Meisenheimer *et al.*, Phys. Rev. Materials **3**, 104420 (2019)
Kotsonis *et al.*, Phys. Rev. Materials **3**, 104420, (2020)

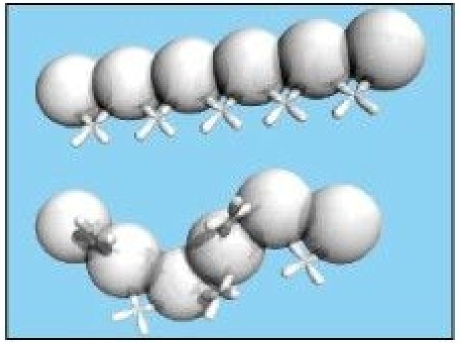
Amorphous semiconductors: transition metal oxides





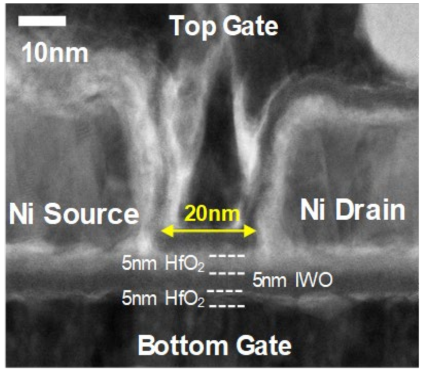
Kamiya, Nomura. J Dis Tech 2009

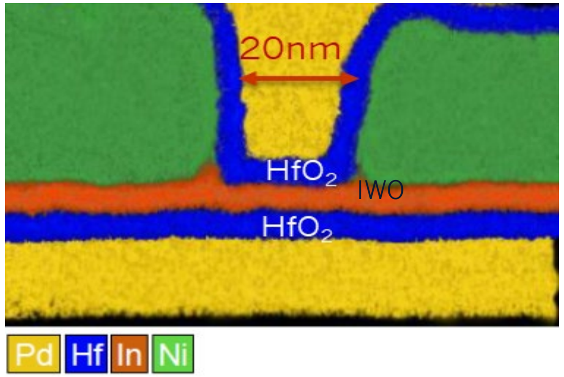
- Covalent Semiconductor (e.g. Si): CBM & VBM arise from sp^3 hybridized orbi
- Ionic TMO (e.g. ZnO, In_2O_3, SnO_2): CBM from empty s-orbitals of M catio
  VBM from filled O 2p orbitals

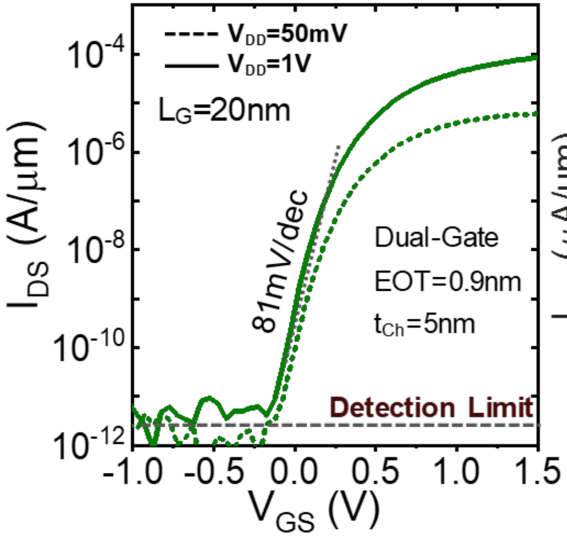


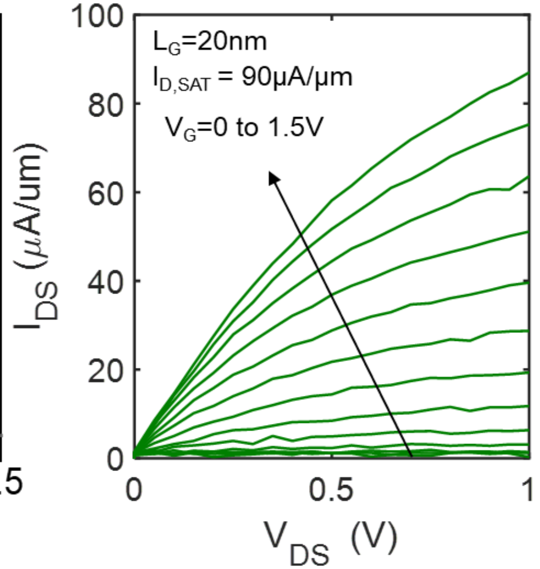
- Crystalline vs amorphous Si:
  Spatially directed sp^3 orbitals causes mobility degradation with disorder
- Crystalline vs amorphous TMO:
  Spherically extended s orbitals are less affected by structural randomness

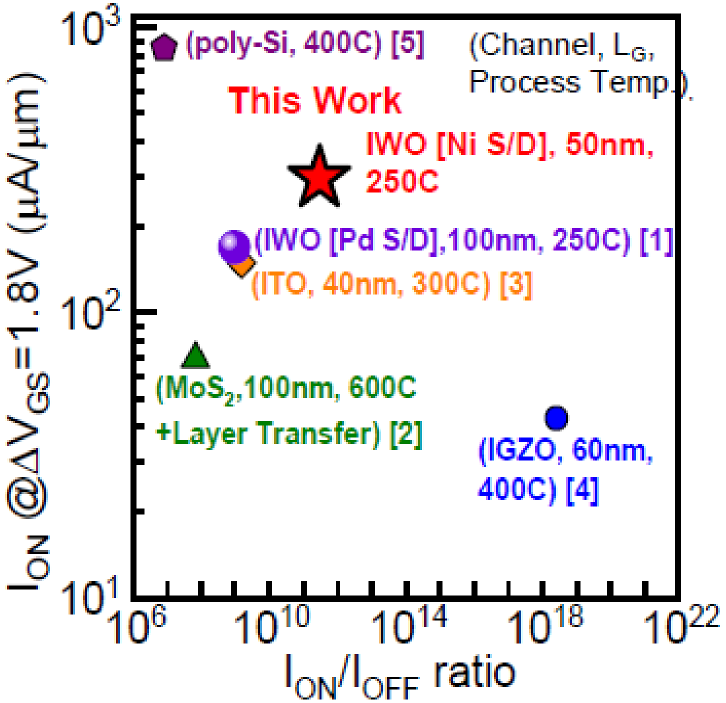
Amorphous W-doped In_2O_3

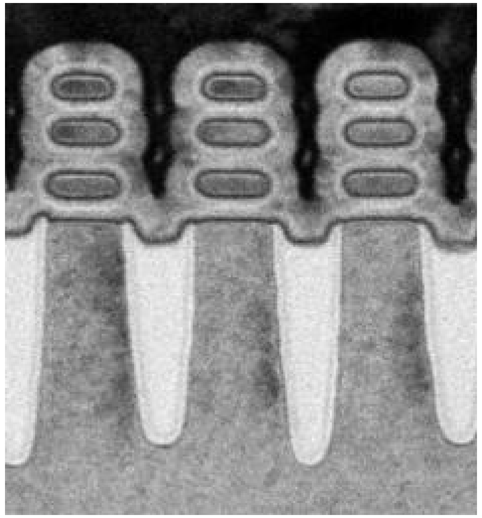












L_G (nm)	SS (mV/dec)	V_{t0} (V)	DIBL (mV/V)	μ_0 (cm^2/V-s)	v_{inj} (cm/s)
50	73	0.55	70	15	1.5×10^6

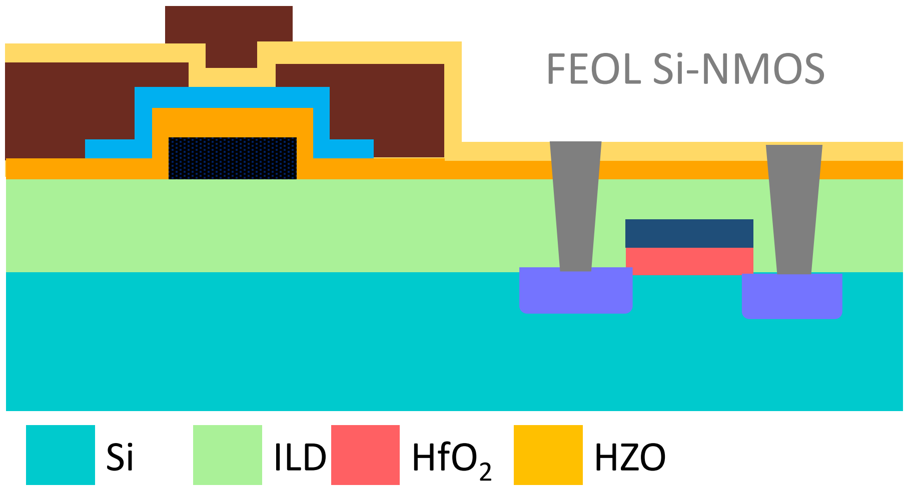
Wriddhi Chakraborty, Huachen Ye, Suman Datta (Notre Dame)

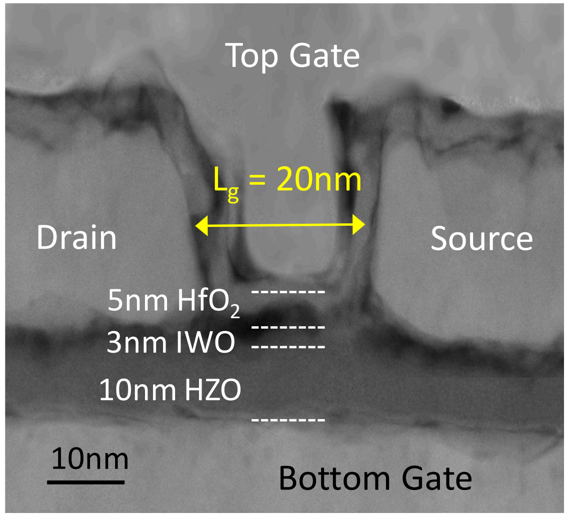
Attoampere leakage transistors processed ***in situ*** *below 250°C for capacitorless 3D DRAM*

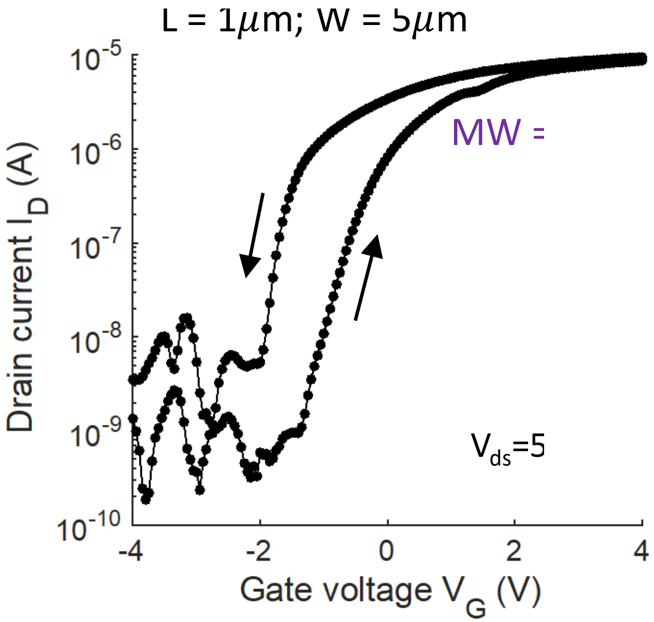
H. Ye et al, Double-Gate W-Doped Amorphous Indium Oxide Transistors for Monolithic 3D Capacitorless Gain Cell eDRAM, IEDM 2020

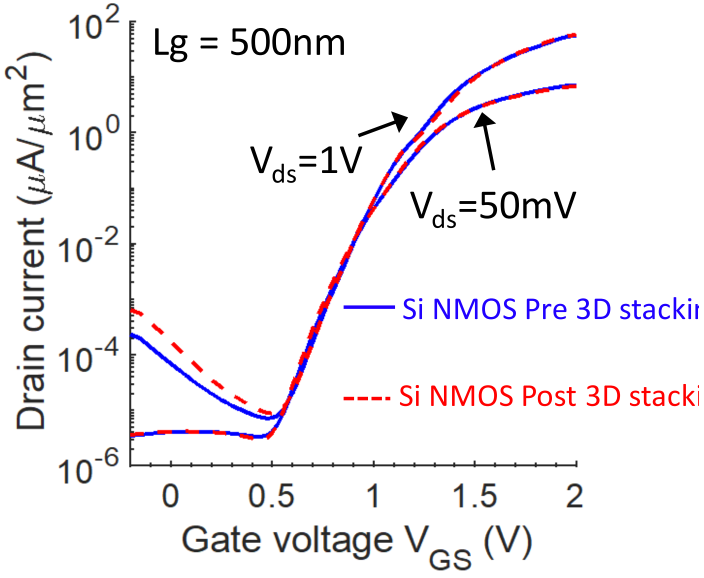
Monolithic 3D integration of BEOL FeFET

Sourav Dutta, Suman Datta (Notre Dame)

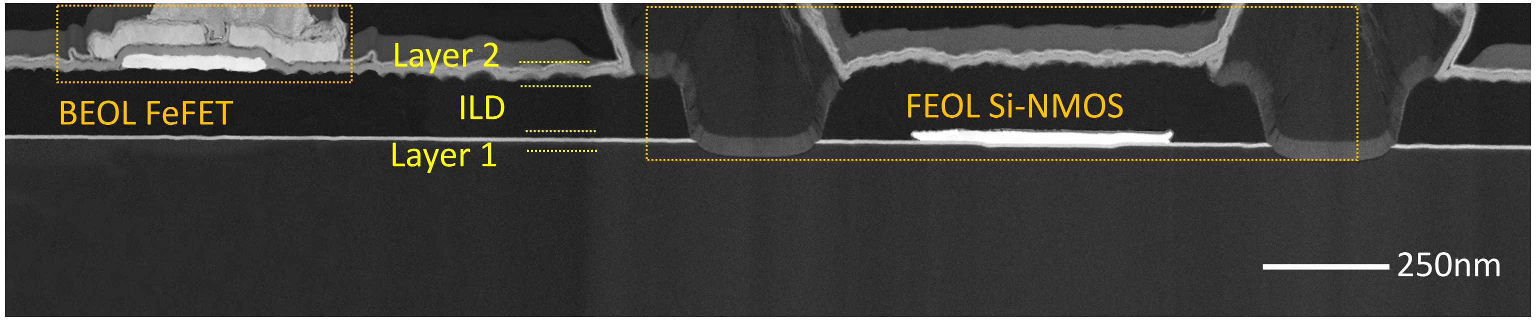








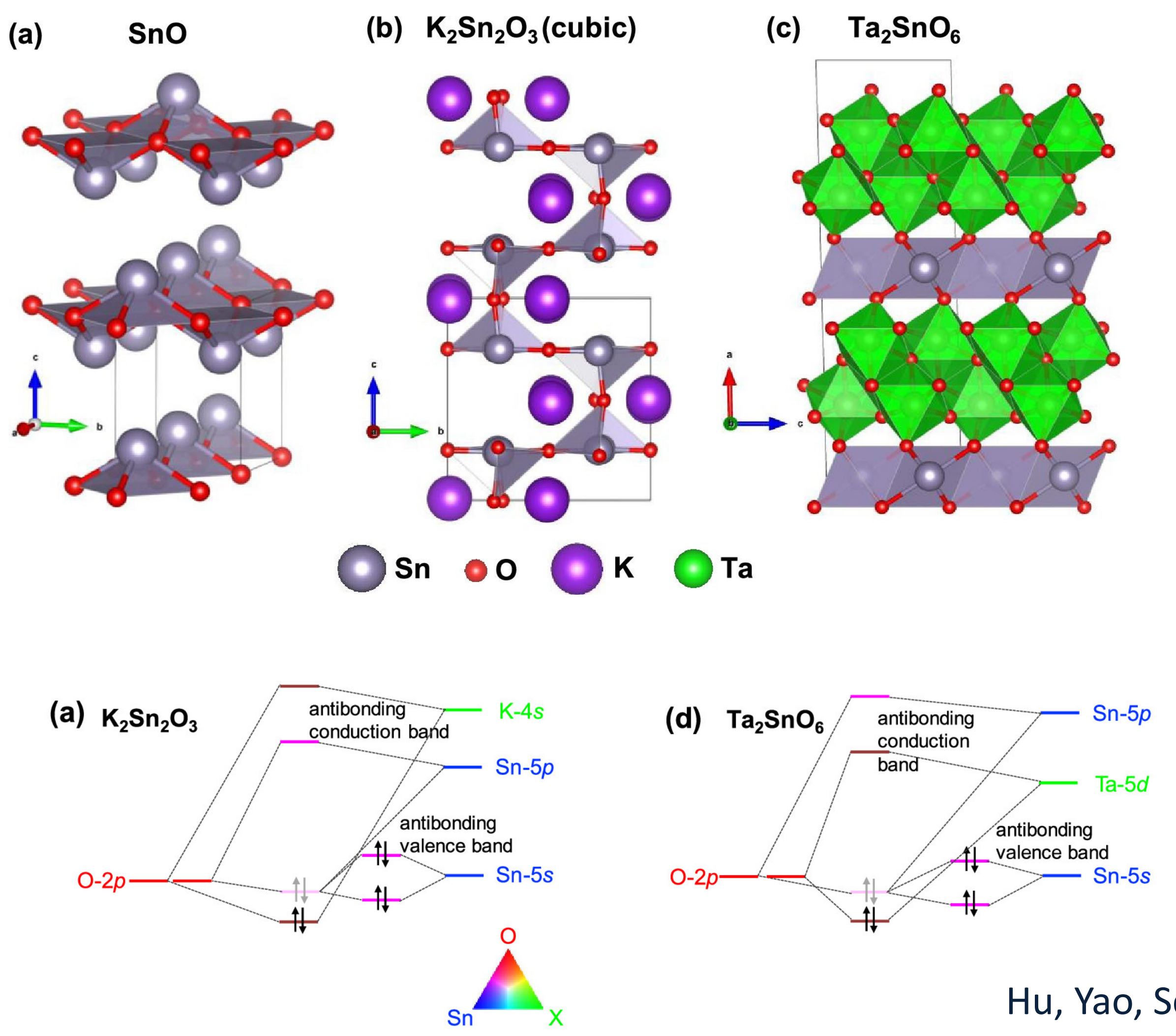
350 °C Processing for BEOL devices

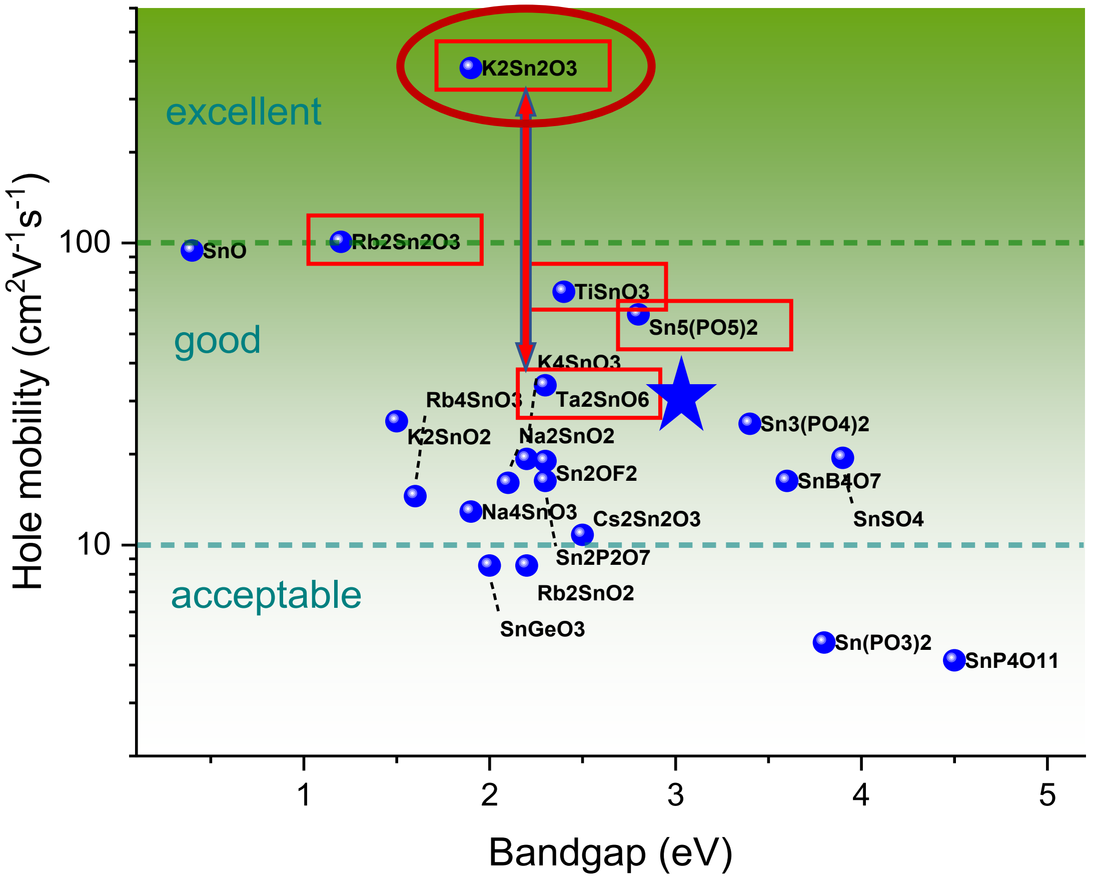


- 2-tier monolithic 3D integrated structure with BEOL FeFET (top layer) and FEOL Si NMOS (bottom layer)

S. Dutta et al, Monolithic 3D Integration of High Endurance Multi-Bit Ferroelectric FET for Accelerating Compute-In-Memory, IEDM 2020

Sn-based amorphous oxides for p-channel

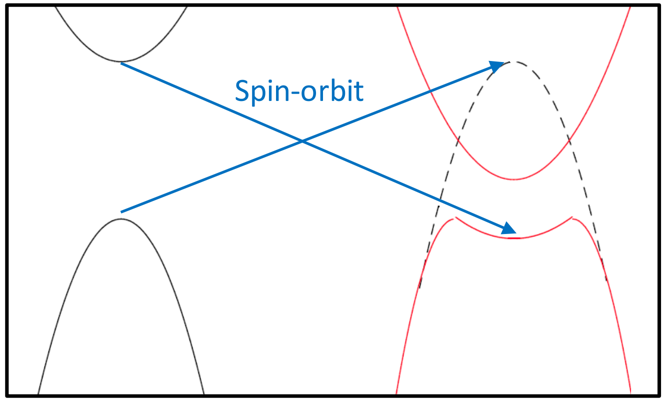




Hu, Yao, Schlom, Datta, and Cho. Chemistry of Materials 33, 212 (2021).

Defect tolerance: topological protection

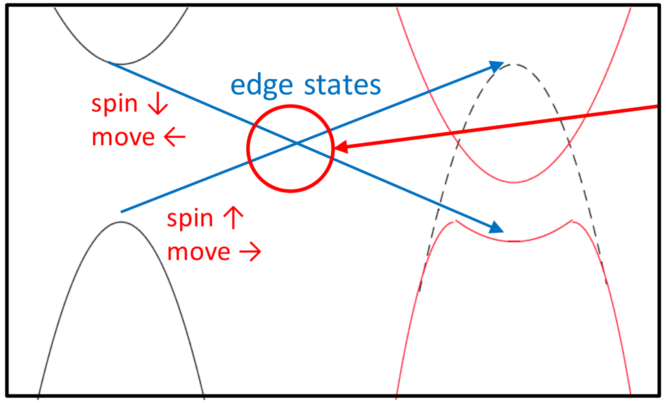
- Insulators with CB and VB “swapped” (*e.g.*, by the spin-orbit interaction)
- Edge states are “protected” by time-invariance; no backwards scattering: **Tolerant to “Imperfections”**



Spin-orbit induces CB and VB swap

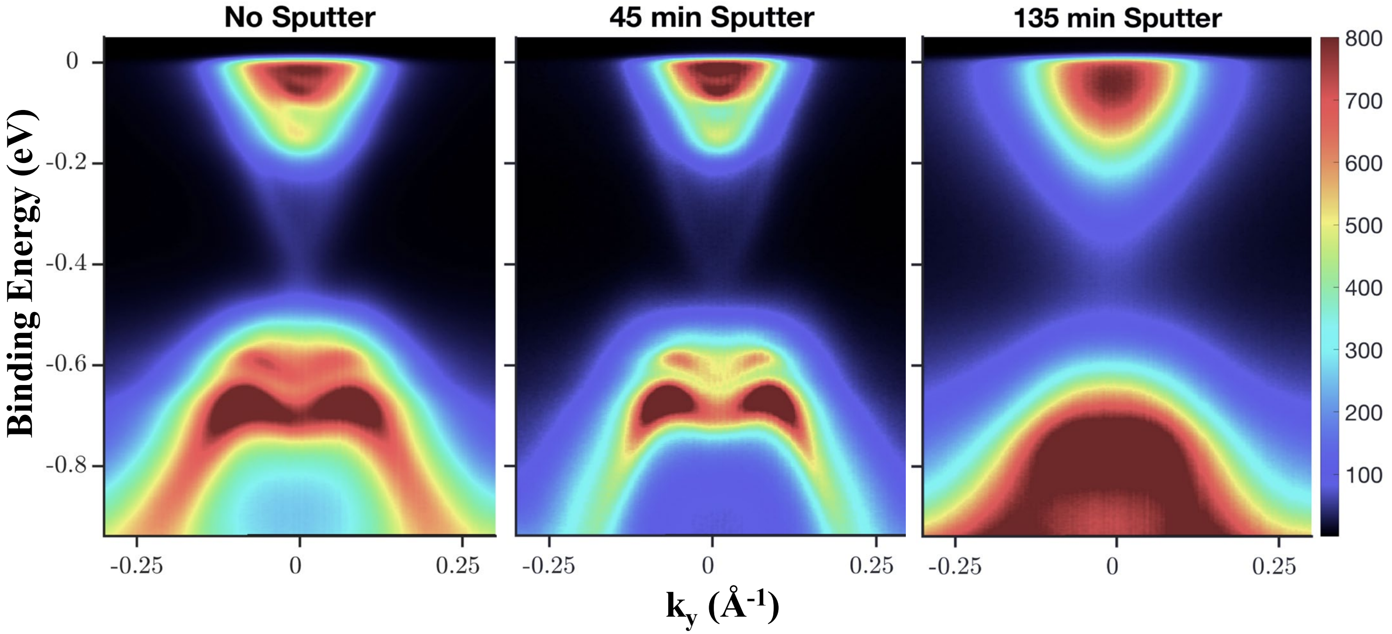
Trivial insulator

Topological insulator

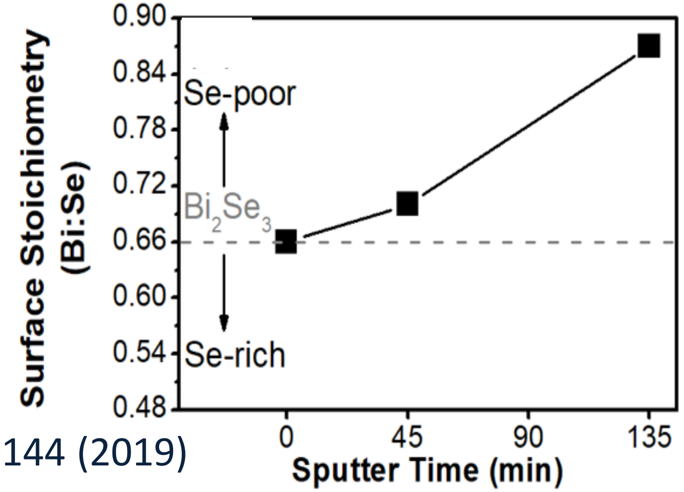


Dirac dispersion

At interface/surface bands must cross



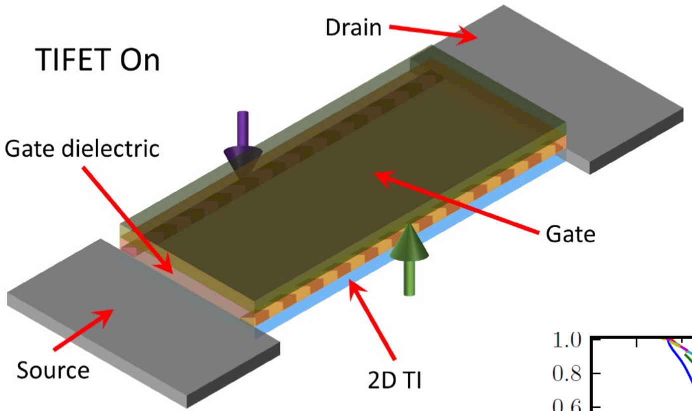
Bi_2Se_3



Barton, Hinkle, et al. ACS Applied Materials & Interfaces 11, 32144 (2019)

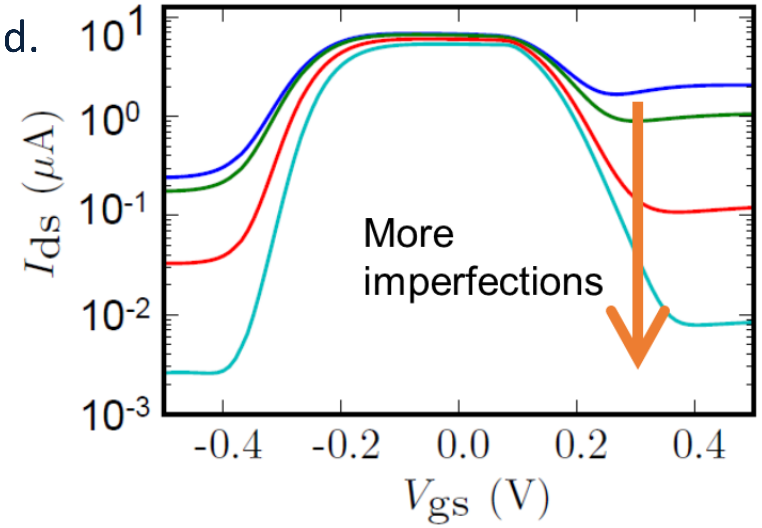
Defect tolerance: TI FET

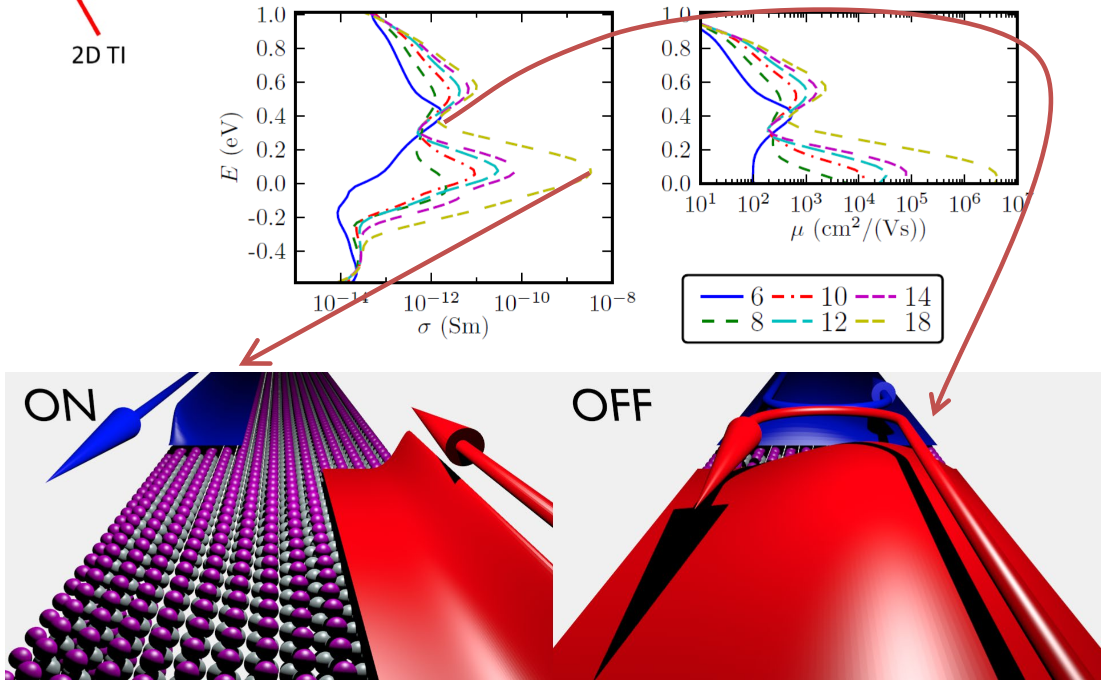
- High conductivity when E_F is in between “bulk” band-gap; no back-scattering allowed.
- Off-state is achieved by moving E_F into one of the bulk bands scattering is high.

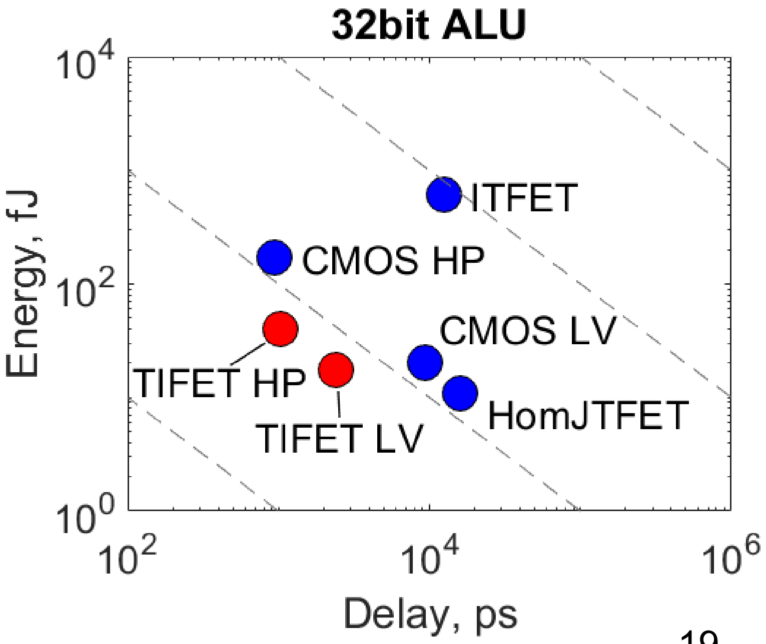


- Calculated current: $I_{ds} - V_{gs}$

Vandenberghe, Nat Comm 8, 1 (2017)



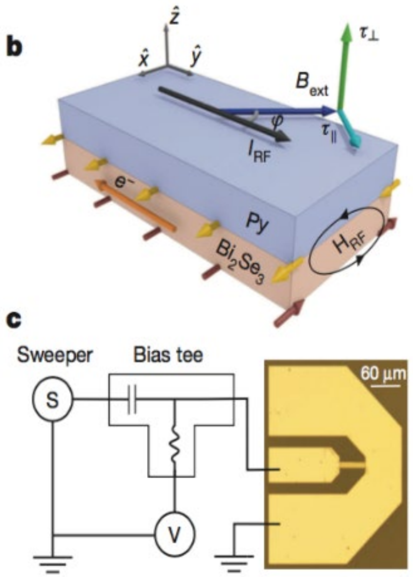




Utilizing TI spin texture

SOT

Mellnik et. al, Nature **511**, (2014)



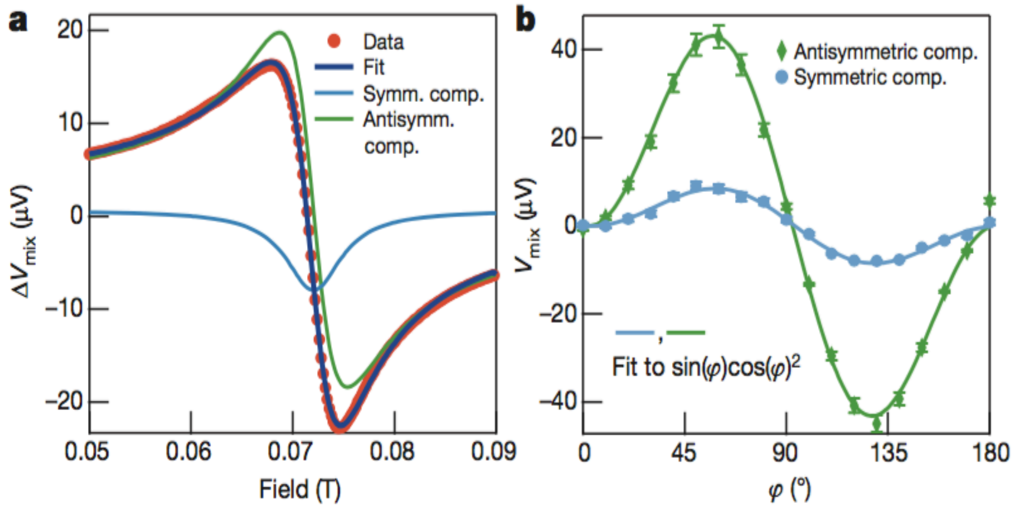
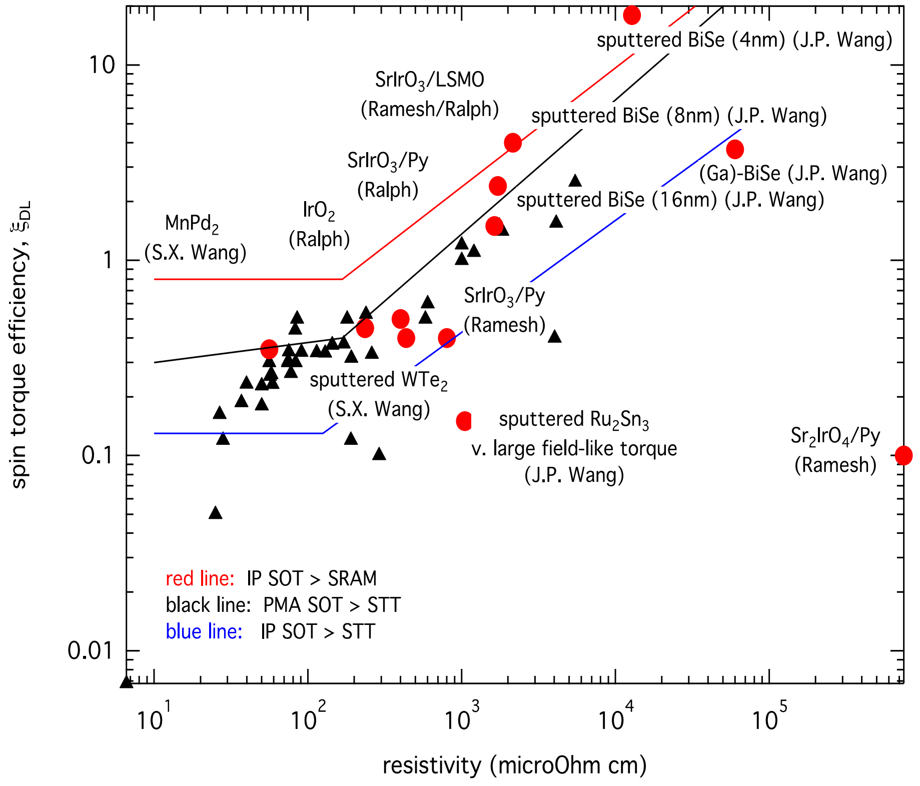
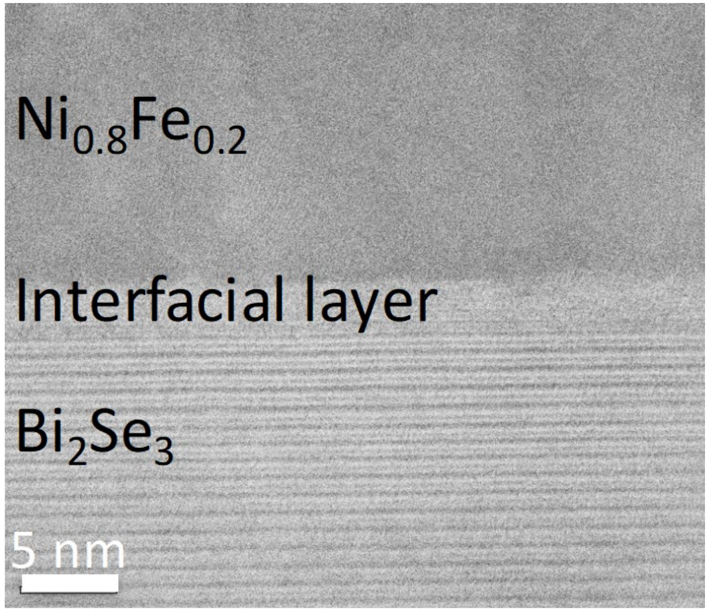
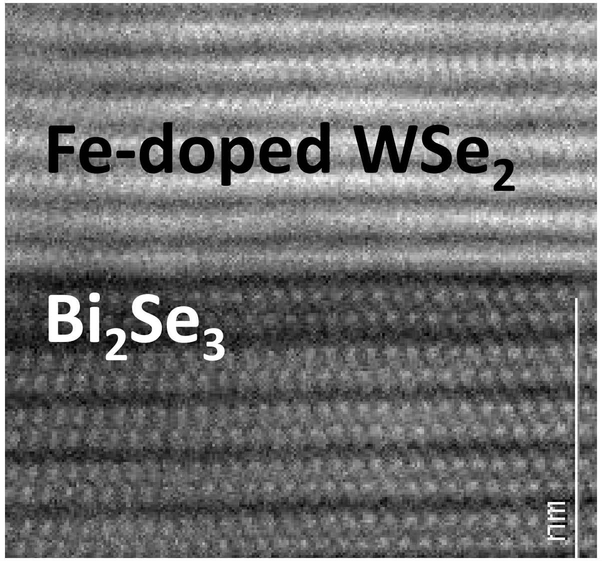


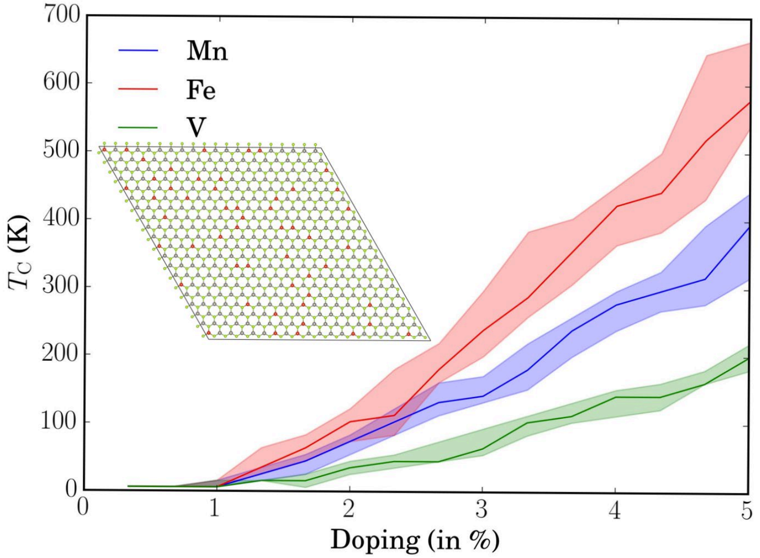
Figure 2 | ST-FMR measurements of the current-induced torque, with fits.



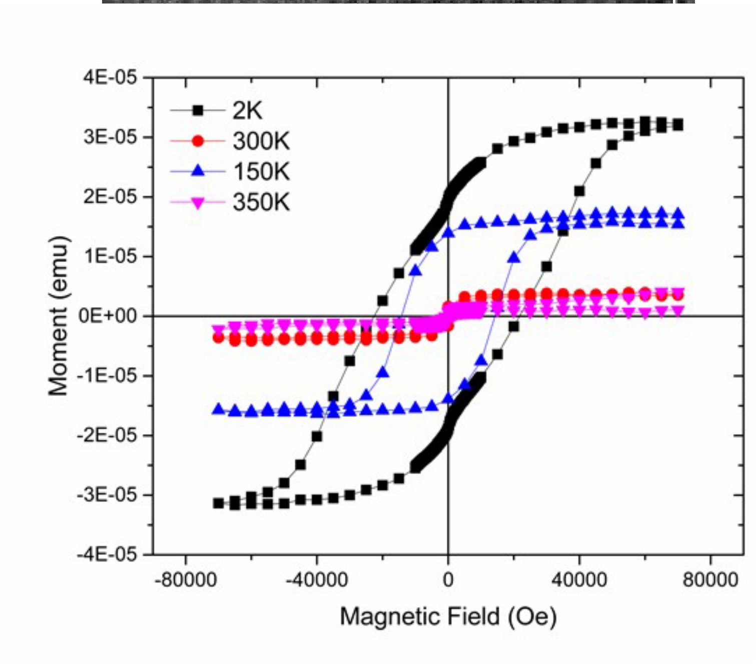
Ferromagnetic TMDs





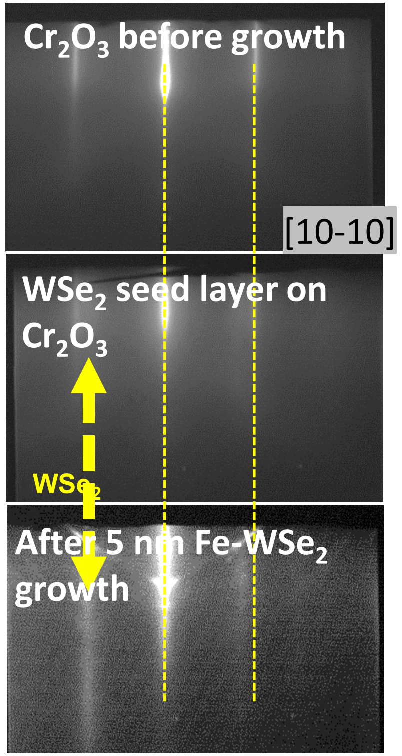


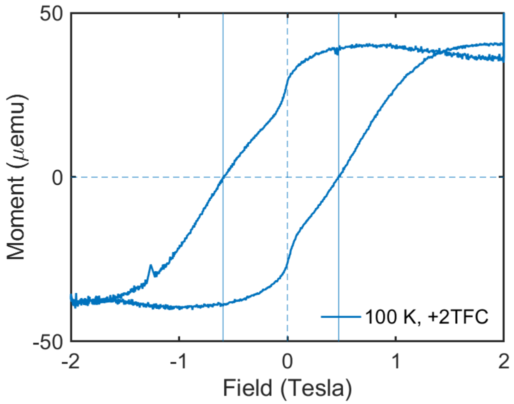
- 2D magnets offer high-quality interfaces
- Efficient spin interaction with underlying materials

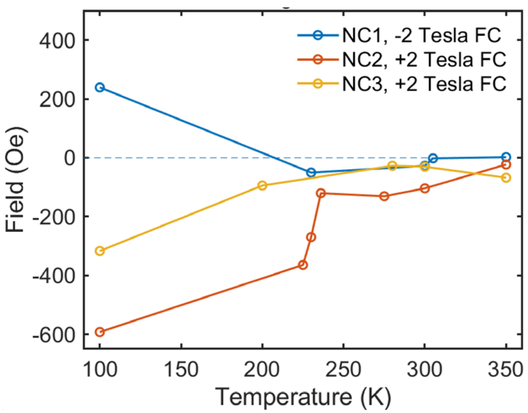


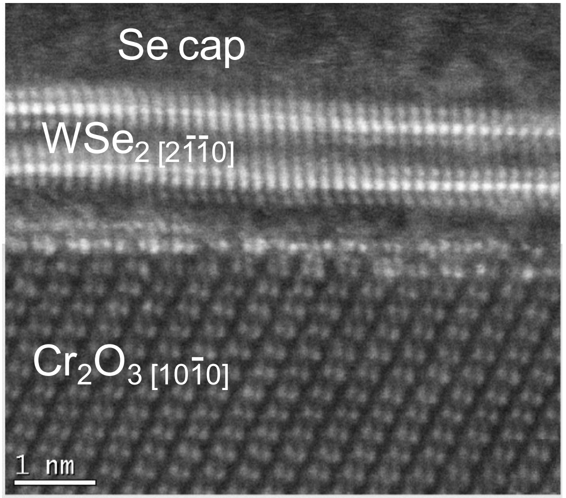
Ferromagnetic interface exchange coupling

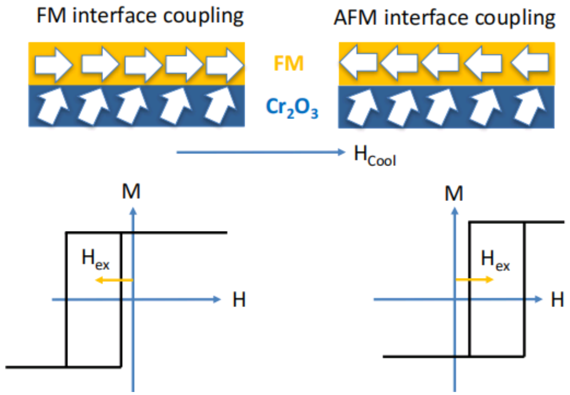
- Epitaxial growth of layered 2% Fe-doped WSe_2 on Cr_2O_3 is realized.
- Bias field emerges below 200 K.
  - Sign of bias field changes together with cooling field, indicating ferromagnetic interface exchange coupling.

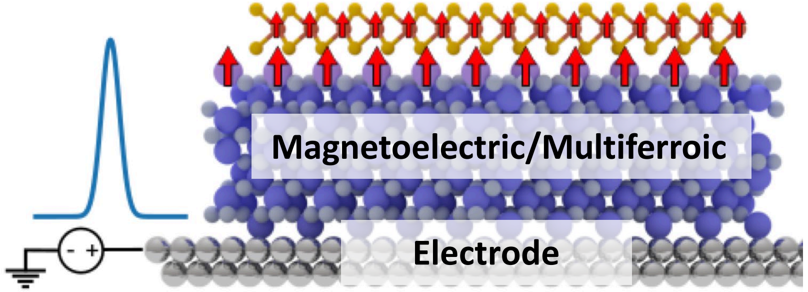










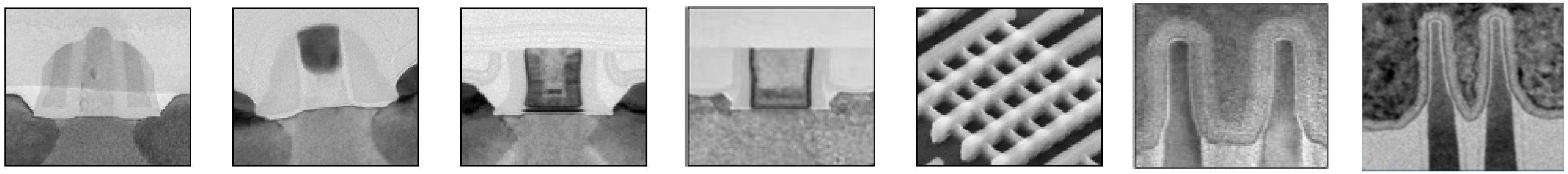


Collaboration with John Heron from Univ. of Michigan

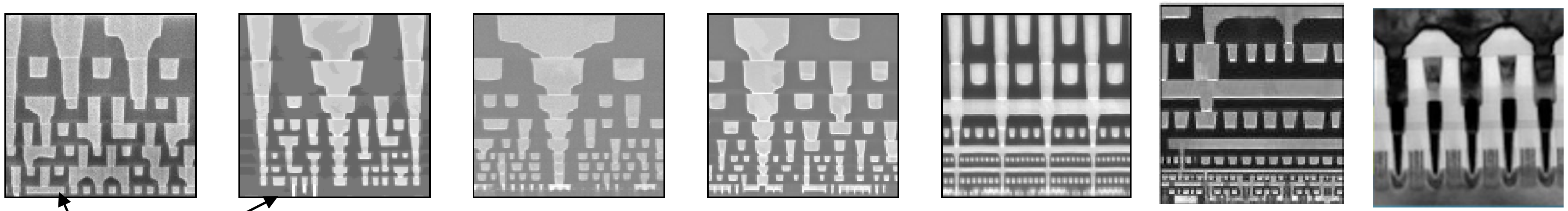
Scaled, dense interconnects

Transistors get smaller and faster,…

90 nm	65 nm	45 nm	32 nm	22 nm	14 nm	10 nm
2003	2005	2007	2009	2011	2014	2017



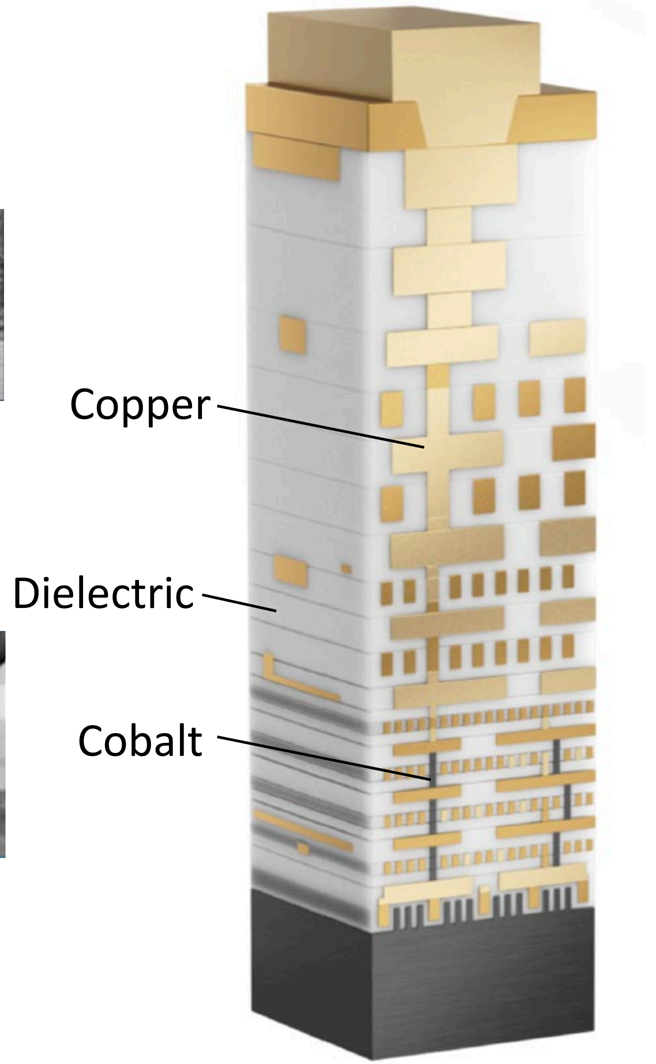
Faster transistor speed



Metal layer 1 width

120 nm	95 nm	68 nm	52 nm	40 nm	26 nm	18 nm

Increased Interconnect Delay



Schematic from Intel Architecture Day 2020

… wires get smaller and slower.

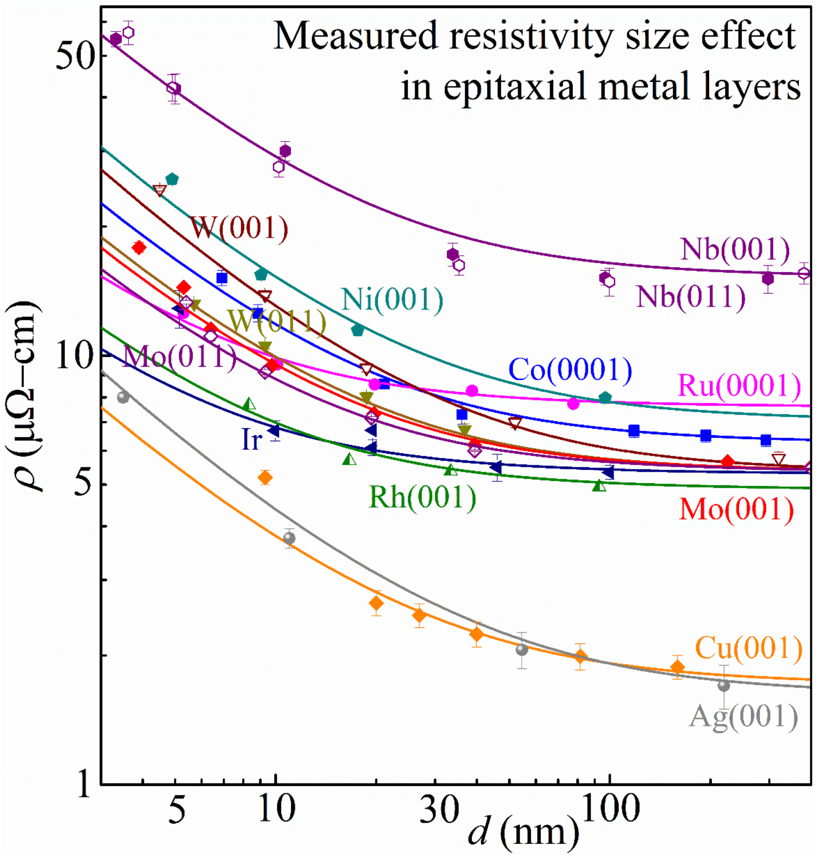
http://download.intel.com/newsroom/kits/22nm/pdfs/22nm-Details_Presentation.pdf; http://download.intel.com/newsroom/kits/14nm/pdfs/Intel_14nm_New_uArch.pdf; Intel Technology and Manufacturing Day 2017

Scaled, dense interconnects

Prof. Daniel Gall, RPI

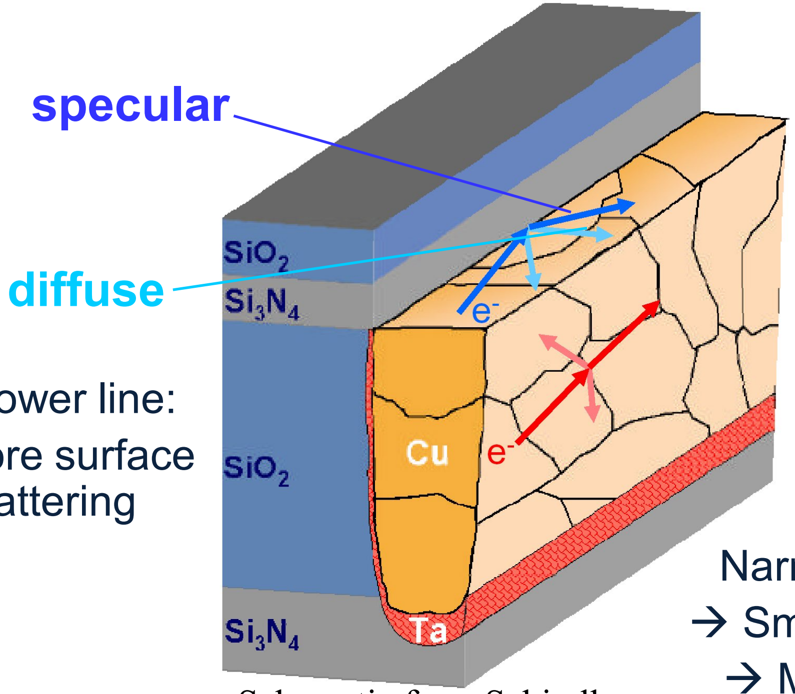
IMPACT
Innovative Materials and Processes for Accelerated Compute Technologies

Problem: The resistivity of metal wires increases with a decreasing cross-section.



Causes for resistivity increase:

(1) Surface scattering



Schematic from Schindler

Narrower line:
→ More surface scattering

Solution:

Specular scattering

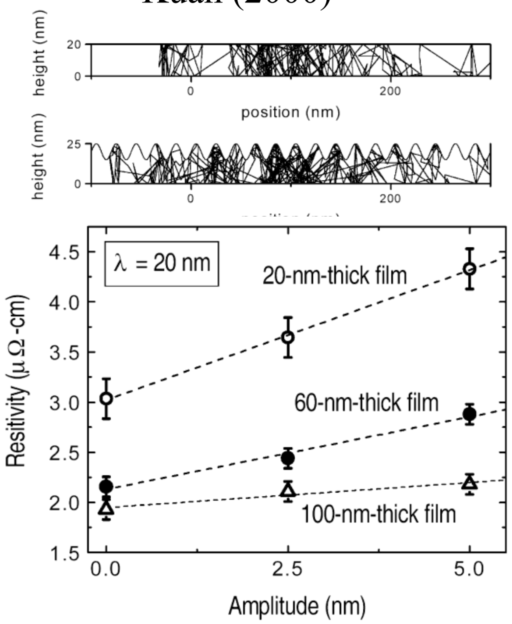
(2) Grain boundary scattering

Narrower line:
→ Smaller grains
→ More grain boundary scattering

Large grains
or
100 % Transmission

(3) Roughness effects

Classical Monte-Carlo
Kuan (2000)

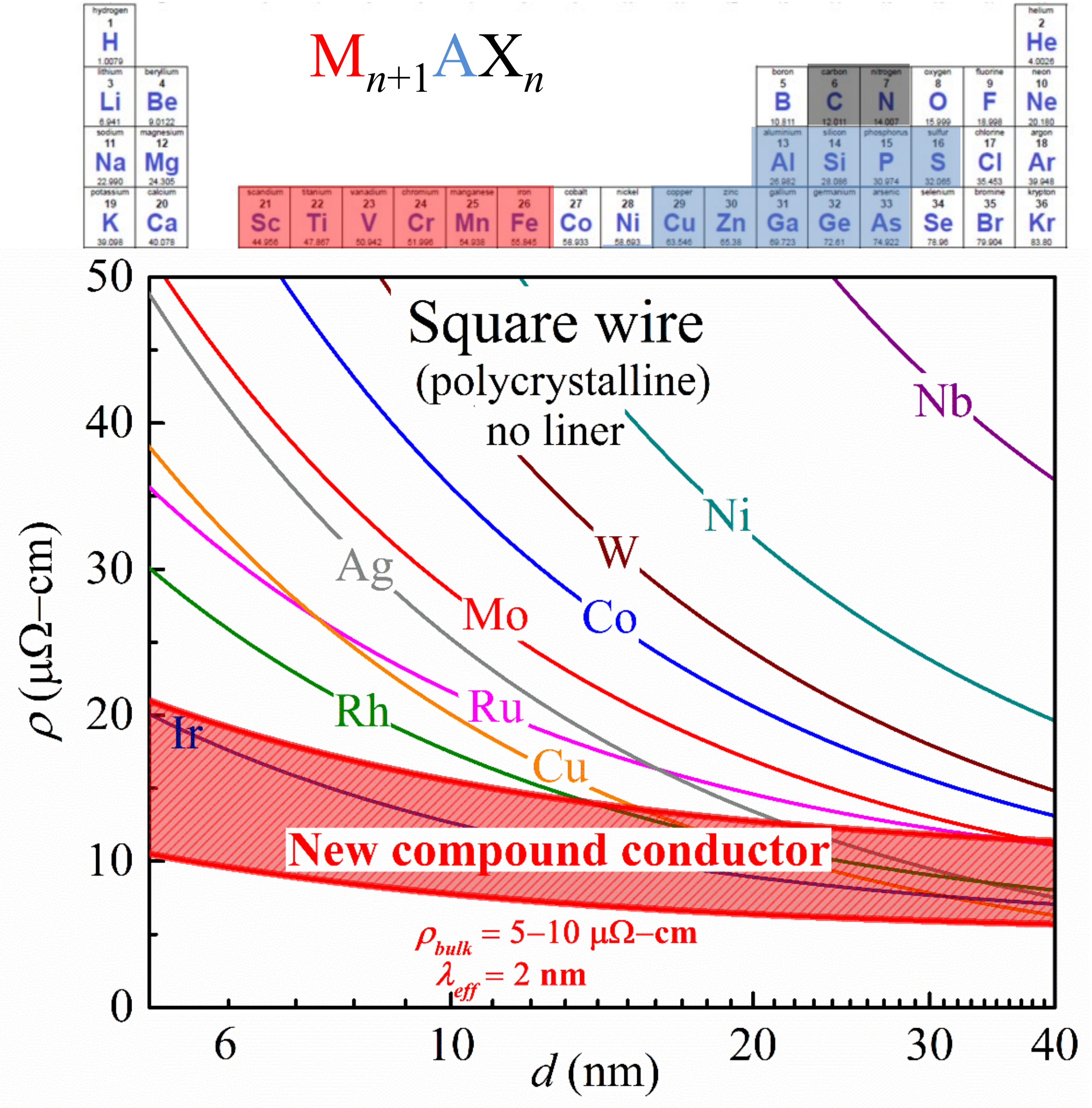


Narrower line:
→ Surface roughness is more important

Smooth interfaces

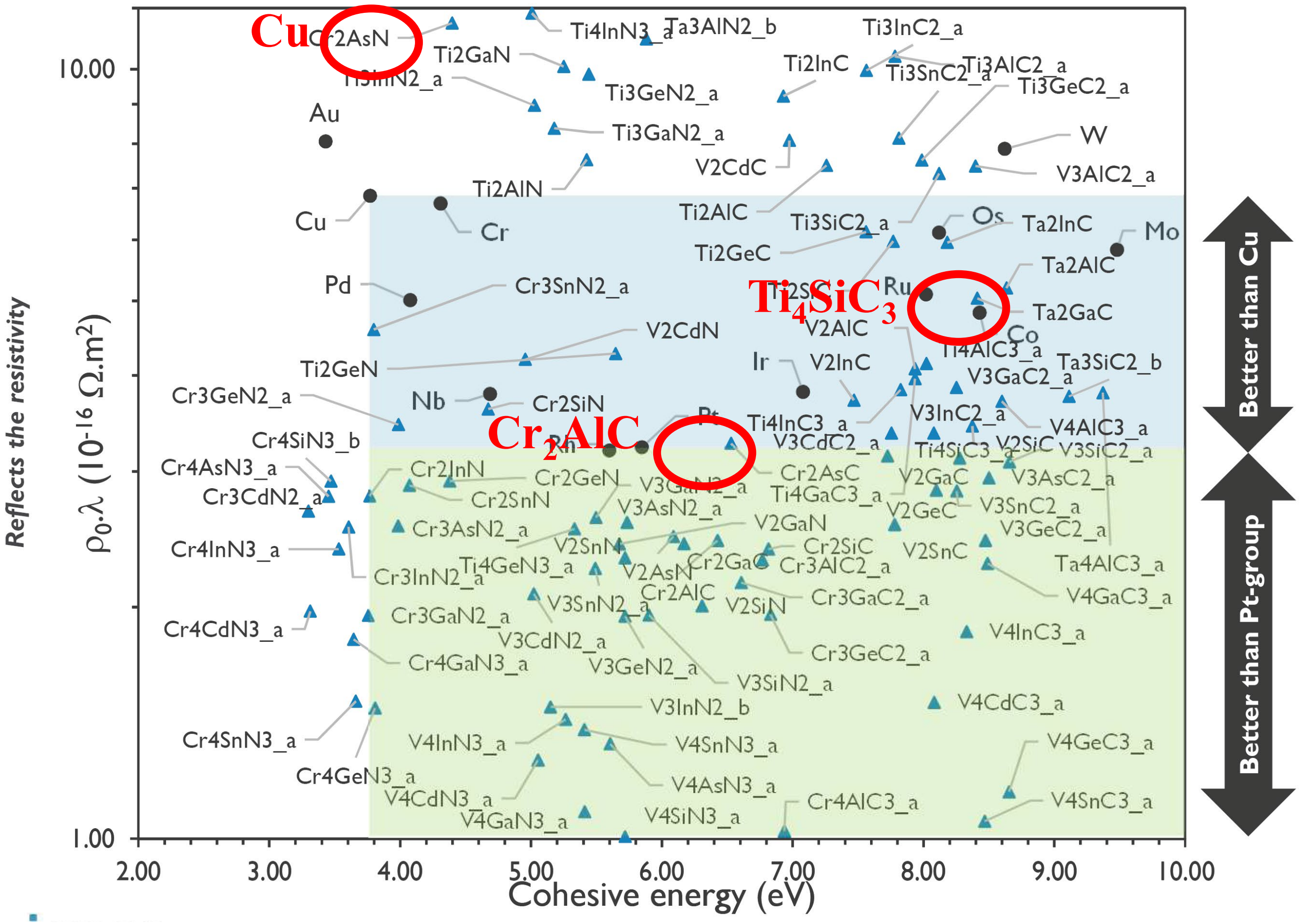
Cr_2AlC and Ti_4SiC_3 (MAX phase)

Prof. Daniel Gall, RPI



alternative conductors for narrow interconnects

IMEC prediction (2018): a large number of MAX phase compounds outperform elemental metals:

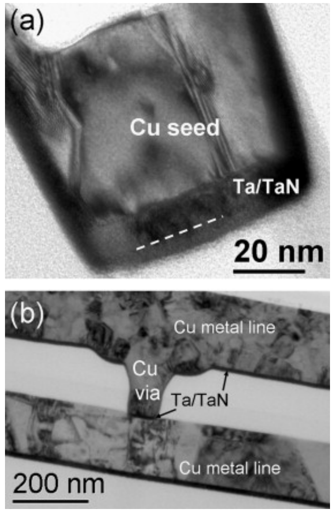


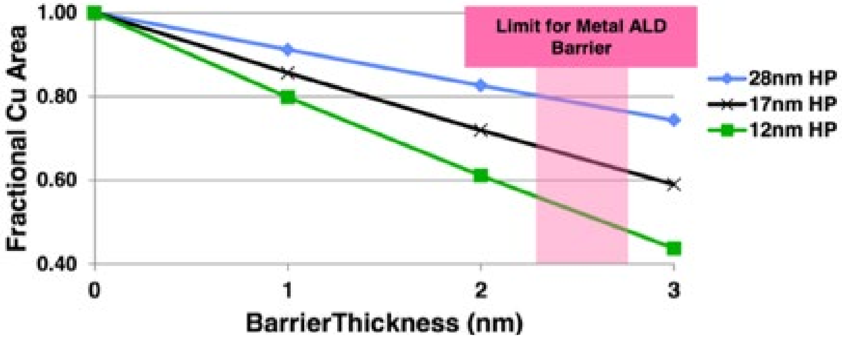
Daniel Gall, "The search for the most conductive metal for narrow interconnect lines," (invited perspectives article) J. Appl. Phys. **127**, 050901 (2020).

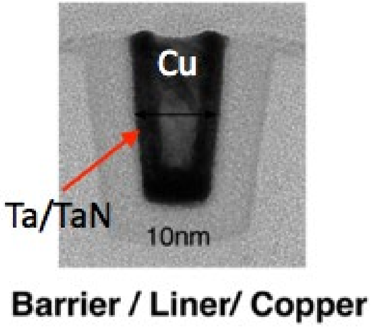
K. Sankaran, K. Moors, S. Dutta, C. Adelmann, Z. Tokei, and G. Pourtois, in *Metallic ceramics for low resitivity interconnects: an ab initio insight*, iitc 2018.

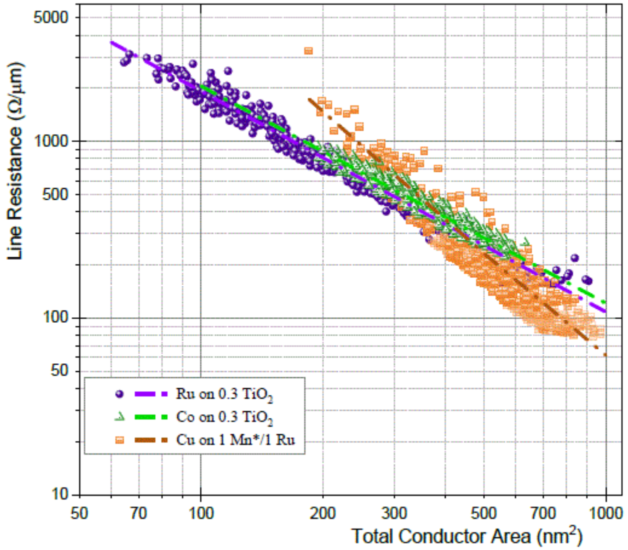
2D materials for interconnect liners

TaN/Ta > 4nm is needed to block Cu diffusion









van der Veen, IMEC, IITC (2018)

PTC, Mat. Sci. Semi. Proc., **27**, 860 (2014)

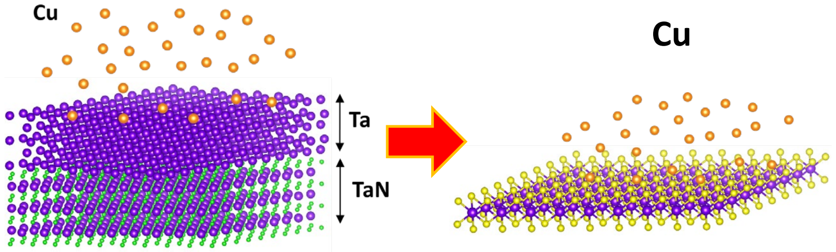
Interconnects are very resistive at scaled dimensions: (1) Increasing Cu resistivity; (2) Limited Cu area

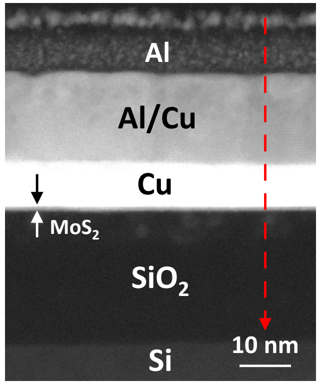
- Explored MoS_2, TaS_2, graphene, hBN
- BEOL compatible growth
- Excellent Cu diffusion barrier properties
- Excellent wetting and adhesion
- Reducing Cu resistivity by suppressing scattering

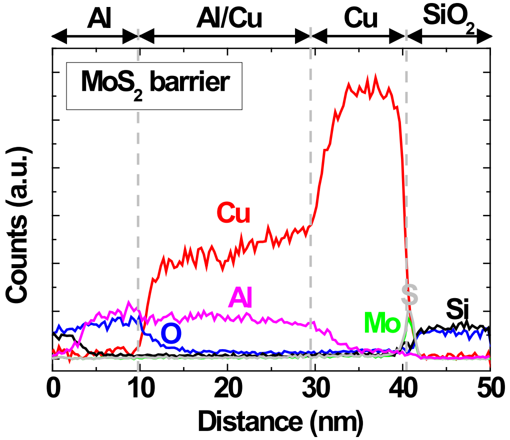
Zhihong Chen

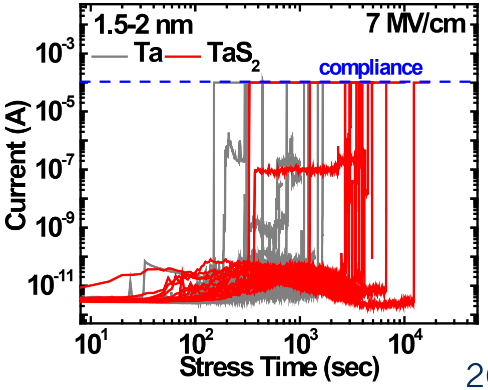
Review: JAP, **128**, 080903 (2020)

Atomically thin 2D barrier/liner for enhancing Cu interconnect performance





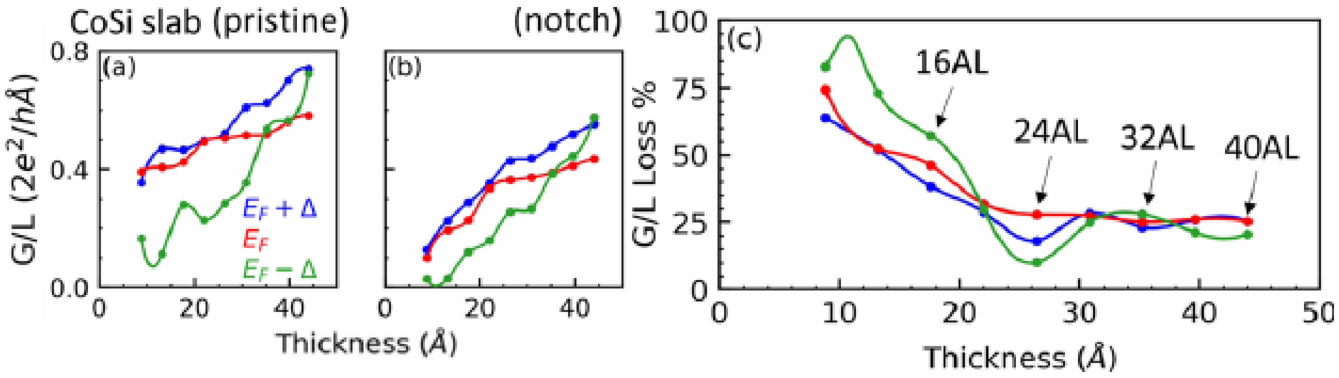


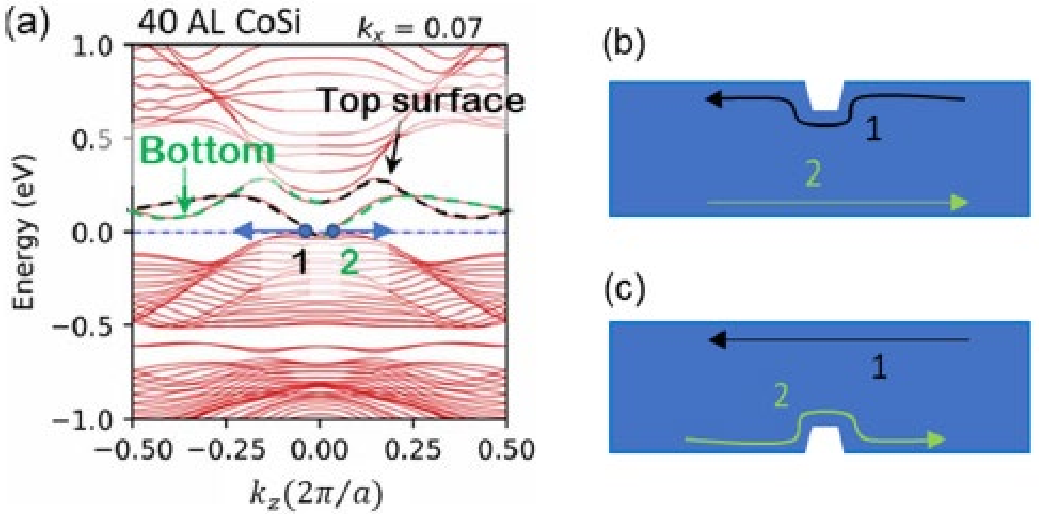


Topological interconnects

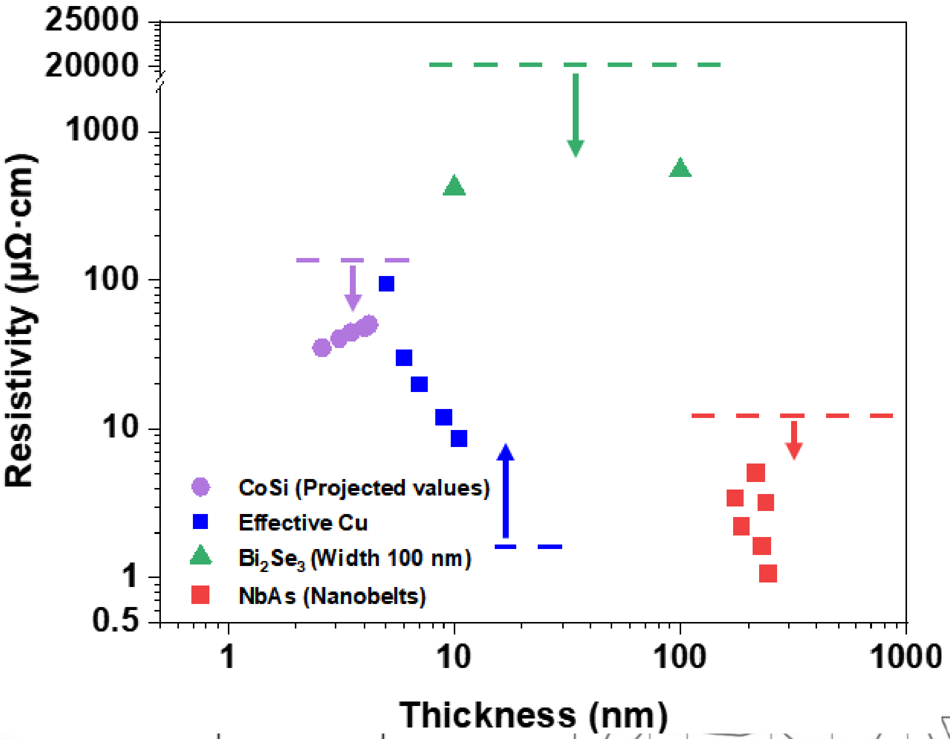
IMPACT
Innovative Materials and Processes for Accelerated Compute Technologies

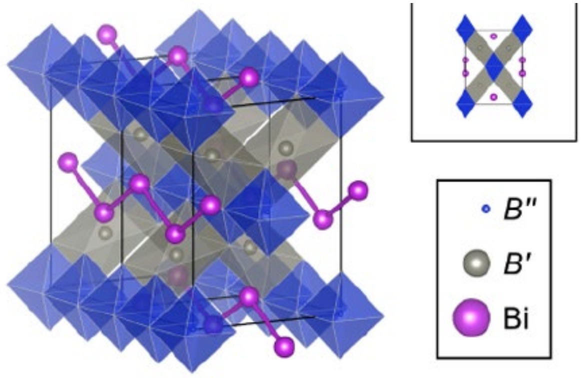
CoSi, multifold-fermion semimetal

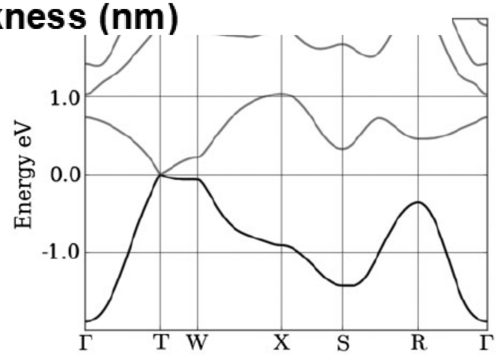




Ching-Tzu Chen, et al., IBM, IEDM (2020).







(a) $BiZnSiO_4$

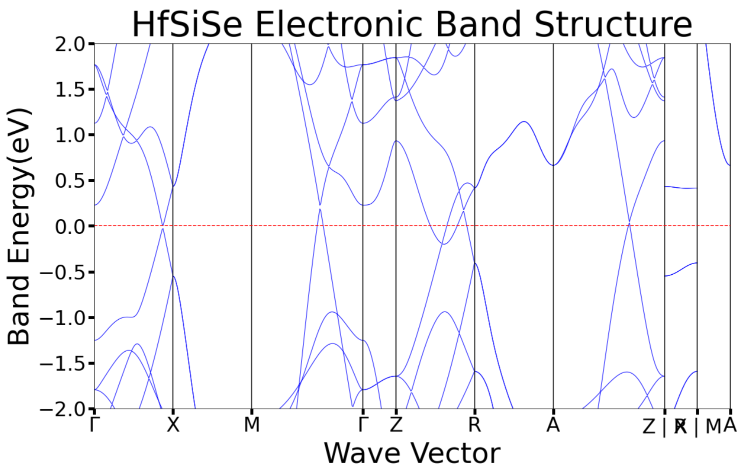
Steinberg, Kane, Mele, and Rappe, Phys. Rev. Lett. 112, 036403.

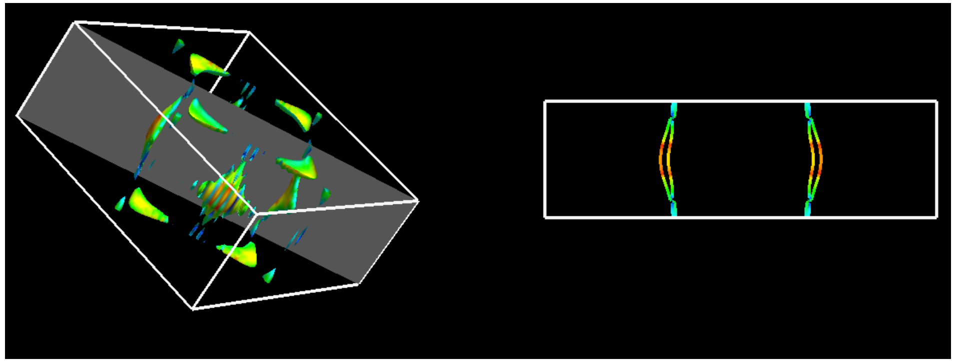
Additional Needs

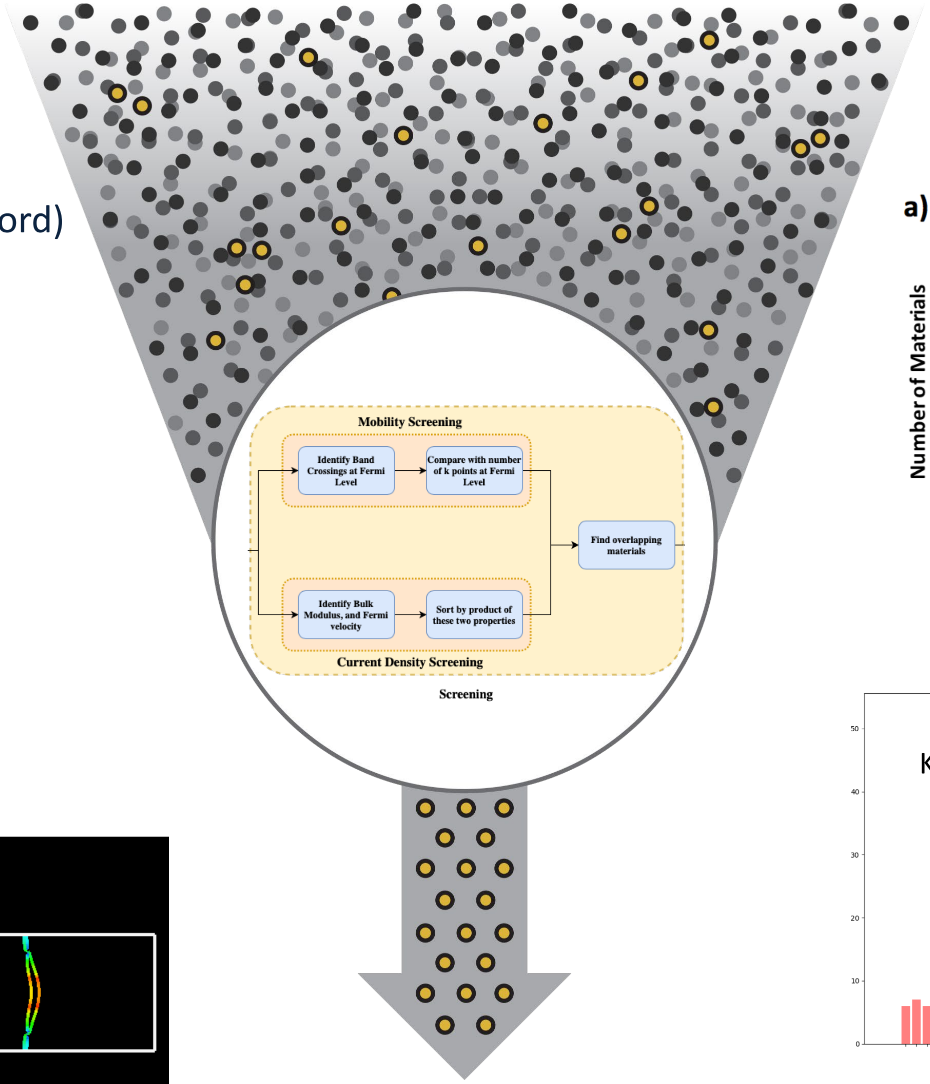
Data mining and physics-based ML to screen materials

New Weyl Semimetals

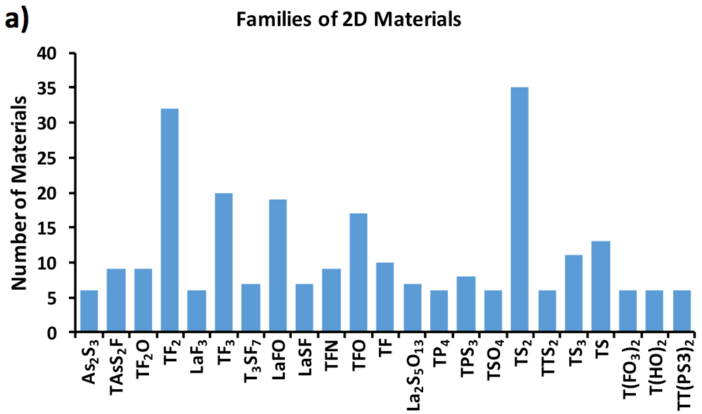
Evan Antoniuk, Akash Ramdas, Evan Reed (Stanford)



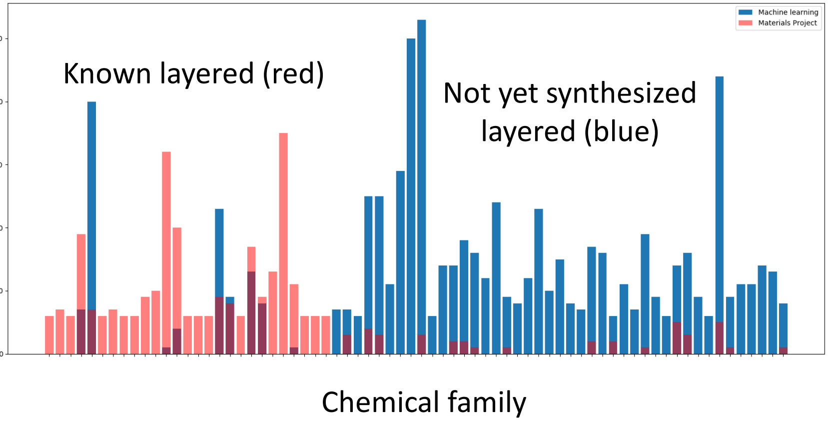




New 2D Materials

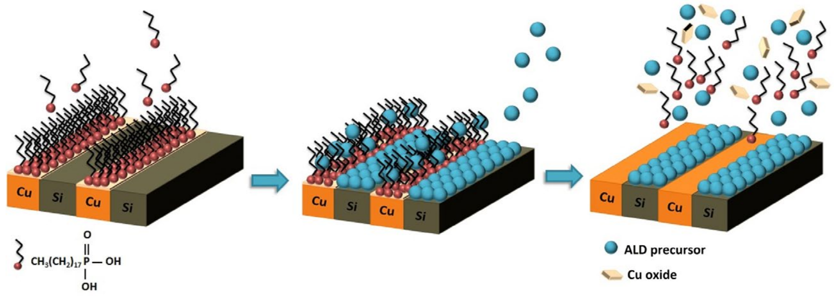


***DMREF* Award 1436330**



Cheon, Duerloo, Sendek, Porter, Chen, Reed, Nano Letters 17, 1915 (2017).

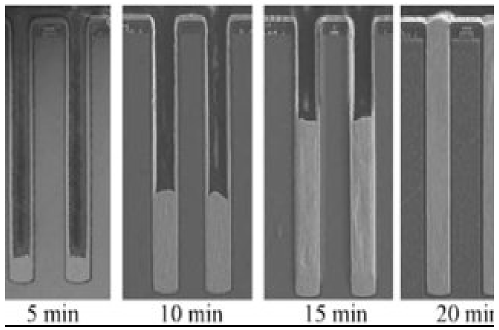
Area-selective ALD



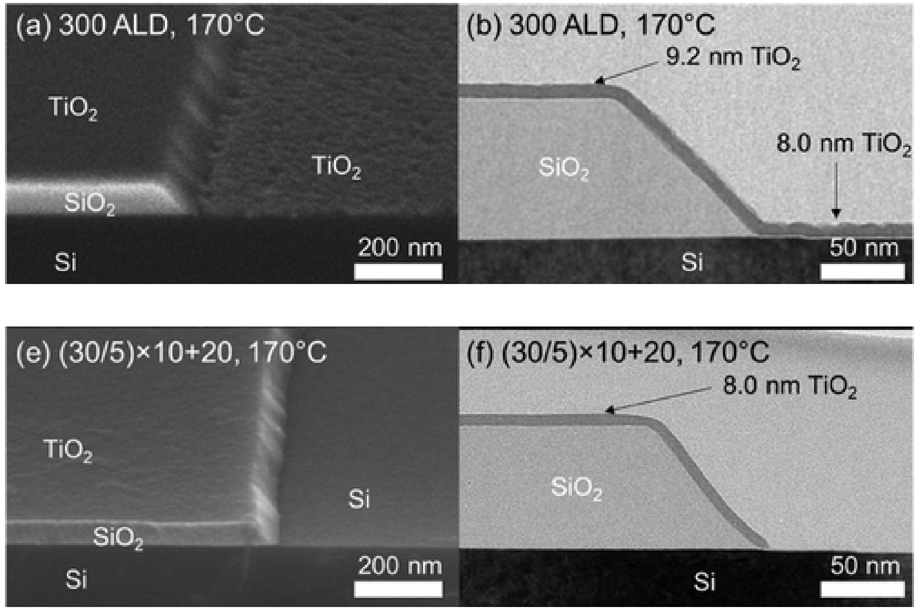
Al Auger map

SEM　60 cycles Al_2O_3 ALD　after etching

Bent (Stanford)

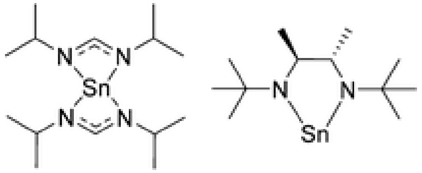


George (Colorado)
Kummel (UCSD)



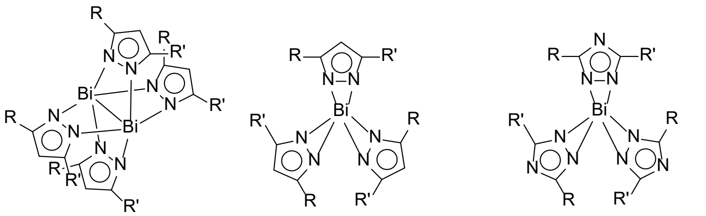
Parsons (NC State)

New precursors are needed



Gordon (Harvard), Hock (IIT)

Currently, no good commercially available Sn(II) or Bi precursors



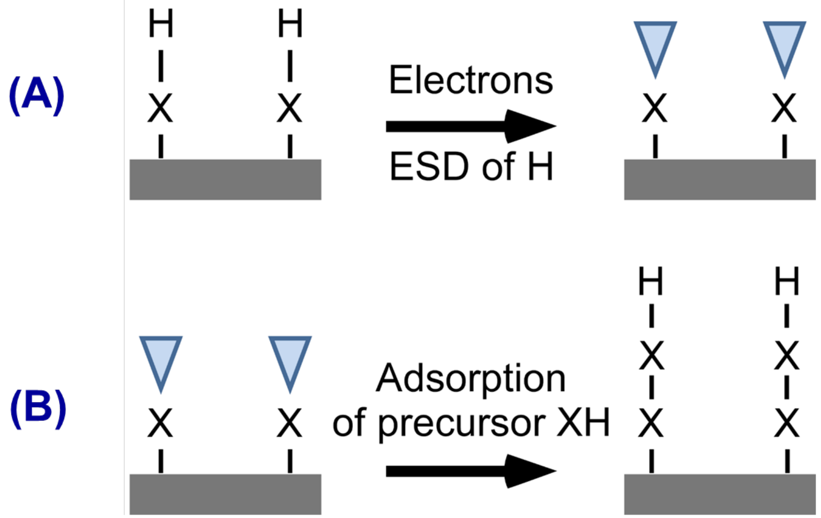
1, R = R' = tBu
2, R = R' = C_6H_5
3, R = R' = CF_3
4, R = $CF_2CF_2CF_3$, R' = tBu
5, R = R' = alkyl, perfluoroalkyl

Winter (Wayne St)

Electron enhanced ALD

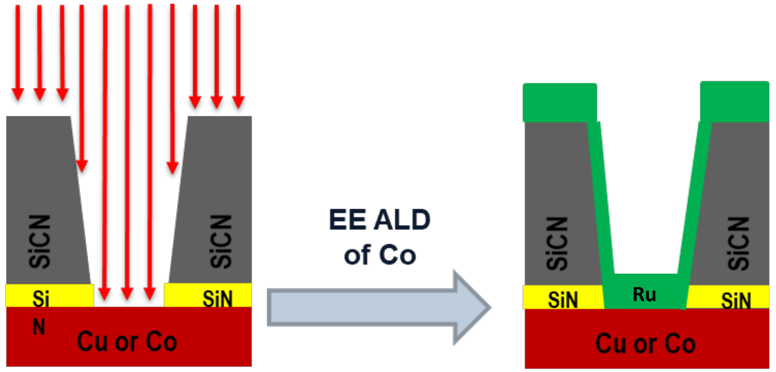
Zach Sobell, Michael Collings, Andrew Cavanagh, and **Steven George**, Dept. of Chemistry, Univ. of Colorado

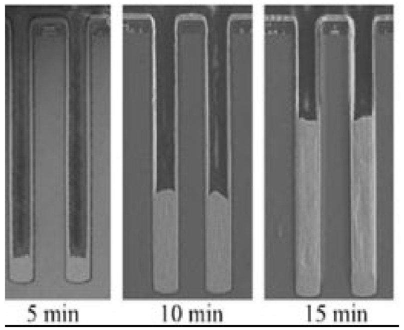
EE-ALD Using Electron Stimulated Desorption (ESD)



Directional Electron Flux

Deposition Primarily on Horizontal Surfaces





Non-thermal process for low temperature deposition

Current Work on Ru EE-ALD at Low Temperature

Sequential Precursor & Electron Exposures:

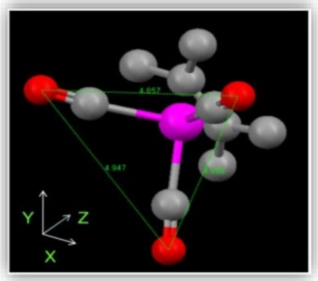
(A) Precursor Adsorption

$Ru^* + (DMBD)Ru(CO)_3(g) \rightarrow Ru\text{-}Ru(CO)_3 + DMBD\ (g)$

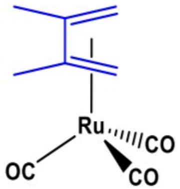
(B) Electron Stimulated Desorption

$Ru\text{-}Ru(CO)_3 + e^- \rightarrow Ru\text{-}Ru^* + 3CO\ (g)$

* designates surface species



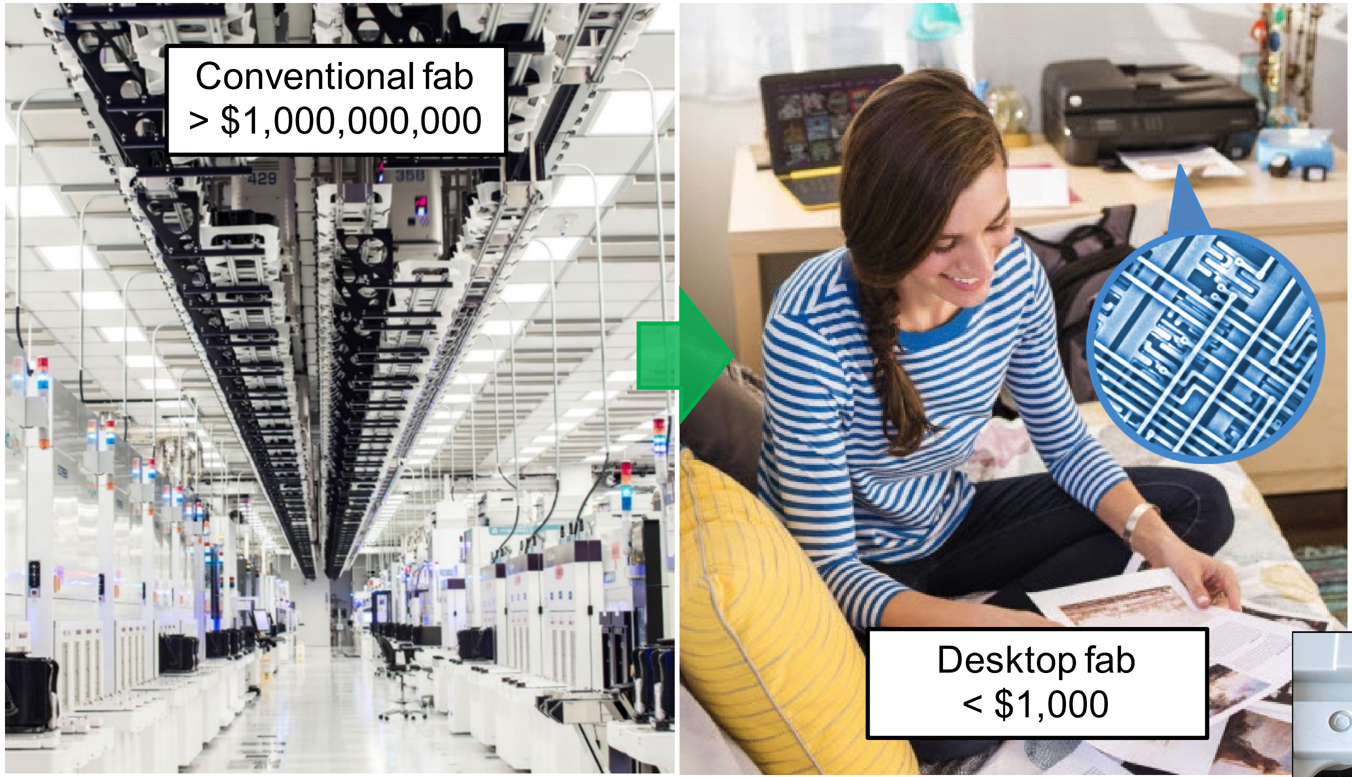
RuDMBD
Ru(0)



Dimethylbutadiene-tricarbonyl Ruthenium

Desktop IC manufacturing

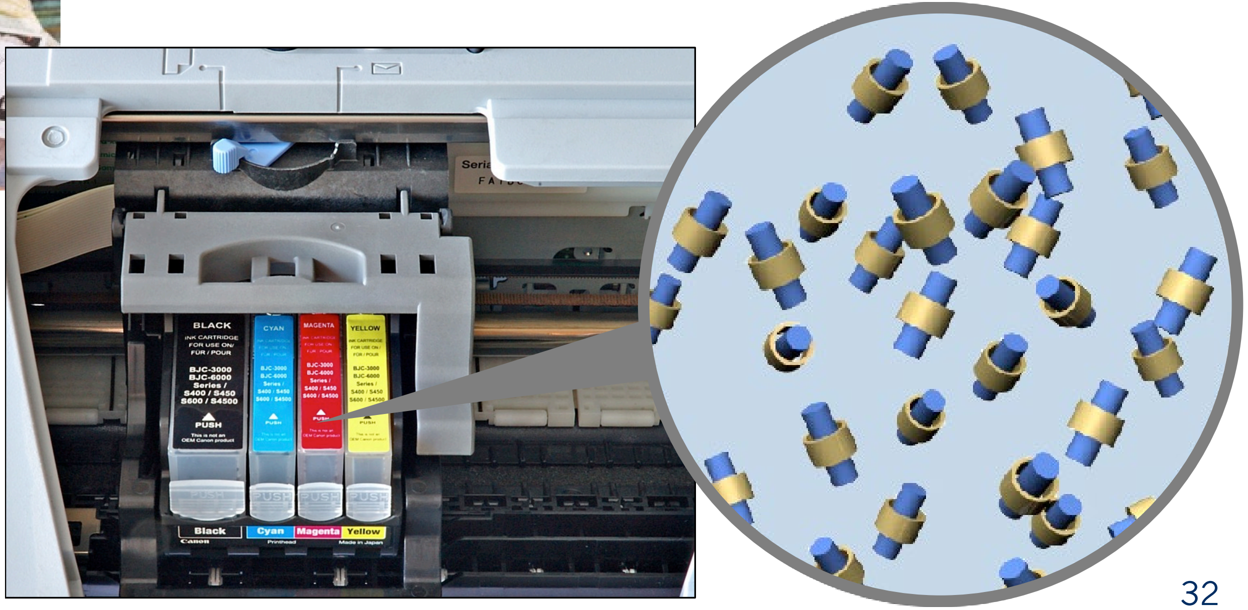
Michael Filler and Eric Vogel – Georgia Tech



	Integrated	Modular materials	Modular devices
Examples	InchFab	Organics, NCs	GT/UMich
Mobility	~500 cm^2/V-sec	~1-20 cm^2/V-sec	~500+ cm^2/V-sec
Critical feature size	Limited by lithography (~10 nm)	Limited by print resolution (~10 mm)	Limited by device synthesis (~10 nm)
Unique mask sets	Yes	No	No
Heterogeneous integration	Same challenges as wafers	Yes, of materials	Yes, of devices
Local process temperature/toxicity	High	Moderate	Low
Interconnect	Via lithography	Via printing	Via printing
Materials flexibility	Low	High	High
Cost of ownership	Moderate	Low	Very low
Desktop footprint	No	Yes	Yes
Supply chain	Interdependent	Interdependent	Independent

Requires:

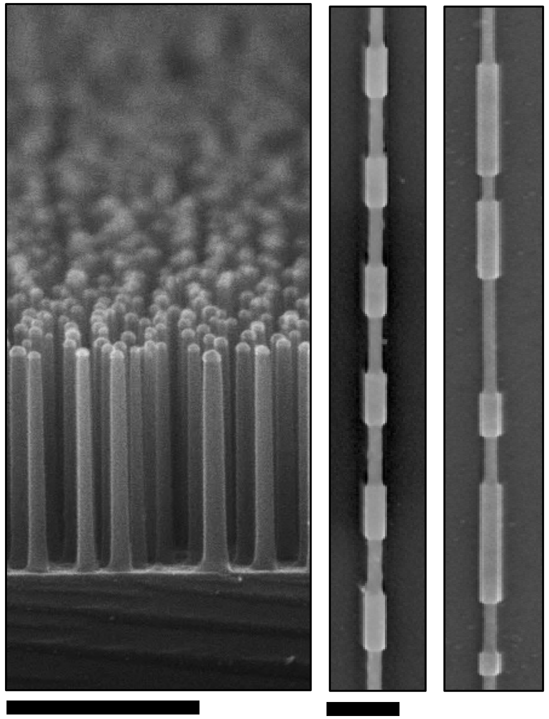
- Plug-and-play
- Extreme low cost
- Functional diversity



Modular devices for desktop IC manufacturing

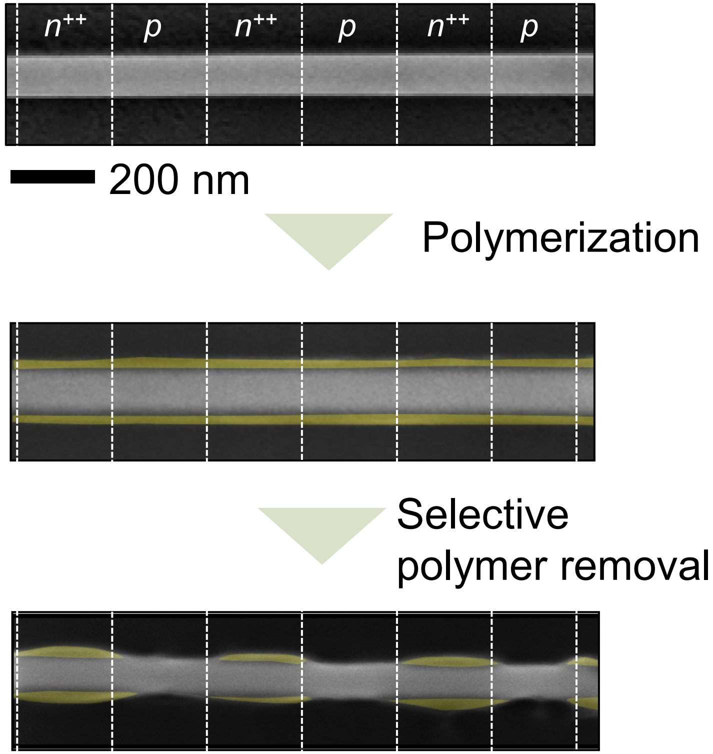
Michael Filler and Eric Vogel – Georgia Tech

Bottom-up synthesis



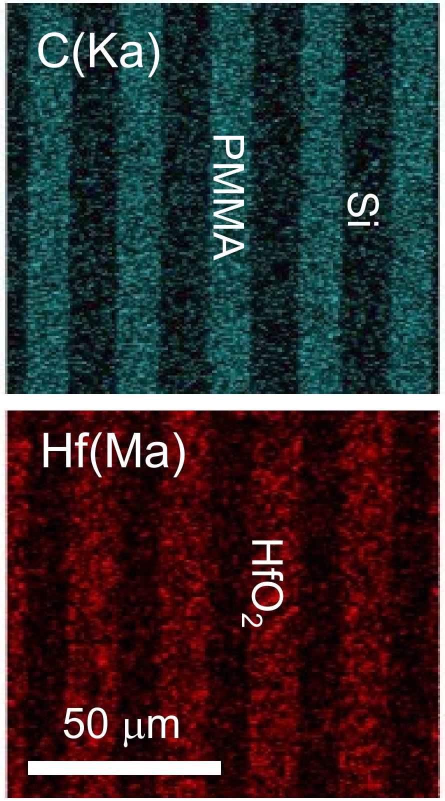
Programmable structure/ composition

Non-photolithographic patterning



Deep sub-micron features

Selective deposition



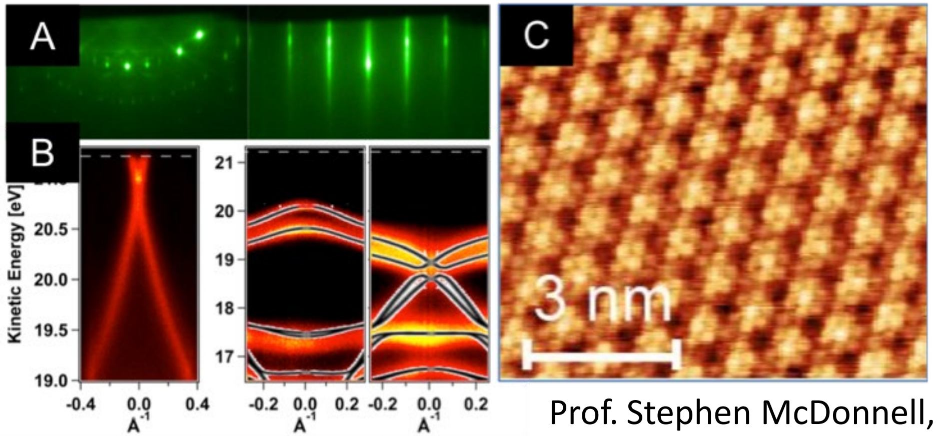
High quality films

Enables heterogeneous integration

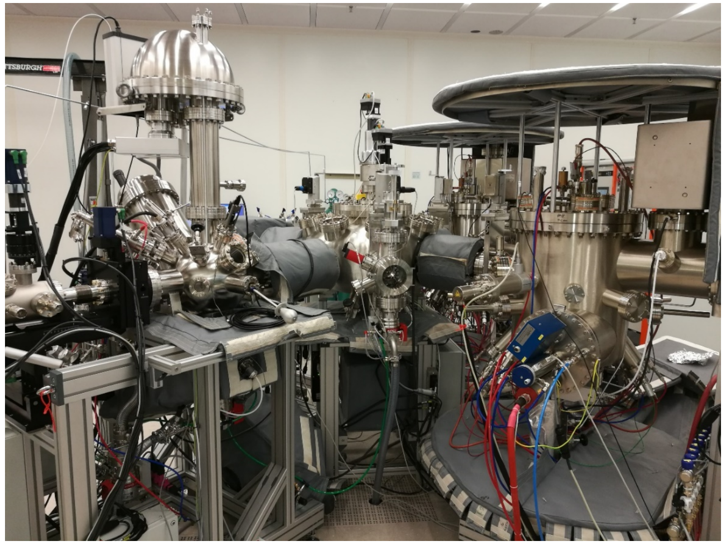
- Use of diverse processes, materials, and devices
- High T front-end devices deposited on low T substrates

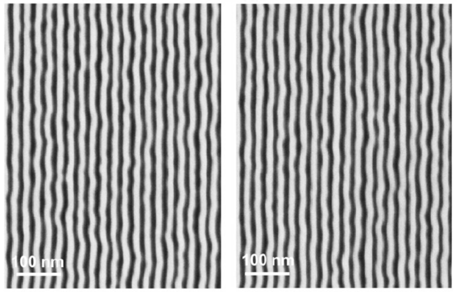
Aligned with on-going progress in printing technology

Multi-modal characterization, in-situ, in-operando



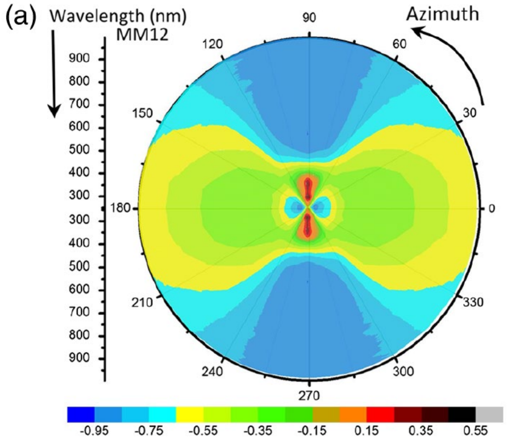
Prof. Stephen McDonnell, U of Virginia

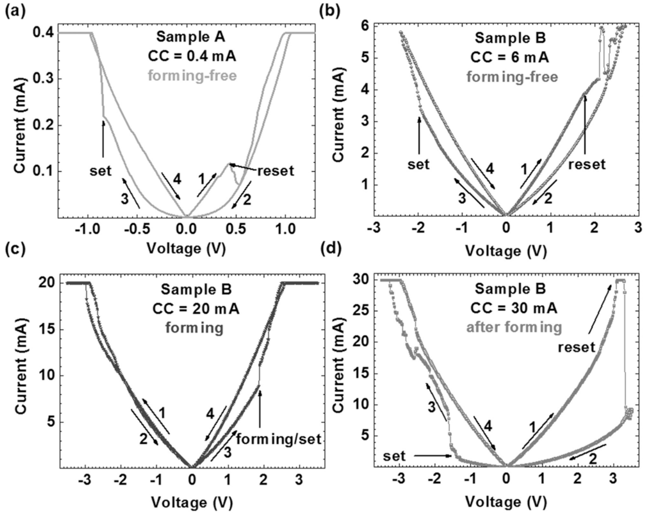


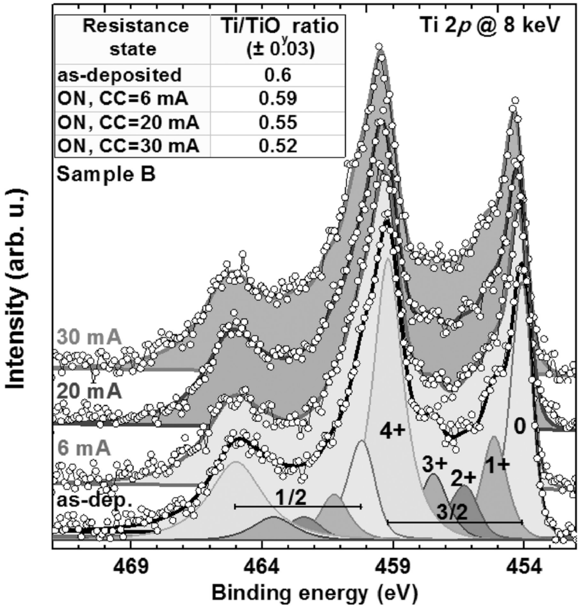


Inline monitoring for 3D structures

In-operando HAXPES







Dixit et al., J. Micro/Nanolith. MEMS MOEMS 14, 031208 (2015)

Sowinska et al., JAP 115, 204509 (2014)

Summary

- Co-locate new logic with embedded NVM in upper layers and develop ultra-dense, nanoscale interconnects.

- Develop new synthesis techniques and combine with aggressive deployment of old techniques.
    - Lower energy barriers (surfactants, catalysts, 2D materials)
    - Provide energy in non-thermal ways (plasma/electron enhanced)
    - Selective chemistry

- Exploit fundamental physics and engineering findings for BEOL applications.
    - Configurational entropy
    - Topologically protected transport
    - Orbital engineering

- Continue to work closely with theorists and develop new characterization tools.