

Submodule Fault Detection in MMCs using Support Vector Classification

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Abstract—With increasing use of modular multilevel converters (MMC), diagnosis and localization of submodule (SM) faults are gaining importance. Most of the existing SM open-circuit (OC) fault detection methods perform diagnosis and localization separately leading to longer detection times. In this paper, a support vector classifier (SVC)-based SM double-switch OC fault diagnosis method, combining detection and localization, is proposed. The proposed method does not require any additional hardware. The training set for the SVC is created by simulating normal operation and SM double-switch OC faults in PSCAD/EMTDC software. Simulation results analyze the performance of the proposed method.

Index Terms—Machine learning, multilevel converters, pulse width modulation, selective harmonic elimination, support vector classification.

I. INTRODUCTION

The modular multilevel converter (MMC) is a power electronics converter topology used in HVDC power transmission, FACTS devices, and high-voltage drives. The MMC can help generate high voltage levels with low harmonic content through low voltage SMs which can be controlled individually [1]. Some of the advantages of the MMC are as follows:

- Good output harmonic performance when providing high voltages [1],
- High modularity [2], and
- Low current rating for power switches [1].

An MMC consists of many SMs and each SM contains insulated gate bipolar transistors (IGBT). IGBTs are one of the most fragile components in the SM, making them prone to firing faults [3], [4]. These faults can be classified as open-circuit (OC) and short-circuit (SC). SMs typically have SC withstand times in the order of microseconds as the capacitor in the SM discharges immediately [5]. SM SC faults are suppressed by hardware diagnostic methods [6], [7]. However, SM OC faults can remain undetected without specific diagnostic methods, lead to derating of the MMC by preventing discharge of the capacitor in the faulted SM. This damages the converter [8] and distorts the current waveform [9]. Proper diagnosis of the SM OC fault requires fault detection and localization. Fault detection methods generate an alarm to indicate the occurrence of an OC switch fault in a phase. The faulty SMs

are identified through fault localization methods and bypassed by their antiparallel switches using a fault-tolerant control method.

SM OC fault detection methods can be of two types: hardware-based and software-based [10]. Reference [11] proposes a hardware-based nearest level modulation (NLM) method for detecting OC faults. This, however, requires installation of an additional inductor winding to measure the voltage across the arm inductors. Reference [12] proposes a hardware-based method that performs fault diagnosis in the respective SM. This method requires the measuring points of the voltage sensor to be reconfigured to monitor the SM terminal voltage. Reference [13] compares the output voltage of a group of SMs with certain reference voltages and requires an additional supervisory sensor to obtain those references. Reference [14] proposes hardware-based fault detection by studying the output voltages of the SM under both normal and fault conditions. However, it requires the aid of an extra hardware circuit to detect SM output voltage. Hardware-based methods, in general, require changes in the installation, increasing the difficulty of implementation. This shortcoming reduces their applicability in existing commercial projects. On the other hand, software-based fault detection methods proposed in [15], [16] eliminate the need for extra hardware devices. Model-based software methods compare measured state variables with estimated state variables, which are computed using mathematical modeling [15]. Reference [15] estimates the ideal circulating current and the output current using the state model of the MMC and the variables in the main control system. However, there is a long time interval (more than 100 ms) to diagnose which SM is faulty. References [17] and [18] propose data driven methods for faulty SM identification. However, they use manually determined thresholds requiring intervention in tuning. Reference [19] proposes an artificial neural network (ANN)-based method to detect the faulted SM. This method computes a threshold for identifying how long a faulted SM exhibits highest voltage in a given time period.

This paper proposes an SVC-based SM fault detection method for MMCs. The proposed method does not require extra hardware devices, utilizes the voltage sorting array in the MMC controller allowing it to be embedded as a code inside the controller itself. This removes the need for a design change of the controller. The SVC does not require model-based state estimation and indicates the presence of a double-switch SM

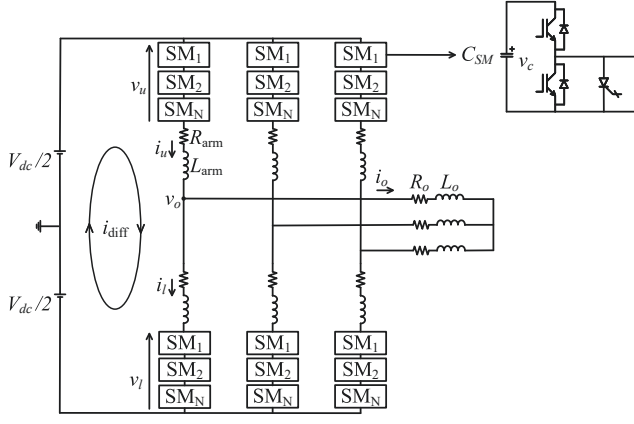


Fig. 1. Three-phase MMC.

OC fault. Studies are performed in PSCAD/EMTDC software to create a dataset for training the SVC. A three-phase MMC with 4 SMs in each arm is modelled in PSCAD/EMTDC.

The rest of this paper is organized as follows. Basics of MMC control, operating principles and double-switch faults in the MMC are introduced in Section II. Section III discusses the proposed fault detection and localization method. Section IV discusses the performance validation of the proposed method in PSCAD/EMTDC. Finally, the conclusions are provided in Section V.

II. SM FAULTS IN MMCs

A. Overview of MMC Modeling and Control

Fig. 1 shows the generic topology of a three-phase MMC with N half-bridge (HB) SMs in each phase arm. Each HB SM consists of a DC capacitor bank C_{SM} , two complementary IGBTs, and a switch used only to bypass a faulty SM. When an SM is inserted, it contributes to the voltage output of the MMC by supplying its SM capacitor voltage. During normal operating conditions, the output of an SM is

$$V_{SM} = \begin{cases} V_{C_{SM}} & \text{when SM is inserted,} \\ 0 & \text{when SM is bypassed.} \end{cases} \quad (1)$$

The combined voltage of the SMs of the upper and lower arms of a phase at any given instant are represented as v_u and v_l respectively. v_u and v_l are related to the sum of capacitor voltages of the upper and lower arm of that phase as

$$v_u = N_u V_{cu}^\Sigma, \quad (2)$$

$$v_l = N_l V_{cl}^\Sigma, \quad (3)$$

where

$$N_u, N_l \in \left\{ 0, \frac{1}{N}, \frac{2}{N}, \dots, 1 \right\}. \quad (4)$$

N_u and N_l are the upper and lower arm insertion indices, and V_{cu}^Σ and V_{cl}^Σ are the sum of the SM capacitor voltages in the upper and lower arm of that phase. The single-phase equations of an MMC are

$$R_{arm} i_u + L_{arm} \frac{di_u}{dt} = \frac{V_{dc}}{2} - v_o - v_u, \quad (5)$$

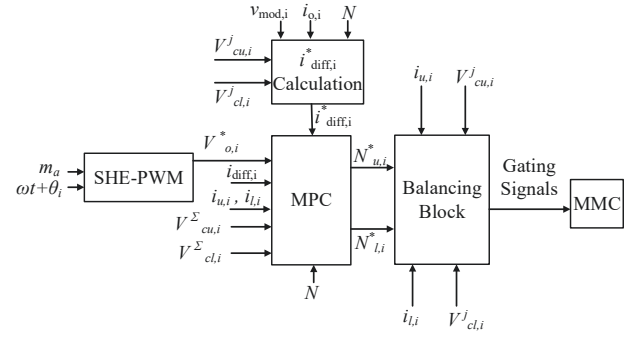


Fig. 2. SHE-PWM MMC controller.

$$R_{arm} i_l + L_{arm} \frac{di_l}{dt} = \frac{V_{dc}}{2} + v_o - v_l, \quad (6)$$

$$i_u = i_{diff} + \frac{i_o}{2}, \quad (7)$$

$$i_l = \frac{i_o}{2} - i_{diff}, \quad (8)$$

where v_o and i_o represent the phase to neutral output voltage and the output current, i_{diff} the circulating current of that phase, V_{dc} the dc linking voltage, v_u , i_u , and v_l , i_l the voltage and current of the upper and lower arms respectively, and L_{arm} , R_{arm} the arm inductance and arm resistance respectively. Substituting (7) and (8) in (5) and (6), the ac and dc dynamic equations are as follows:

$$v_o = -\frac{1}{2} \left(R_{arm} i_o + L_{arm} \frac{di_o}{dt} \right) + \frac{v_l - v_u}{2}, \quad (9)$$

$$V_{dc} = v_u + v_l + 2 \left(R_{arm} i_{diff} + L_{arm} \frac{di_{diff}}{dt} \right). \quad (10)$$

The differential voltage, causing the differential current, is

$$v_{diff} = V_{dc} - v_u - v_l. \quad (11)$$

The full dynamic model of the MMC for phase i is obtained from (2), (3), (10), and (11) as

$$\begin{cases} \frac{di_{diff,i}}{dt} = \frac{1}{2L_{arm}} v_{diff,i} - \frac{R_{arm}}{L_{arm}} i_{diff,i} \\ \frac{dV_{cu,i}^\Sigma}{dt} = \frac{NN_{u,i}}{C_{SM}} i_{u,i} \\ \frac{dV_{cl,i}^\Sigma}{dt} = \frac{NN_{l,i}}{C_{SM}} i_{l,i}, \end{cases} \quad (12)$$

where C_{SM} is the SM capacitance.

MMC control is performed using selective harmonic elimination pulse width modulation (SHE-PWM) proposed in [20]. Fig. 2 shows the MMC controller used for this analysis. It tracks the circulating current reference i_{diff} , maintains the averaged voltage of SM capacitors and limits the i_{diff} ripple.

B. Double-Switch Open Circuit Faults in MMCs

The arm current i_{arm} flowing through a normal SM is

$$i_{\text{arm}} = C_{SM} \frac{\Delta V_{SM}}{\Delta t}. \quad (13)$$

Arm current is positive if it flows in the direction shown in Fig. 1.

The behavior of an SM under a double-switch OC fault is described in Table I. When there is a double-switch OC fault and the arm current is positive, the capacitor charges and the voltage across the SM is $V_{C_{SM}}$. The current flows through the antiparallel diode D1 of the upper IGBT (Fig. 1) and charges the capacitor. This is irrespective of whether the SM is inserted or bypassed as the double-switch OC fault prevents the firing of the IGBTs despite the MMC controller command to fire. For positive arm currents, the faulty SM becomes effectively inserted. When there is a double-switch OC fault and the arm current is negative, the SM is shorted and the voltage across the SM is zero. Hence, the capacitor neither charges nor discharges. The current flows through the antiparallel diode D2 of the lower IGBT effectively bypassing the faulty SM.

Equation (13) can be rearranged as

$$i_{\text{arm}} \frac{\Delta t_1}{C_{SM}} + i_{\text{arm}} \frac{\Delta t_2}{C_{SM}} = \Delta V_{C1} + \Delta V_{C2} = \Delta V_{CT}, \quad (14)$$

where Δt_1 and Δt_2 are the time periods when an SM is effectively inserted and bypassed, ΔV_{C1} and ΔV_{C2} are the changes in net capacitor voltage when the SM is effectively inserted and bypassed. From Table I, it is seen that $\Delta V_{C2} = 0$ as the capacitor neither charges nor discharges during this time and ΔV_{C1} is positive as the capacitor charges during this time making ΔV_{CT} positive and V_{CT} , the capacitor voltage of the faulty SM, to rapidly increase.

TABLE I
SM BEHAVIOR UNDER DOUBLE-SWITCH OC FAULTS

Arm current	SM status	V_{SM}	Capacitor status
positive	inserted	$V_{C_{SM}}$	charging
positive	bypassed	$V_{C_{SM}}$	charging
negative	inserted	0	same
negative	bypassed	0	same

III. PROPOSED SM FAULT DETECTION METHOD

A. SVC-Based Fault Detection Method

The SHE-PWM controller creates a sorted array of SM capacitor voltages for its own computations. The same resource is utilized to perform fault detection. Fig. 3 shows the proposed SVC fault detection method. The method first obtains the array of sorted SM capacitor voltages from the MMC controller of the corresponding phase for one time period. The simulation time step is $50 \mu\text{s}$ and each time period is 0.0167 s (system frequency is 60 Hz). This results in 334 sorted SM capacitor voltage time stamps per time period. Training data is obtained

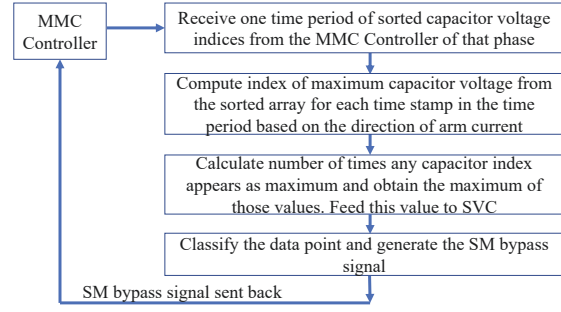


Fig. 3. Proposed SVC fault detection method.

from PSCAD by simulating ten cycles each of normal and faulted operation of SM_1 in the upper arm of phase a . The number of times voltage of the SM considered for training $V_{C_{SM_1}}$ is maximum in every time period is computed. This serves as the training data for the SVC. The training data does not require more than two faulted SM operation time periods as the number of times $V_{C_{SM_1}}$ is maximum in a time period saturates at 334 providing no additional information. Fig. 4 shows the data used to train the SVC.

After receiving one time period (334 time stamps) of sorted capacitor voltage indices from the MMC controller, the proposed method computes the index of maximum capacitor voltage from the sorted array for each time stamp based on the direction of arm current. If the arm current is positive, the array received from the MMC controller is sorted in descending order and the first element of the sorted array provides which SM capacitor has the maximum voltage for that time stamp. If the arm current is negative, the array received from the MMC controller is sorted in ascending order and the last element of the sorted array provides which SM capacitor has the maximum voltage for that time stamp. The proposed method then computes the number of times each SM capacitor voltage is maximum in that time period and the maximum of those values is fed to the SVC. This data point is classified by the SVC as faulty or normal SM operation. Then, the proposed method returns a bypass signal that indicates which SM is faulty. The bypass signal is an array with dimension equalling the number of SMs in the arm of that phase. Each element in the bypass signal array indicates if that particular SM is faulty or not. If an SM is faulty, the bypass signal array returns a value of 1 for the index corresponding to the faulty SM. Let any valid SVC hyperplane classifying the training data (Fig. 5) be denoted by $g(x) = w^T x + b$. The optimal SVC hyperplane classifier is computed by solving for the following expression:

$$\min_w \frac{1}{2} w^T w \quad (15)$$

$$\text{subject to } y_i (w \cdot x_i + b) \geq 1 \quad \forall i,$$

where w and b are the weight and the bias of the SVC and x_i and y_i are the input to the SVC and the output of the SVC.

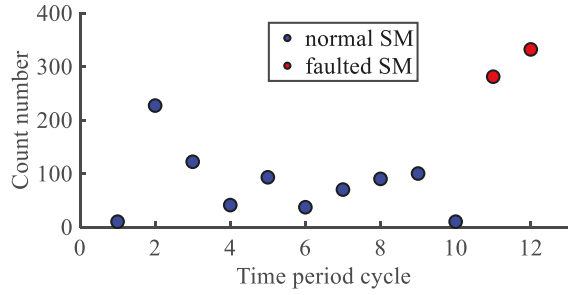


Fig. 4. Number of times $V_{C_{SM1}}$ is maximum in a time period.

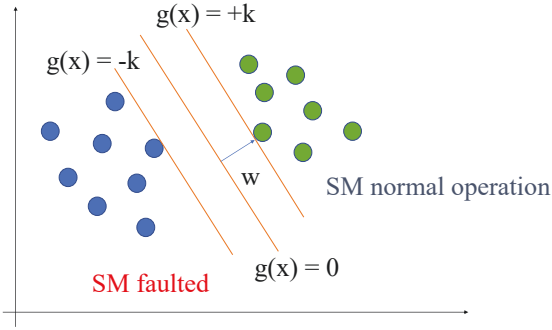


Fig. 5. Classification of sample support vectors using a hyper-plane.

TABLE II
PARAMETERS OF THE MMC FOR SIMULATION

Parameter	Value
Number of SMs in each phase arm N	4
DC-link voltage V_{dc}	10 kV
SM capacitance C_{SM}	4600 μ F
Arm inductance L_{arm}	9 mH
Load resistance R_o	12 Ω
Load inductance L_o	4 mH
Fundamental frequency f_o	60 Hz
Modulation index m_a	0.8
Sampling frequency f_s	2 kHz
Rated V_c for normal operation	2.5 kV

Equation (15) can be expressed in the Lagrangian form as

$$\min_{w,b} J(w,b,\alpha) = \frac{1}{2}w^T w - \sum_{i=1}^N \alpha_i d_i (w^T x_i + b) + \sum_{i=1}^N \alpha_i$$

subject to $\alpha_i \geq 1 \quad \forall i$,

(16)

where the α s represent the Lagrangian multipliers. The lagrangian function J is minimized for w and b and maximized for α . At the optimum, $\frac{dJ}{dw} = 0$ and $\frac{dJ}{db} = 0$. Applying the above conditions to (16), we get

$$w_0 = \sum_{i=1}^N \alpha_i d_i x_i, \quad \sum_{i=1}^N \alpha_i d_i = 0. \quad (17)$$

Equation (17) is substituted into (16), reorganized in the dual form and solved for the lagrangian multipliers using QP optimization. The SVC weight w and bias b values are found to be -1.3 and 1.091 .

IV. PERFORMANCE EVALUATION

To evaluate the performance of the proposed SVC-based SM fault detection method, a detailed model of the three-phase MMC with 4 SMs in each arm is created in PSCAD/EMTDC software. A double-switch OC fault is simulated in SM₃ of the upper arm at time $t = 0.7575$ s. As discussed in Section II, when the arm current is positive, the faulted SM capacitor voltages increases and when the arm current is negative, the faulted SM becomes effectively bypassed and the SM neither charges nor discharges during this time. Thus, the capacitor voltage of the faulted SM increases in a stepwise fashion. Fig. 6(a) validates this behavior in the faulted SM capacitor voltage. The lower arm current reduces by a smaller factor as it supplies the load after the fault of an SM in the upper arm. As the upper arm current is much smaller than the lower arm current, the rate of decrease of capacitor voltages of the upper arm SMs is lower than their lower counterparts. This can be observed in Fig. 6(a).

The SHE-PWM MMC controller maintains the sum of all capacitor voltages to V_{dc} . When capacitor voltage of SM₃, V_{ca3} , increases, the controller tries to reduce the voltage by modifying the PWM signal fed to SM₃. This signal is, however, not processed by the SM due to the double-switch OC fault and its capacitor voltage continues to increase. This leads to a reduction in the voltages of the other SMs to maintain the sum of all voltages to V_{dc} . Increase in V_{ca3} leads to an increase in the net impedance offered by the upper arm resulting in reduced upper arm current, Fig. 6(b).

The double-switch OC fault occurs at SM₃ occurs at $t = 0.7575$ s. The method is able to detect the fault at $t = 0.7575 + 0.0167$ s = 0.7742 s where 0.016 s represents one time period corresponding to the system frequency of 60 Hz, Fig. 6(c).

V. CONCLUSIONS

A comprehensive double-switch OC SM fault detection and localization scheme is proposed in this paper. Capacitor voltages of double-switch OC faulted SMs differ from those of normal SMs. The proposed SVC-based method evaluates these voltage variations for diagnosing and localizing these faults. The sorted capacitor voltages from the controller are utilized eliminating the need for any extra hardware. By being independent of system parameters, the proposed method is immune to parameter uncertainties ensuring high robustness. The proposed method is evaluated through simulation studies conducted in PSCAD/EMTDC, and the results demonstrate that the method works accurately and efficiently.

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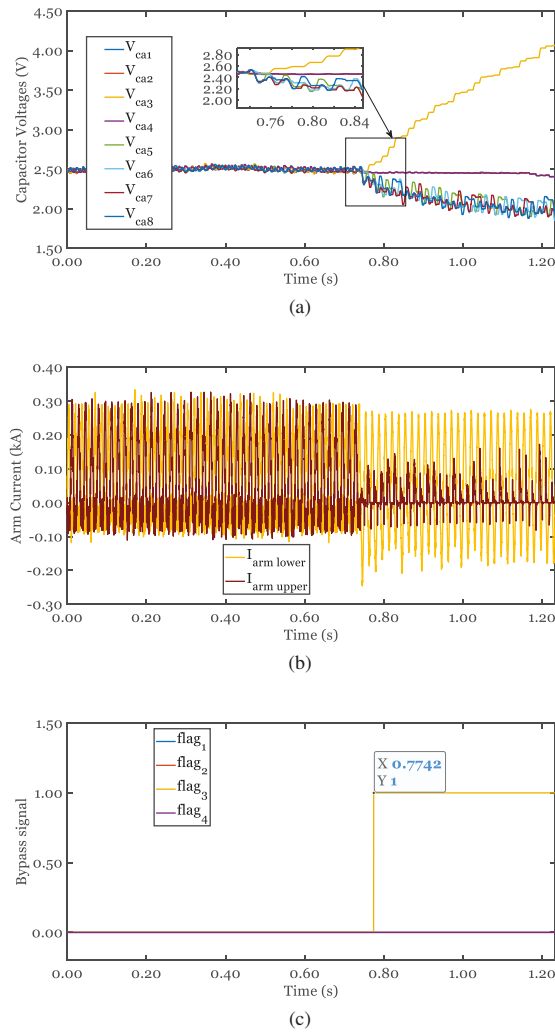


Fig. 6. (a) MMC capacitor voltages during double-switch OC faults, (b) MMC arm currents during double-switch OC faults, and (c) Bypass signal produced by the SVC.

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