A Novel Hybrid GaN/CMOS Rad-Hard DC to DC Converter Module

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***Abstract*— This paper presents a hybrid GaN/CMOS buck converter designed to achieve high efficiency and high conversion ratio, with low profile and high total dose radiation tolerance. This work is based on our previous work with switching frequencies of 4MHz to 15MHz and 88.6% measured peak efficiency with an air-core off-chip inductor. This converter shall provide a load current over 10A and output voltage as low as 1V with an input voltage of 18V. The gate driver and the controller are integrated within a single CMOS integrated circuit (IC). The closed-loop control of the converter is based on voltage mode control. The cascode gate driver is implemented with custom 3.3V enclosed-gate transistors, and employs an asymmetric high-side/low-side driver architecture to minimize losses. The power stage consists of a half-bridge GaN power module with synchronized GaN boot-strap circuits to achieve the maximum power stage efficiency. All power supplies for the controller/driver IC are generated directly from the 18V input with multiple on-chip regulators. Soft-start and undervoltage protection are also included on chip. The CMOS IC is designed in a commercial 0.35um high-voltage bulk CMOS process.**

Keywords—DC-DC buck converter, radiation hardened by design (RHBD), GaN power transistors

I. INTRODUCTION

Recent advancements in power converter applications, such as automotive point-of-load converters (PoL), space power management, and wireless and computational electronics has stimulated the need for light-weight, compact buck converters with high efficiency, high load currents and large step-down conversion ratios. These small form factor, high-efficiency, medium power (10W to 50W) converters are required to support emerging markets. Furthermore, applications in harsh environments, such as in high energy physics (HEP) colliders, demand buck converters with extremely high radiation and magnetic field tolerance. This work mainly targets applications in HEP instrumentation, specifically the planned upgrade of the Large Hadron Collider (LHC), i.e. the High-Luminosity Large Hadron Collider (HL-LHC), at CERN. For this particular application, a rad-hard DC-DC converter with 5-10A current output, >70% conversion efficiency, high magnetic field tolerance (>4 teslas), and ultra-compact size is needed. The radiation hardness requirements include extreme total ionizing dose (TID) levels (>100Mrad) and neutron fluence levels (>1E15n/cm^2, 1MeV equivalent), but this application does not have significant single event threats. Previous publications on radiation hardened buck converters targeting HEP applications report maximum voltage input of 12V and current output of 5A [1] or an improved radiation tolerance with lower conversion ratio and input voltage [2].

The architecture of the authors' first version of the CMOS-GaN hybrid DC-DC buck converter is illustrated in Fig. 1 [3]. The integrated driver/controller IC was implemented in the same 0.35um process that is used for the presented converter. The power stage consisted of discrete GaN power transistors. Design techniques for achieving radiation hardness and small form-factor were addressed in that work. This first version of the hybrid converter prototype was fabricated and measured, and Fig. 2 summarizes the measured efficiencies with various input voltages and output currents at a fixed 4MHz switching frequency. The results show that the converter achieves peak efficiency of 80% for a conversion ratio at 6V input to 1.5V output. The efficiency drops to 71% for a large conversion ratio with 14V input due to increased switching losses.

Section II describes the improved converter architecture (i.e. the second version), including the implemented soft-startup sequence schemes and integrated GaN power module. Section III discusses several innovative circuit techniques that are implemented in the CMOS IC to improve the converter's efficiency and radiation hardness. Customized enclosed gate layout for all 3.3V transistors has been used throughout the chip to ensure its radiation robustness. Section IV presents simulations results. Meanwhile, the CMOS IC has been

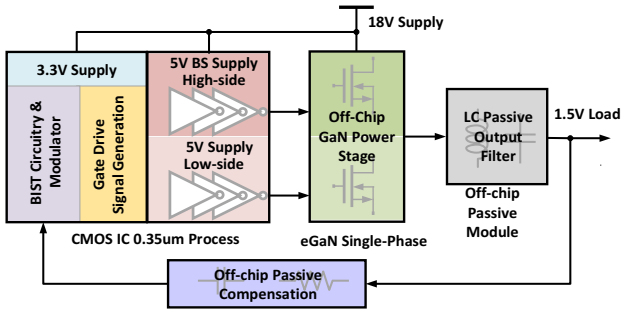

Fig. 1. Block diagram of existing hybrid RHBD GaN/CMOS DC-DC converter.

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integrated with the GaN stages and the new hybrid converter boards are currently undergoing evaluation.

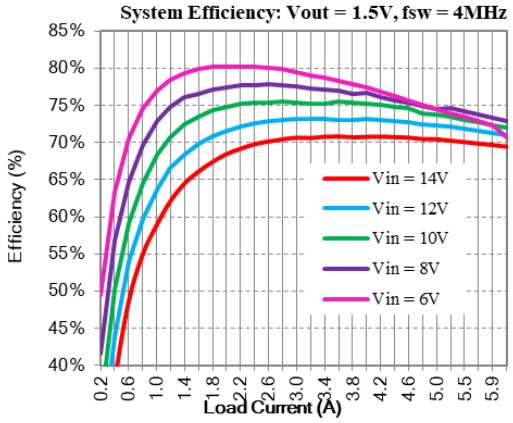

Fig. 2. Measured efficiency of the converter with 1.5V output and 4MHz switching frequencies at different input voltages.

II. Converter Architecture

Fig. 3 shows the detailed schematic diagram of the presented hybrid CMOS/GaN DC-DC buck converter. An EPC2111 half-bridge GaN switch module is used for the power stage, with an EPC2038 synchronous GaN bootstrap architecture [4] [5]. The EPC2111 has a breakdown voltage of 30V and supports 16A continuous current. The sizes for the high and low side devices are optimized for low-duty cycle applications, such as high conversion ratio buck converters. Compared with the conventional passive diode used for the bootstrap supply, the active synchronous GaN bootstrap FET has the advantages of mitigating over-charge of the bootstrap capacitance during the low-side body diode conduction. The EPC2038 has an extremely small form factor (<1mm^2) and input/output capacitances (20/140pC), which is ideal for high-speed switch applications.

The integrated driver and controller IC of Fig. 3 includes fully on-chip voltage references, as well as current bias and voltage regulators. Soft-startup (SS) sequence control is also implemented on-chip. Since the entire converter has only a single high voltage power input, the 5V driver supply and 3.3V controller supply are generated on-chip. There are two voltage regulators. The first one is an 18V-to-5V high-voltage linear regulator to directly provide a power supply with high di/dt current capability for gate drivers. The second voltage regulator is implemented with an 18V-to-5V voltage buffer followed by a 5V-to-3.3V low-voltage dropout regulator (LDO). The 18V-to-5V buffer is essentially a smaller version of 18V-to-5V high-voltage linear regulator, with much lower current sourcing capability provided by a smaller p-type lateral diffusion MOS (LDMOS) passing transistor. A dedicated and intermediate 18V-to-5V regulator for 3.3V power supply is used to avoid the high current spikes of the output driver provided by the 5V high-voltage regulator.

A soft-start sequence is used for the on-chip current biasing, voltage reference, and supply regulation, which is summarized in the flow chart of Fig. 4. The soft-start handles two tasks: 1) power/reference/biasing generation on chip, and 2) soft start sequence for the IC and power stage. In Fig. 4, the red color shows the 18V domain, blue indicates the 5V domain, and green is the 3.3V domain. A coarse voltage is first used to start up initial bias currents for the IC, after which stable 5V and 3.3V supplies are generated. Finally, a precise reference provided by bandgap reference (BGR) ramps up the output voltage.

III. Radhard CMOS IC Circuits

Radhard circuits are employed throughout the IC to enable a CMOS IC that may potentially survive 400Mrad of total ionizing dose (TID). This section presents highlights of the presented (improved) power converter [3].

A. Rardhard Bandgap Reference

A precision voltage provided by a bandgap reference circuit is critical for the operation of the converter since TID-induced threshold voltage shifts is the main source of converter failure in HL-LHC applications. Any mismatch in sensitive transistor pairs in the circuits will directly affect the output voltage and finally push the converter out of stability. One of the most important design considerations is to compensate the threshold voltage mismatch induced by TID throughout the converter's lifetime. This work presents a dynamic threshold MOS

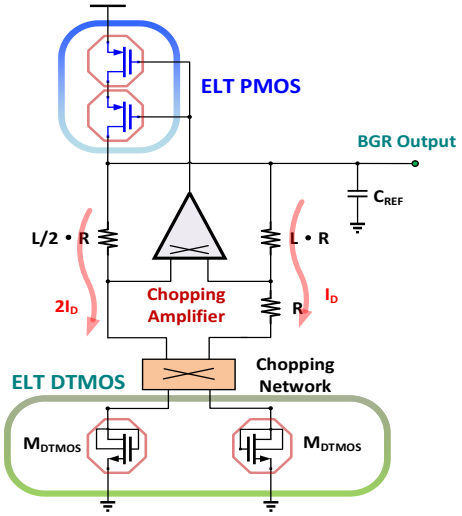

Fig. 5. Block diagram of the DTMOS radhard BGR with chopping stabilization and fully ELT transistors.

(DTMOS)-based radhard voltage reference with chopping stabilization and elimination of conventional PMOS current mirrors, as shown in the block diagram of Fig. 5.

Based the positive and negative temperature coefficient cancellation of a classical BGR structure, this voltage reference circuit employs multiple radhard enhancement techniques, including replacement of the typical PMOS current mirror with a resistive current mirror that uses a single PMOS and the scaled resistors R and R/2. With high TID effects, the threshold mismatch of the conventionally well-matched PMOS pair could be as large as several hundreds of millivolts, as one PMOS could have a 100mV shift while the other has a 300mV shift. The gain of the operational amplifier forces an equal voltage drop across the two resistors, such that the currents through the two branches are scaled by two. Since the matching of this

current mirror does not depend on two transistors but instead depends on two resistors, the PMOS mismatch problems that are present in a conventional current mirror are not present in this architecture. Similarly, unlike typical BGR circuits, the ratioed current density of the two DTMOS are maintained by forcing the resistive ratioed currents into an equally sized device pair, rather than forcing the equivalent current into ratioed transistors. Since the drain voltages of the DTMOS are similar, chopper stabilization, a method of dynamic offset cancellation, is incorporated in both the DTMOS reference devices to average any TID-induced threshold voltage mismatch. The operational amplifier also internally employs choppers at its input devices to cancel static mismatch of its input pair. The use of chopper stabilization does not affect the basic functionality of the circuit. Finally, a resistive trimming network is implemented on both current branches to tweak the balanced voltage output, which may shift from operating temperature or the average shift from the chopper blocks that is induced by the TID radiation.

B. *Trapezoidal Ramp Generator*

The output of the ramp generator provides a stable ramp clock for the comparator to generate appropriate pulse-width modulated (PWM) signals to control the gate drivers. The previous version of the ramp generator used a typical Schmitt trigger-based RC relaxation oscillator; whose output waveform has a triangle-shaped ramp. In order to generate low-duty cycle

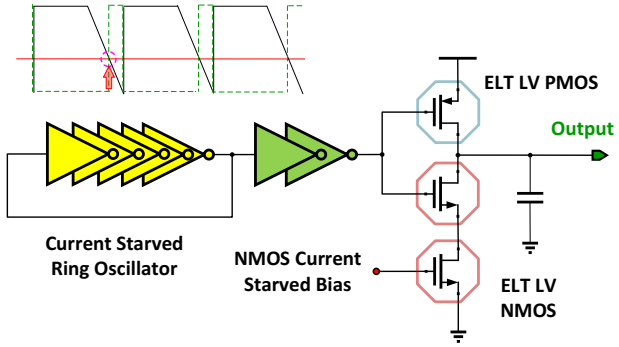

Fig. 6. Block diagram of the trapezoidal ramp generator with optimum comparator input range.

pulses for high conversion ratios, the comparison operation of the comparator was sitting close to its minimum lowest voltage. The presented innovative ramp generator produces a trapezoidal-shaped ramp that allows the voltage comparison to occur near the middle of the comparator's input range, where both transistors of the input differential pair are within their strong saturation region and have maximum gain and fastest response time.

Fig. 6 details the presented ramp generator, which is a current starved ring oscillator followed by a sink current starving capacitor. The trapezoidal waveform at the output is achieved by limiting the sink current, which creates a falling ramp edge from the square-like wave of the proceeding buffer output. The output of the ramp generator has a square wave with 50% duty cycle clock for chopping stabilization and a ramp wave feeding the comparator's input. The oscillating frequency can be tuned by bias current to achieve a range of 2 MHz to 10 MHz.

C. *Peripheral Circuit Blocks*

The error amplifier is one of the most important analog blocks within the controller. Since the amplifier's performance does not tolerate large threshold voltage mismatch in its differential input, the error amplifier employs chopper stabilization. The chopping clock is provided by the ramp generator. Since the switching frequency is of an order of

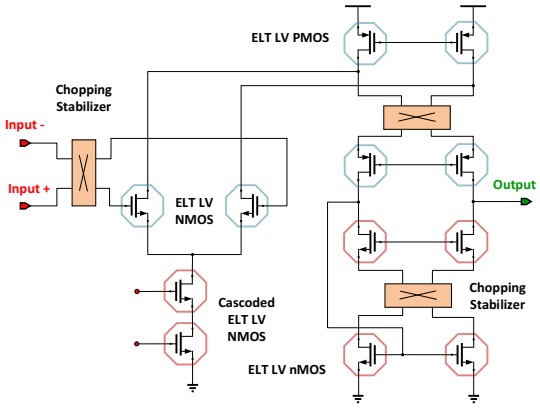

Fig. 7. Block diagram of the radhard chopper amplifier.

magnitude higher than the bandwidth of the compensation network, the chopping spurs are filtered out and do not cause instability in the converter's output. Fig. 7 shows a simplified schematic diagram of the error amplifier, and simulation results demonstrate significant reduction in threshold mismatch of the differential input pair when employing chopper stabilization.

Under-voltage lockout (UVLO) is an important protection circuit for the converter's power stage. The UVLO prevents the IC from providing an output at supply voltages lower than a desired supply threshold. Low supply voltages can generate low-voltage driving signals, which increases conduction loss of the power switches and may quickly damage the power stage. Fig. 8 shows the UVLO circuit employing hysteresis, which forces the converter to turn-on when the gate supply is above 4V and shutdown when it drops below 3.5V.

The outputs of the high-side and low-side power devices have separate sink and source terminals to optimize turn-on and turn-off delay with on-chip resistors. As mentioned above, the low-side driver is about three times wider than the high-side driver because the synchronization conduction loss of the low-side switch is the dominant loss in the power stage for high-conversion ratios. Interleaved sink and source current flow is also used in the driver to minimize parasitic gate inductance by cancellation of mutual parasitic inductance.

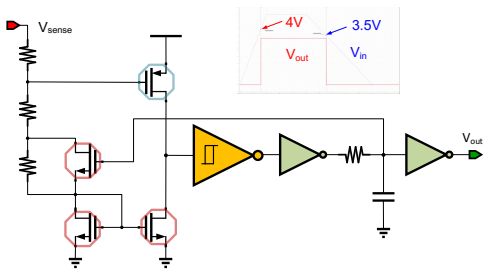

Fig. 8. Block diagram of the UVLO.

IV. CMOS Controller and Driver IC

Fig. 9 highlights the top-level transient simulation of the complete converter, including both controller/driver IC and GaN power stage with off-chip passive components. The converter is supplied with an 18V input, and the 5V supply for the GaN driver and 3.3V for the controller circuits are generated internally with several on-chip voltage regulators. The output inductor is a 500nH commercial air-core inductor. The large inductance will support an inductor ripple current of less than 2A with 1.5MHz switching frequency.

Fig. 9 shows the time between 5.7ms and 5.78ms after the 18V input voltage is applied. The circled area specifically shows the handover of the reference voltage for the error amplifier from the ramped soft-start voltage to the internal stable BGR. The converter is initially powered and controlled by the soft-start sequence, as illustrated in Fig. 4. The top waveforms show that the feedback node of the error amplifier is tracking the switch from the soft-start reference voltage to the BGR. The second row of waveforms shows the comparator outputs based on the closed-loop compensation of the error amplifier, and the third row of waveforms gives the high-side and low-side driver outputs to the GaN power stage. The bottom waveforms plot the inductor ripple current and output voltage. Simulations have verified functionality of the entire converter from initial startup to acquisition of a stable, regulated voltage output of 1V with 6A load current. The simulated steady state power converter efficiency, including the CMOS IC, is above 86%.

Fig. 10 shows the final chip layout in the 0.35um CMOS process with main blocks highlighted. A prototype evaluation board has been designed and fabricated, and measurements are currently in progress. Fig. 11(a) shows the fabricated testing board with the 500nH output inductor. Fig. 11(b) shows the relative sizes of the IC, output air-core inductor and GaN power module, which demonstrates that the complete DC-DC converter can be implemented within the desired low-profile specifications for the HL-HLC.

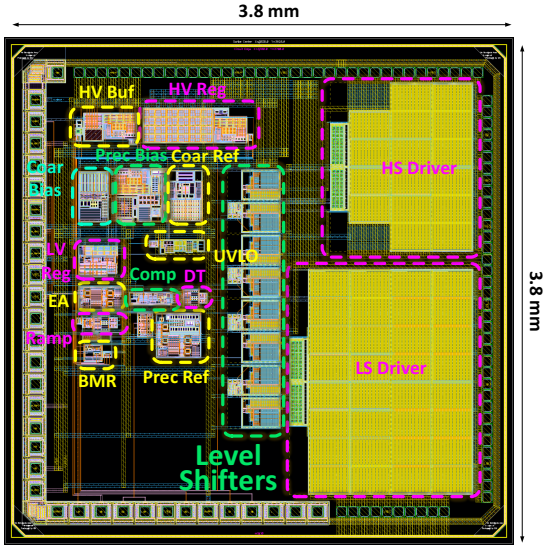

Fig. 10. Layout of the controller plus driver IC.

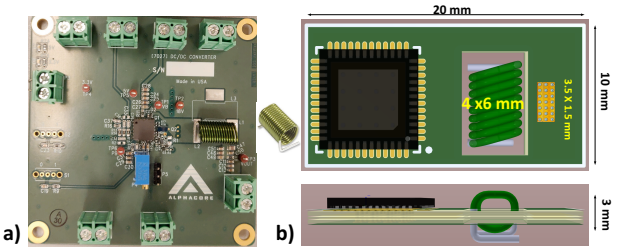

Fig. 11. a) Fabricated testing board with inductor; b) Assembly showing low-profile of the complete DC-DC converter.

V. Conclusion

This work presents a hybrid GaN/CMOS buck converter that is implemented using a custom integrated CMOS driver/controller IC and enhancement-mode GaN power devices. The presented converter is ideal for HEP instrumentation such as the HL-HLC. Several innovative RHBD techniques are used to improve TID performance up to 100Mrad(Si). A half-bridge GaN power module has been selected and its associated power stage has been designed to maximize converter efficiency with 10A of load current.

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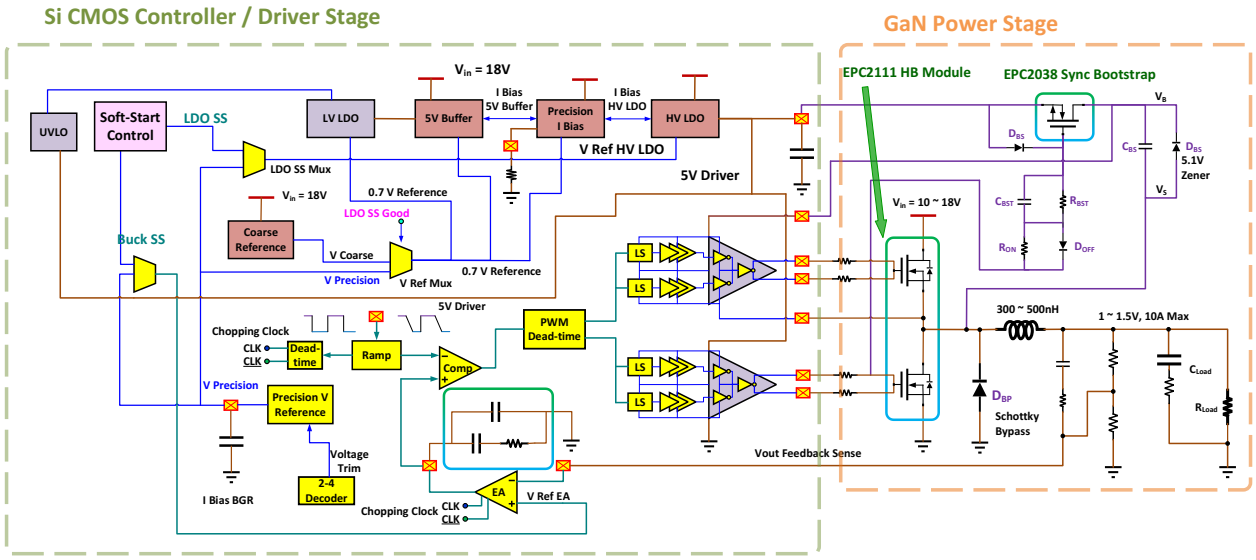

Fig. 3. Schematic block diagram of the presented novel hybrid CMOS/GaN radhard buck converter.

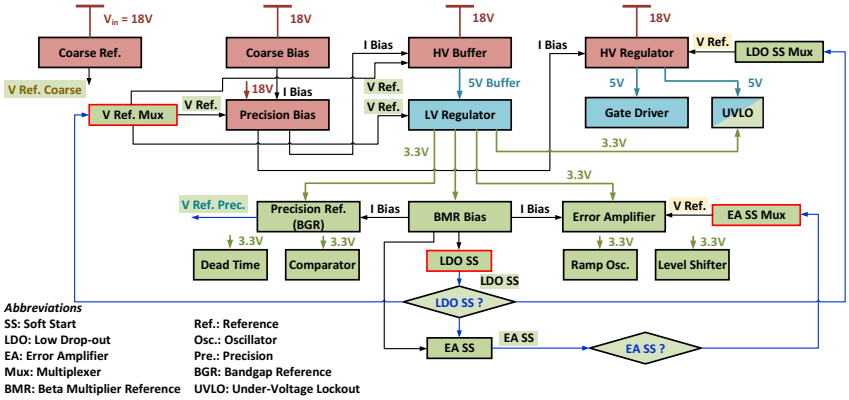

Fig. 4. Flow-chart of the soft-startup sequence of proposed novel hybrid CMOS/GaN radhard buck converter.

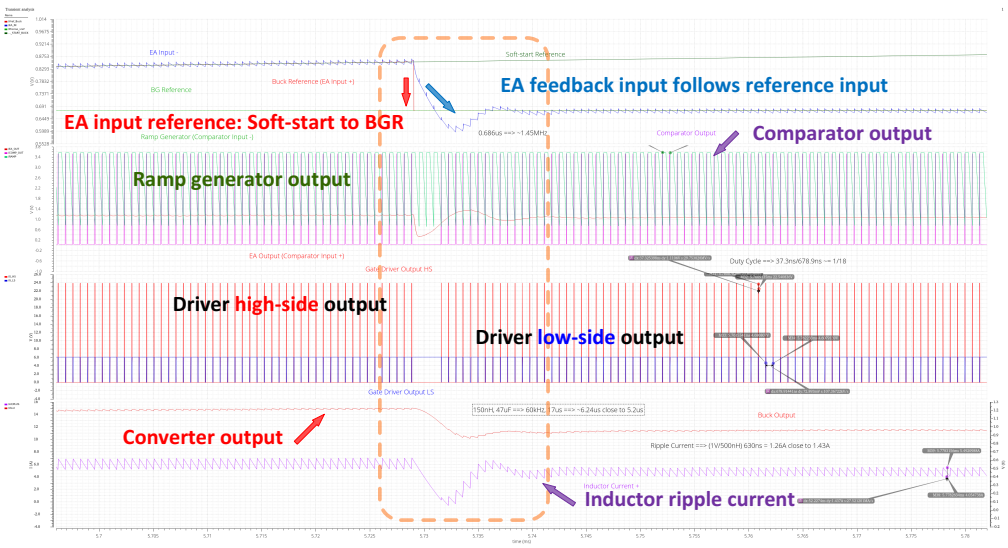

Fig. 9. Simulated outputs showing the soft-startup sequence while the error amplifer's positive input reference is switched from ramp to BGR reference.