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# COMPUTATIONAL DESIGN AND 3D WEAVING OF 2D-PRINTABLE CONFORMAL FLEXIBLE ELECTRONICS USING HARMONIC FOLIATION THEORY

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## ABSTRACT

*This paper proposes a new way of designing and fabricating conformal flexible electronics on free-form surfaces, which can generate woven flexible electronics designs conforming to free-form 3D shapes with 2D printed electronic circuits. Utilizing our recently proposed foliation-based 3D weaving techniques, we can reap unprecedented advantages in conventional 2D electronic printing. The method is based on the foliation theory in differential geometry, which divides a surface into parallel leaves. Given a surface with circuit design, we first calculate a graph-value harmonic map and then create two sets of harmonic foliations perpendicular to each other. As the circuits are processed as the texture on the surface, they are separated and attached to each leaf. The warp and weft threads are then created and manually woven to reconstruct the surface and reconnect the circuits. Notably, The circuits are printed in 2D, which uniquely differentiates the proposed method from others. Compared with costly conformal 3D electronic printing methods requiring 5-axis CNC machines, our method is more reliable, more efficient, and economical. Moreover, the Harmonic foliation theory assures smoothness and orthogonality between every pair of woven yarns, which guarantees the precision of the flexible electronics woven on the surface. The proposed method provides an alternative solution to the design and physical realization of surface electronic textiles for various applications, including wearable electronics, sheet metal craft, architectural designs, and smart woven-composite parts with conformal sensors in the automotive and aerospace industry. The performance of the proposed method is depicted using two examples.*

## 1 INTRODUCTION

Flexible electronics has been an emerging field of research in the past decade. Compared to conventional semiconductor devices, flexible electronics are relatively soft and stretchable. After stretching, it can conform to the curved surface [1] and thus enable various novel applications, such as implantable medical devices [2], wearable electronics [3, 4, 5], flexible displays [6] and soft robots [7, 8]. The rapid development of digital manufacturing has boosted innovations in flexible electronics. The three commonly used methods are inkjet printing [9], laser-induced manufacturing [10], and 3D printing [11] as shown in Figure 1a. Inkjet printing is an efficient method for directly depositing conductive materials on the substrate. The process is relatively low cost and adaptable for large-scale fabrication of circuits, sensors, transistors, etc [9]. For micro-scale electronics printing, an advanced laser-induced method is a powerful tool. With laser beam scanning at a specific power rate, the non-conductive metal films are sintered into electrically conductive patterns [12]. Both the

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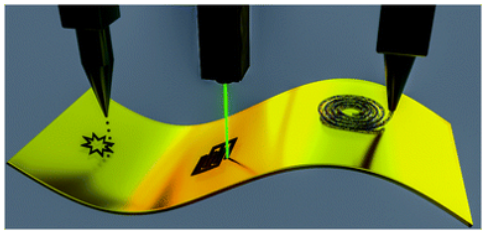
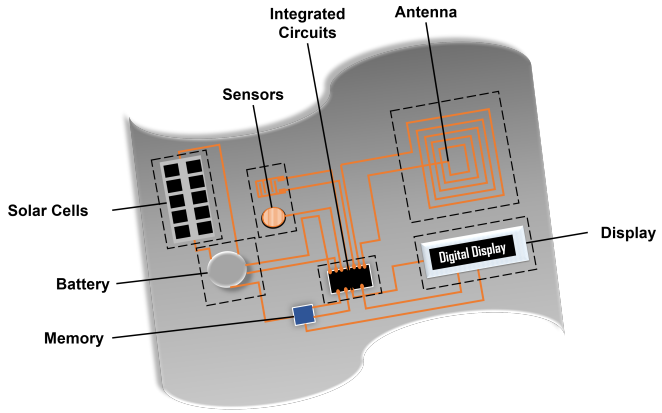


(a) Digital manufacturing of flexible electronics from left to right: inkjet printing, laser scribing, and 3D printing [11].




(b) A schematic of hybrid flexible electronics: a soft substrate with printed circuits, silicon ICs (processor), power supply, etc.

**FIGURE 1**: Manufacturing Strategies and Applications of Flexible Electronics

inkjet printing method and the laser sintering method can only print the electronics in 2D. For fabricating 3D architectures or non-planar electronics, additive manufacturing has become popular [13]. However, conventional planar-layered 3D printing technologies still face challenges, such as limited printable materials [14] or inconsistent print quality [15]. Particularly when printing thin shell structures, efforts for creating very fine tessellations and support structures are required to ensure a successful printing, which slows down the process and introduces a time-consuming removal procedure [14].

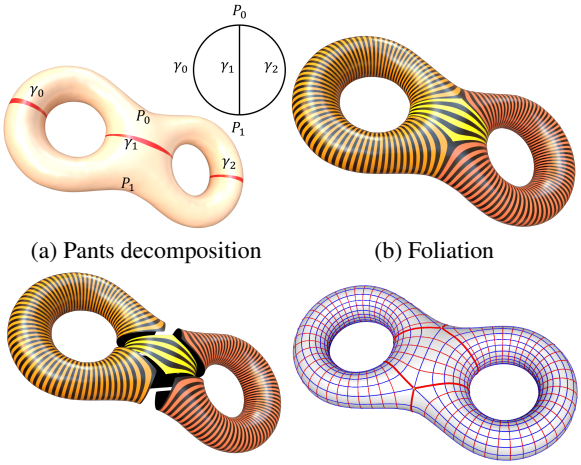
Flexible electronics directly uses a soft material as a substrate and shows its ability to make a complaint and stretchable electronic device. However, in terms of high-performance computing, conventional silicon rigid integrated circuits (ICs) are more efficient [16]. Thus, a compact and flexible hybrid electronics (FHE) system that integrates various electronic components, such as sensors, actuators, energy storage devices, or silicon integrated circuits, have shown a growing demand [2, 17, 18, 5, 16] (Figure 1b is a schematic of a hybrid flexible electronic). A temporary solution is to directly solder the ICs and other rigid components to the flexible substrates and connect them with printed circuits [19]. However, when stretched to conform to a surface, the reliability of the FHE deteriorates. The loading, including bending, shearing, and twisting, can generate considerable stress and damage the bonding at the interface between rigid components and the printed circuits [20, 21].

Another approach is known as E-textiles, which combines conventional textiles with electronic components. They can preserve the advantages of fabrics as flexible and perform functionalities, for instance, interact with the environments or users [22, 23]. E-textile is made by creating an interlocking network of threads, and it can exhibit high strength during severe deformations. Thus, the bonding between the fabric and the ICs increases by integrating the rigid components on plastic strips and involving in the weaving process [24, 25]. Wicaksono *et al.* [25] proposed a method that combined electronic devices with plastic substrates embedded into a knitted textile. Nevertheless, the problem of stretching-induced large strain still exists. Since textiles are made of plain or rolled sheets, when covered onto a curved surface, the fabrics will undergo large deformations [26, 27] or will be cut and sewn. This surface fitting process breaks the fiber continuity, produces defects such as wrinkles or local sliding, damages the mechanical properties, and even causes failures such as splitting or delamination [28, 29, 30]. As a result, the trend toward direct fabricating to form a surface becomes evident [31, 23].

Inspired by traditional woven fabrics, a flexible electronics constructing method conforming to free-form surfaces by weaving is proposed to tackle the barriers mentioned above. Woven fabrics are the textiles formed by interlacing two sets of threads at right angles [32]. Due to the advantages, including lightweight, economy, and ease of implementation, woven material has been used widely in the clothing industry [33, 34, 35, 36, 37]. The method is based on our earlier work, the so-called 3D weaving technique [38], which can directly form a surface by intertwining two series of strips. In detail, we first calculate two families of orthogonal foliations on a given surface using the Harmonic foliation theory. Then, a quadrilateral mesh is generated, and each quad is regarded as a woven cell. By separating the Quad-mesh into two group strips, flatten them in planar, and cutting out the strips on the physical material, we obtain two orthogonal groups of weaving threads and intertwine them to reconstruct the surface.

The 3D weaving method is an ideal solution to the fabrication of conformal FHE for two reasons. First, because the weaving strips are generated in a plane, they can easily be combined with other mature 2D electronic manufacturing methods, such as inkjet printing and laser sintering. Second, the flexible electronics are directly shaped during weaving. The post-processing process of deforming the woven surface to conform it to the target surface is omitted. Consequently, the stretching-induced strain is prevented.

The rest of the paper is structured as follows: Section 2 provides a brief description of the computational method for the




(a) Pants decomposition (b) Foliation

(c) Cylindrical decomposition (d) Quadrilateral remeshing

**FIGURE 2**: Foliation Generation Pipeline.

(a) Quad-mesh (b) Strip generation (c)Unfolded strips

**FIGURE 3**: Strip Generation on a C Shape Surface

proposed 3D weaving techniques. Section 3 first presents two examples: an LED circuit on a hemispherical surface and a human face surface with 2D-printed conformal circuits. Then the manufacturing considerations are discussed. Section 4 concludes the work, discusses the contributions, and outlines the future development.

## 2 COMPUTATIONAL METHOD OF 3D WEAVING

The foliation theory is applied in this work to compute the woven threads on arbitrary surfaces. We first summarize the steps as follows and then explain them in the corresponding sections.

1. Two families of orthogonal foliations are calculated on a given surface (section 2.1, 2.1.1, 2.1.2). Then we decompose the surface into topological cylinders based on the foliation results 2.1.3.
2. A quadrilateral mesh is computed to cover each of the cylinders (section 2.1.4).
3. From the quad-mesh, we horizontally/vertically cluster the unit cells into strips and unfold them onto the 2D plane. By cutting the strips out on physical materials, e.g., construction paper, we get two orthogonal groups of weaving threads (section 2.2).
4. By interlacing the warp and weft threads in a particular order (such as plain weaving or twill), we can obtain a woven structure that is conformal to the input surface.

### 2.1 Theory of Harmonic Foliation

According to the definition of topological foliation, a foliation can tile a surface by infinitely many parallel curved leaves. Specifically, a leaf is a curve on the surface, either a closed-loop or an infinite spiral.

In this work, the foliation is induced by a harmonic map, which guarantees the smoothness of foliation. Once calculate a foliation, the corresponding orthogonal foliation can be found. The algorithm for a high genus closed surface is shown in Algorithm. 1 to demonstrate the process. A complete theory on the computational generation of foliations on more general cases can be found in the paper [38]. The main procedures include pants decomposition, generalized Harmonic map, cylindrical decomposition, and quadrilateral remeshing.

**2.1.1 Pants Decomposition** In Figure 2a, we demonstrate the pants decomposition step, which slices the surface to topological spheres [39]. A pants decomposition can be represented as a graph $G$, the so-called *pants decomposition graph*, where each pair of pants $P_i$ is represented as a node $n_i$, and each cutting loop $\gamma_j$ is denoted by an edge $e_j$. Suppose on the surface $S$, the cutting loop $\gamma_i$ is shared by two pairs of pants $P_j, P_k$, then in the graph $G$, the arc of $e_i$ connects nodes of $n_j$ and $n_k$. Furthermore, we associate a positive weight $h_i > 0$ for each edge $e_i$ in the pants decomposition graph. We use $(G, \mathbf{h})$ to denote the pants decomposition graph $G$ with the weights $\mathbf{h} = (h_1, h_2, \cdots, h_{3g-3})$, and call it the *weighted pants decomposition graph*. Later, the weights can be used to adjust the strip widths.

**2.1.2 Harmonic Map** As shown in Figure 2b, the second step is to compute a foliation based on a harmonic map between the surface and the weighted pants decomposition graph $(G, \mathbf{h})$.

The weighted pants decomposition graph $(G, \mathbf{h})$ can be treated as a *metric space*, where the distance between two points $p, q \in G$ is defined as the length of the shortest path connecting them, and denoted as $d_{\mathbf{h}}(p, q)$.

Given a mapping $f : (S, \mathbf{g}) \to (G, \mathbf{h})$, the pre-image of a node

is called a *critical leaf*, and the union of critical leaves is called the *critical graph*, denoted as $\Gamma \subset S$. In general, the critical graph is of 0 measure, then we can define the *harmonic energy* of the mapping $f$,

$$E(f) := \int_{S \setminus \Gamma} |\nabla_{\mathbf{g}} f|^2 dA_{\mathbf{g}}. \tag{1}$$

If $f$ minimizes the harmonic energy, then $f$ is called a *harmonic map*. Wolf [40] proved the existence and the uniqueness of the harmonic map. The preimage of each non-node point is a closed loop on the original surface. All such closed loops compose a foliation $\mathscr{F}$. The Ribbon graph of the foliation $\mathscr{F}$ is exactly $(G, \mathbf{h})$.

**2.1.3 Cylindrical Decomposition** As shown in Figure 2c, the preimages of the nodes form the critical graph $\Gamma$, the surface is sliced along $\Gamma$ and decomposed into $3g-3$ topological cylinders. Different cylinders are rendered using different colors, all the leaves within one cylinder are homotopic to each other.

For each edge $e_i \in G$, its preimage is a cylinder $C_i$. The restriction of the harmonic map on the cylinder $C_i$, $f_i := f|_{C_i}$, can be treated as a harmonic function, $f_i : C_i \to [0, h_i]$. The gradient of $f_i$ can be expressed explicitly. Suppose a face $[v_p, v_q, v_r]$ is in the cylinder $C_i$, the gradient of the piece-wise linear map $f_i$ on this face is

$$\nabla f_i := \mathbf{n} \times (f_i(v_r)(v_q - v_p) + f_i(v_p)(v_r - v_q) + f_i(v_q)(v_p - v_r))$$

where $\mathbf{n}$ is the normal to the face, by abusing the symbols, $v_r$ represents the position of the vertex $v_r$. The *Hodge star* operator is defined as

$${}^{\star}\nabla f_i := \mathbf{n} \times \nabla f_i.$$

When the mesh triangulation is refined enough, the integration lines of the vector field ${}^{\star}\nabla f_i$ give the so-called *conjugate foliation* $\mathscr{F}^{\star}$ that is orthogonal to the original foliation $\mathscr{F}$. According to [41] the conjugate foliation $\mathscr{F}^{\star}$ itself is harmonic as well. The conjugate foliation is depicted in Figure 2 frame (d), whose leaves are the blue loops.

**2.1.4 Quadrilateral remeshing** Figure 2 frame (d) illustrates the quadrilateral remeshing step. Basically, given a pair of conjugate foliations $\{\mathscr{F}, \mathscr{F}^{\star}\}$, we can collecting some leaves to form a quadrilateral tessellation of the surface. The weft and warp strips are mapped to red and blue loops on the surface respectively. As shown in Figure 2, the red/blue leaves are orthogonal, and the quadrialteral cells are similar to squares. Moreover, the user can specify density of the planar regular grid in order to determine the resolution of the quadrilateral mesh on surface; since each of the quadrilaterals represents a woven unit cell, the accuracy and scale of the woven surface can be adjusted accordingly.

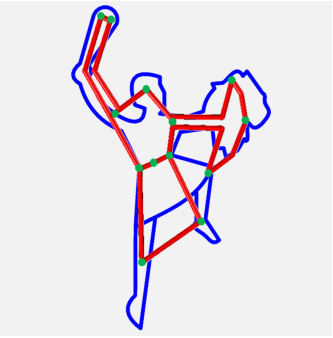
**Algorithm 1: Surface Foliation Algorithm for Close Surface.**

**Input :** A closed surface $\mathscr{S}$ with genus $g > 1$ and a threshold $\varepsilon$
**Output:** A foliation $\mathscr{F}$ of $\mathscr{S}$
Construct a pants decomposition of $\mathscr{S}$;
Construct the pants decomposition graph $G$, assign the edge weight $\mathbf{h}$ to $G$;
Construct an initial map $f : \mathscr{S} \to G$ by mapping each pair of pants to the corresponding node;
Compute the initial harmonic energy $E$;
**while** *true* **do**
  $E_0 \leftarrow E$;
  **foreach** *vertex* $v_i \in \mathscr{S}$ **do**
    $f(v_i) \leftarrow \operatorname{argmin}_{q \in G} \sum_{j=1}^{n} \omega_{ij} d_{\mathbf{h}}(f(v_j), q)^2$;
  Calculate the harmonic energy $E$;
  **if** $|E - E_0| < \varepsilon$ **then**
    break;
**foreach** $p \in G$ **do**
  Compute the leaf $f^{-1}(p) \in \mathscr{S}$;
Return the foliation $\mathscr{F}$ consisting of all leaves;

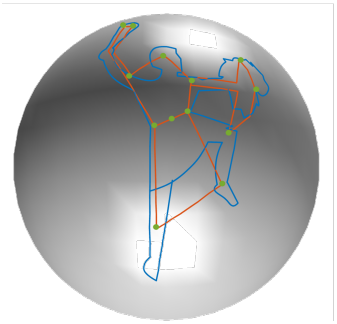
## 2.2 Strip Generation

The input surface is represented as a triangular mesh, which is converted into a quadrilateral mesh using the obtained foliation. First, the vertex positions are sampled on the triangular mesh where a horizontal trajectory intersects a vertical trajectory. Next, the vertices are connected by edges by tracing the horizontal and vertical trajectories. Then, the vertices are optimized to ensure each quadrilateral face is planar using the method introduced in [42]. The edges are divided into horizontal and vertical edges. Quad faces are connected by horizontal edges to form vertical strips and by vertical edges to form horizontal strips. We computationally cut them along vertical edges or horizontal edges. All the strips can be isometrically embedded onto the plane. The horizontal and vertical bands overlap one the other, and the two layers cover the entire surface. This procedure is called unfolding.

Once the strips are digitally generated and unfolded, we can pack them together to fill a planar material. Here, we use construction paper as an example. By cutting out the strips manually with scissors or automatically with a cutting machine, we can physically get the two groups of pieces for weaving. In practical



(a) Original 2D Pattern of the Orion constellation



(b) Conformal mapping 2D Pattern to a 3D Hemisphere

**FIGURE 4**: Original 2D Orion Constellation Pattern and the Conformally Mapped Pattern on Hemisphere

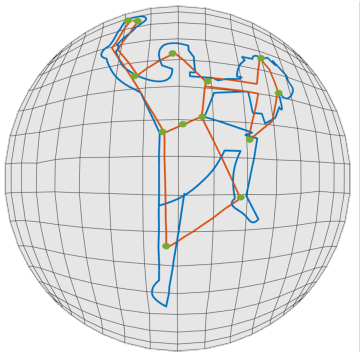


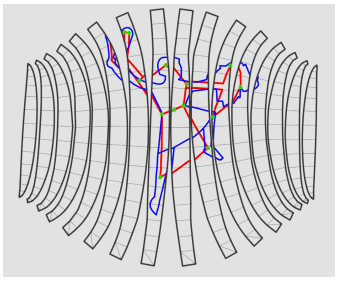
**FIGURE 5**: The Conformal Orion Constellation Pattern on a 3D Hemisphere Discretized by Harmonic Foliation.

weaving, the horizontal and vertical strips function as weft and warp yarns, respectively.

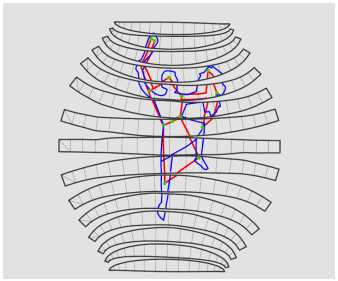
## 3 FABRICATION OF CONFORMAL FLEXIBLE ELECTRONICS

### 3.1 LED Circuit on a Hemisphere Surface

In this example, we apply the algorithm mentioned above to weave and assign the LED circuits on a hemisphere surface. The original design is an Orion constellation as shown in Figure 4a. The blue lines are the contour of the Orion constellation. The green spots represent the 13 stars and are linked by the red lines to show the constellation's outline. Given that the original design is in 2D, we conformally map this 2D design to the hemispherical surface, as shown in Figure 4b. This step can be skipped if the original design is already on the surface. The design is considered as textures and mapped to a hemisphere during the calculation of the foliations and the generation of strips. Figure 5 shows the quad mesh result after the calculation of the harmonic



(a) Weft strips



(b) Warp strips

**FIGURE 6**: Computer-Generated Woven strips for the Orion Constellation Design.

(a) Weft strips

(b) Warp strips

**FIGURE 7**: Woven strips Made by a Desktop Electronic Cutter

foliation. The mesh size is $15\times$ 16. Later, we apply the strip generation and unfold the two groups of weaving strips as shown in Figure 6. The pattern of the Orion constellation is separated into the corresponding individual woven unit cell.

We use a desktop electronic cutter (Silhouette Curio) to make the strips on transparent paper. The cutter can print/cut various materials, such as paper, plastic, cloth, metal, and wooden boards. The maximum workspace is $8.5 \times 12$ inches. The size of the paper is $8.5 \times 11$ inches. Marker pens of different colors trace the Orion constellation design, and then the strips are cut out along the boundaries. To install the LED lights, we use the cutting machine to punch holes at the green spots. Figure 7 shows the two groups of weaving strips fabricated. Figure 8 shows how the strips are interwoven to form the surface. After constructing the surface, we install the LED lights into each of the pre-punched holes and use conductive copper tape to connect them. The final results are shown in Figure 9, where the LED lights are linked by parallel electric circuits. Two $3V$ battery cells are used as power supply. Turn on the switch and the woven surface will be lighted up, as shown in Figure 10.

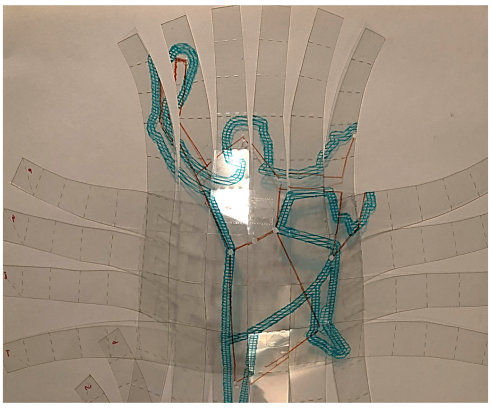


**FIGURE 8**: The Weaving Process of the Orion Constellation Model

### 3.2 Conformal Flexible Electronics on a Human Face Surface with Printed Circuit

In the previous example, we have shown the capability of our method in weaving a surface with circuits. To demonstrate the generality of the proposed method, we apply the technique to make a human facial surface with high curvature spots. Besides, the circuit is printed in 2D using silver-based conductive ink. The waving process is the same as the previous Orion constellation model. Figure 11a shows the circuits distribution on human surface model under quad mesh. The size of the quad mesh is $15 \times 16$. The paper size is $8.25 \times 11.75$ inches. Figure 12 shows the manufactured strips. The black lines represent the boundary of each weaving unit, and the silver lines are the printed circuits.

By adopting the idea of conventional weaving, a variety of weave architectures can be achieved by intertwining the warp and weft threads in different orders. The most common weaving pattern is the aforesaid plain weaving where each warp thread passes up-and-down each weft thread. Visually, objects constructed by plain weaving have a checkerboard-like appearance. The plain weaving creates the maximum amount of interlacing area, providing the most reinforcement to the surface. As shown in Figure 11, by plain weaving the weft and warp strips, the woven surface shows the checkerboard pattern.

### 3.3 DISCUSSION ON MANUFACTURING CONSIDERATION

To ensure the connectivity of the circuits. We propose an 'offset folding' strategy to increase the contact area of the printed wire lines on the intermission edges.

Figure 13 is a schematic of a four-by-four woven rectangular plane to demonstrate the 'offset folding' technique. The yellow lines represent the original circuits. The rusty red lines are the offset circuits that are folded toward the backside on each strip. Taking the second column of Figure 13 as an example (Figure 14), the detailed steps are: First, detect the woven units $n$ which the circuits pass through. Next, manually add offset zones $\delta z$ on the edges of $n$ and taking the original boundaries as mirror planes to mirror the circuits. Finally, fold the strip along the original boundaries (the hidden lines in Figure 14a) and weave with other strips as normal. From the front, the strip looks the same as the original design. The offset circuits printed near the edges link to the adjacent woven cells on the back. Figure 14b shows the front and back views of the strip after folding.

We test the method by weaving the pattern with construction paper as shown in Figure 15a. The circuits are made using copper strips. Notably, offset zones exist at each edge where the circuits go through and are folded on the back. The offset zones are represented as rust-red lines in Figure 13. With a 3V battery, the woven circuits can successfully light up an LED light as shown in Figure 15b, which shows the effectiveness of our proposed 'offset folding' method to guarantee the circuit connectivity.

In the current stage, the step for adding offset zones is done manually. Later, we will include this procedure in the computation algorithm to automate the process and improve efficiency.

## 4 CONCLUSIONS AND DISCUSSION

In this work, we apply the mathematical theories of foliation to the design and fabrication of conformal flexible electronics. By interlacing two sets of threads, we can weave a 3D flexible electronics surface with arbitrary typologies.

Contributions from this framework can be summarized as follows:

1. This paper proposes a systematic solution to the physical realization of the conformal woven flexible electronics. Computationally, the method is general in geometries and scales. A surface with arbitrary topology can be created by interweaving two sets of threads generated by our algorithm. The size of the woven strips is adjustable according to the accuracy and dimension of the applications.
2. From the manufacturing perspective, the proposed method provides a new solution to the physical realization of conformal textiles with 2D printable circuits. Compared with costly 3D electronic printing methods, our approach is more reliable, efficient, and economical. Moreover, the free-form surface can be shaped directly during the weaving process. The conventional indirect procedures need to prefabricate the flexible electronics on soft substrate and then deform the planar flexible electronics to conform it to the surface.
3. From a mathematical standpoint, the weaving structure generated by our method has the least number of singularities, which increases the mechanical strength and, at the same

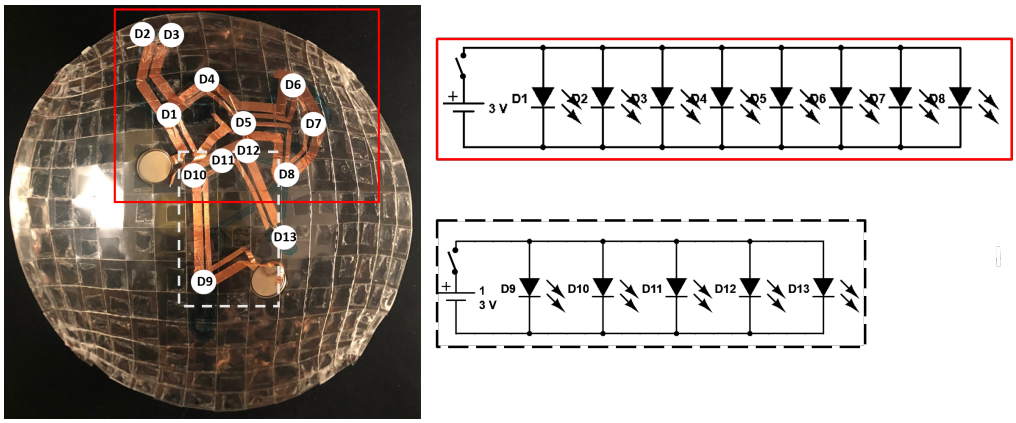



**FIGURE 9**: Circuits design: Left-Circuit on Hemisphere; Right: the Equivalent Circuits

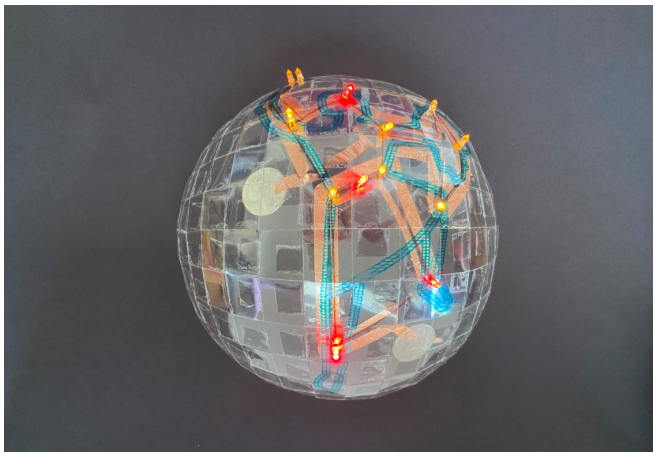
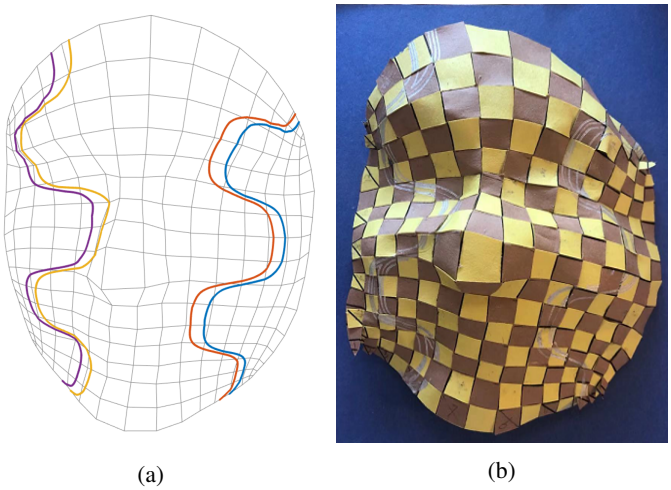
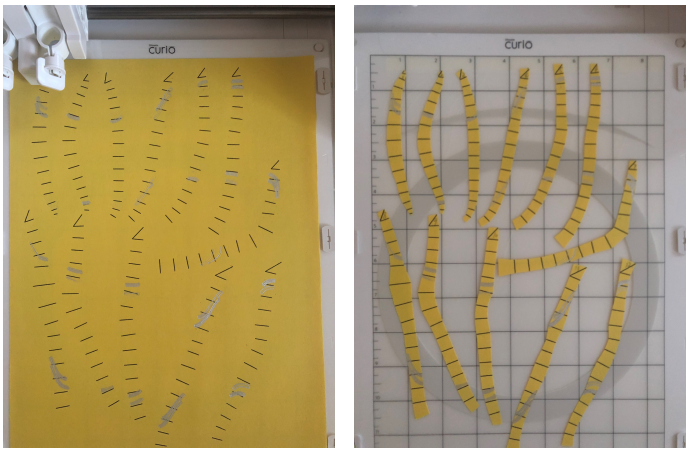


**FIGURE 10**: Lighting Effects



(a) (b)

**FIGURE 11**: Computational generated woven strips of the human face model with circuits




(a) (b)

**FIGURE 12**: Manufacturing the weaving strips of the human face model

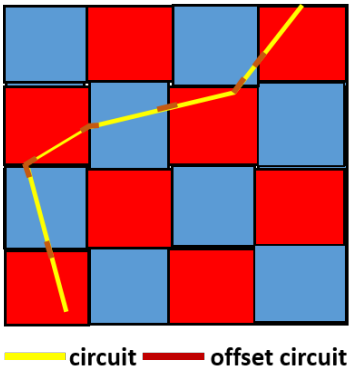
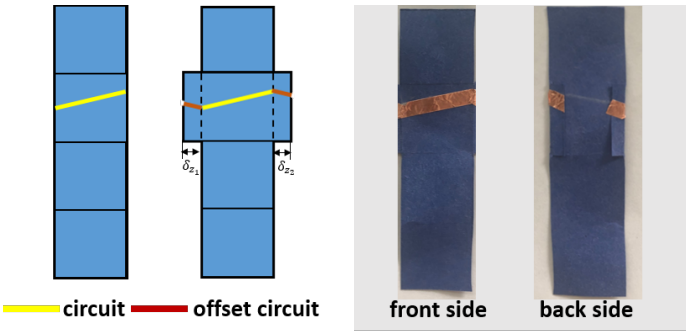


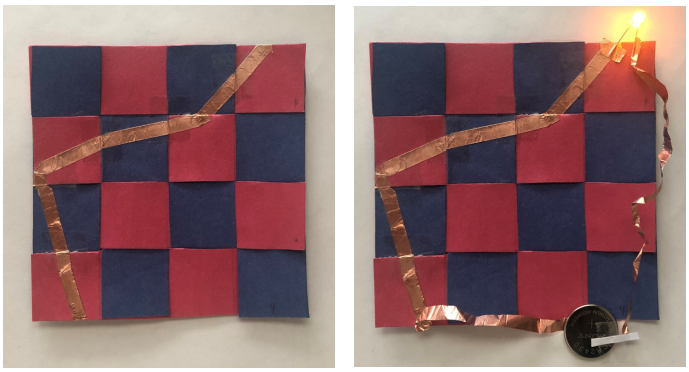

**FIGURE 13**: The schematic of woven flexible electronic surface with offset zones




(a) Adding Offset Zones to the Edges

(b) Strip after Folding the Offset Zones

**FIGURE 14**: Steps for Adding and Folding the Offset Zones



(a) (b)

**FIGURE 15**: Experiment Validation of the Offset Folding Method to Guarantee Circuit Connectivity

time, reduces the complexity of the assembly.

Our current focus is on macro-scale conformal woven fabrics. We have demonstrated our idea by weaving two models using construction paper and conductive material, including copper tape and silver-based conductive pens. In the future, the method can be applied to develop meso-scale flexible integrated electronics, which comprises multiple components such as sensing, actuation, data transmission and analysis, and energy sources. Moreover, combining with our proposed topology optimization framework-the extended level set method [43, 44, 45], we can offer a systematic solution from designing and fabricating structures on a surface with optimized properties and performance.

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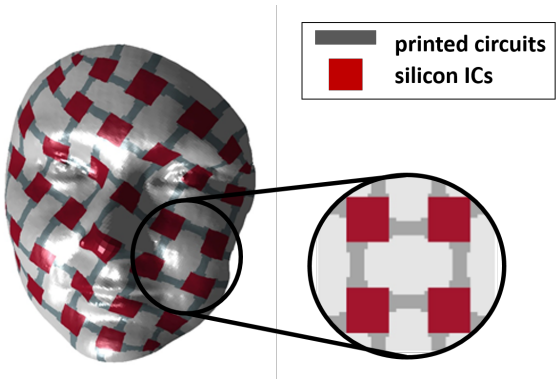


**FIGURE 16**: A schematic of a integrated flexible electronic design on human surface

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