Maintaining Atomically Smooth GaAs Surfaces After High-Temperature Processing for Precise Interdiffusion Analysis and Materials Engineering

Leonid Miroshnik[1], Brian D. Rummel[2], Andrew Li[4], Ganesh Balakrishnan[3], Talid Sinno[4] and Sang M. Han[1,2,3‡] (meister@unm.edu)

[1]Chemical & Biological Engineering, University of New Mexico, Albuquerque, New Mexico 87131, USA

[2]Nanoscience & Microsystems Engineering, University of New Mexico, Albuquerque, New Mexico 87131, USA

[3]Center for High Technology Materials, University of New Mexico, Albuquerque, New Mexico 87106, USA

[4]Chemical & Biomolecular Engineering, University of Pennsylvania, Philadelphia, Pennsylvania 19146, USA

Abstract: Arsenic's high vapor pressure leads to thermal instability during high-temperature processing of GaAs, contributing to the performance degradation of subsequently fabricated devices. The resulting surface damage also obfuscates the exact quantitative characterization of the diffusion process, a critical step in device manufacturing. In this experiment, an encapsulant-and-sacrificial-layer procedure is employed to reduce arsenic sublimation and preserve a smooth surface. A capped GaAs/InGaAs/GaAs quantum well structure is subjected to rapid thermal annealing, and AFM, SEM, and EDS are used to compare the surface qualities of the post-annealed encapsulated GaAs against the reference GaAs. For the encapsulated substrate, a smooth surface with an average root-mean-squared value of 6.5 Å is achieved after high-temperature processing. SIMS analysis is used to obtain the diffused indium atomic concentration profiles for a smooth and roughened GaAs surface and their corresponding diffusion parameters. The analysis demonstrates how precise diffusion parameter extraction requires preserving an atomically-smooth surface in semiconductor diffusion characterization.

Introduction

Thermal decomposition of III-V semiconductors occurs at temperatures well below typical thermal processing and molecular beam epitaxy (MBE) growth temperatures[1,2]. Group V elements are significantly more volatile than their group III counterparts[3,4], and their sublimation during high-temperature processing reduces device performance[5–7]. In gallium arsenide (GaAs), arsenic begins to sublime from the surface at temperatures as low as 370 °C[3]. The material loss from the surface causes roughening and eventually introduces cracks and holes if the substrate is kept at elevated temperatures for extended periods of time[7–9]. Surface damage from high-temperature processing requires additional post-processing steps to reuse the substrate or restore the surface, such that the process can continue[10,11].

Damage to the substrate surface is not the only obstacle posed by thermal processing. A significant step in compound semiconductor device manufacturing is thermal diffusion to tune bandgaps for specific device applications. Many studies in III-V materials have tried to elucidate the mechanisms for interdiffusion, but results are difficult to reproduce because of sensitive or ill-defined experimental setups and uncertain diffusion boundary conditions[12]. Moreover,

interdiffusion studies with GaAs are typically carried out at temperatures well above the initial decomposition temperature[13]. The sublimation of arsenic from the surface and the morphological change of the GaAs structure results in significant uncertainties in reported Arrhenius diffusion parameters, such as the preexponential factor and the activation energy. This result is illustrated by an enormous range of estimated diffusion parameters[12,13]. Gallium arsenide annealing experiments have been conducted in arsenic overpressure environments; however, the analyses are performed over a limited range of experimental conditions with conflicting results[14–16]. Including an arsenic overpressure in an annealing process modifies native defect concentrations on and near the surface, affecting the diffusion parameters[17]. This unpredictability inhibits meaningful analysis of any underlying diffusion mechanisms that could be present.

Beyond affecting the diffusion process, characterization processes are further complicated by the changes in surface morphology. Typical analytical methods for measuring compositional changes and diffusivity in semiconductors are photoluminescence spectroscopy (PL), and X-ray diffraction (XRD). In PL, surface roughness causes an increase in peak broadening[18,19] and peak shifts[20]. For XRD, surface roughness leads to peak broadening and changes in intensity[21,22]. Secondary ion mass spectroscopy (SIMS) is used for high-resolution compositional and spatial analysis. The sample roughness limits the depth profiling SIMS resolution[23] and introduces peak broadening[24,25].

Preventing the loss of arsenic from the GaAs surface mitigates the significant obstacles associated with the high-temperature processing of GaAs. In our study, silicon nitride (Si_xN_y) capping layers are used to protect the sample from arsenic loss and large-scale surface degradation. Limited surface degradation can still occur due to an imperfect Si_xN_y encapsulant and mismatch in thermal expansion coefficients. For this reason, we deposit an aluminum gallium arsenide (AlGaAs) sacrificial layer, which is easily removed after the annealing process using an acid etch. We show that combining these two techniques, referred to as the encapsulated and sacrificial layer (ESL) method, reduces arsenic sublimation-related damage and enables high-resolution compositional analysis for diffusion parameter estimation.

Experiment Description

A GaAs/InGaAs/GaAs quantum well (QW) structure is grown to study the diffusion of indium in GaAs while employing the ESL method. A Vacuum Generators V80 elemental source MBE is used to grow the structure shown in Fig. 1(a). To grow the initial structure, an epi-ready 2-inch GaAs(100) substrate, labeled as s-GaAs in Fig. 1(a), is placed into an MBE, where the wafer undergoes surface contaminant removal at 350 °C for 20 minutes and oxide desorption for 15 minutes at a surface temperature of 615 °C as measured by pyrometry. A valved arsenic cracker source (VACS) is opened once the substrate reaches 350 °C to provide a flux of arsenic to the surface of the wafer to replace the evaporating arsenic and preserve the smooth surface for growth. A GaAs smoothing layer of 200 nm is grown at a substrate temperature of 580 °C. An indium gallium arsenide (InGaAs) quantum well is grown at 480 °C. The atomic composition of the group III elements in the InGaAs layer is measured to be 19% indium and 81% gallium with a quantum well thickness of 7.7 nm with a Malvern PANalytical Empyrean XRD. A square well and constant composition fully strained model is used to fit the InGaAs layer composition with the PANalytical Epitaxy and Smoothfit software. The GaAs capping layer is grown to a thickness of 100 nm at a temperature of 580 °C. Then, the AlGaAs layer is grown to a thickness of 100 nm at a temperature

of 580 °C. The atomic composition of the group III elements in the AlGaAs layer is 85% aluminum and 15% gallium. The final capping GaAs layer is grown to 1000 nm at a temperature of 580 °C.

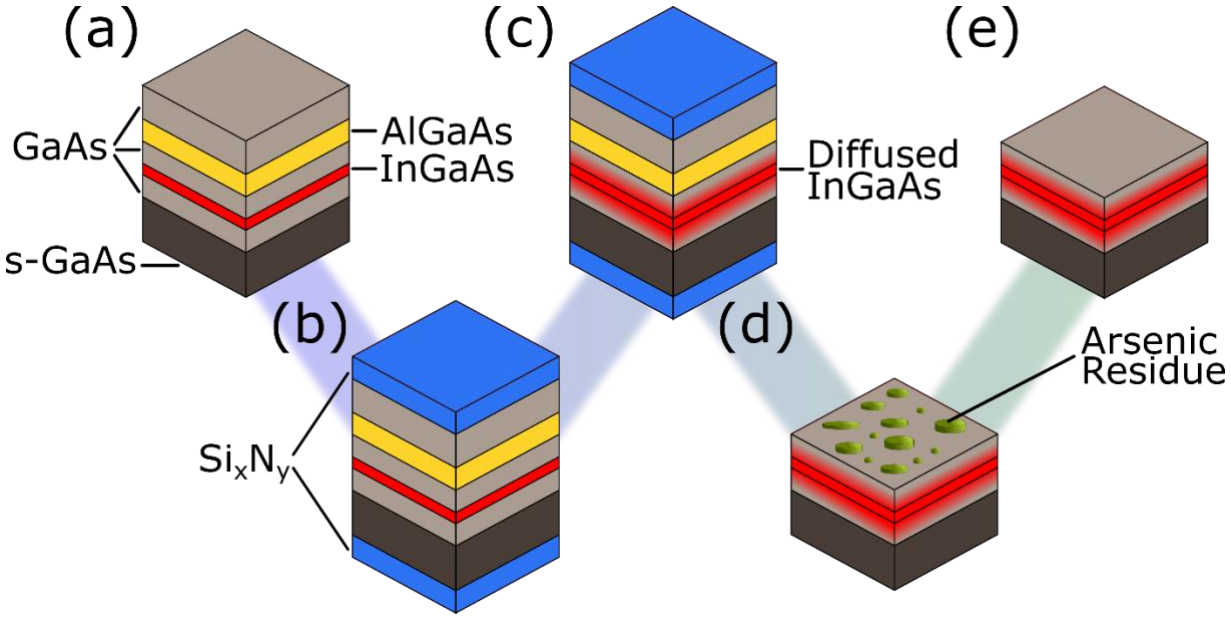

Figure 1: The layered structure for each step of the ESL procedure. (a) The process begins with an MBE-grown structure. (b) The structure is coated with Si_xN_y on the top and bottom surfaces before (c) annealing to diffuse the QW. (d) After the HF-etch and removal of the sacrificial layer, (e) a soft-anneal is used to remove arsenic residue and prepare the sample structure for SIMS analysis.

After the MBE growth, the sample is removed from the growth chamber, and the wafer is cleaved into square 1-cm^2 pieces in a cleanroom environment. The samples are placed into a SAMCO plasma-enhanced chemical vapor deposition (PECVD) chamber for Si_xN_y deposition. A silicon sample is included next to the GaAs/InGaAs/GaAs samples as a deposition reference sample. The Si_xN_y is deposited at a substrate platen temperature of 375 °C, RF power of 50 W, and frequency of 13.56 MHz for 10 minutes. The samples are then turned upside down, the silicon reference is taken out of the deposition chamber, and the Si_xN_y deposition process is repeated. Rahimi et al.[26] show that capping a III-V substrate on its top and bottom surfaces with Si_xN_y reduces annealing damage and preserves the III-V surfaces better than only depositing the cap on the top surface. A J.A. Woollam M-2000 ellipsometer is used to measure the Si_xN_y thickness on the silicon reference sample. The thickness is 514 nm with a refractive index of 1.94 at 532.8 nm. The structure after Si_xN_y deposition is shown in Fig. 1(b).

The Si_xN_y capped sample is placed into a Process Products Corporation rapid thermal annealer (RTA) with a Micristar 828 controller in a nitrogen environment. The temperature is increased to the annealing temperature, ranging from 775 °C to 875 °C, over 20 minutes to minimize damage from the Si_xN_y/GaAs thermal expansion coefficient mismatch. Once the setpoint temperature is reached, the sample is annealed and then cooled to room temperature. A diagram of the annealed sample's structure depicting the diffused InGaAs region is shown in Fig. 1(c) as a red-gradient colored region.

The annealed samples are submerged in a 59% hydrofluoric (HF) acid solution for 6 hours to remove the AlGaAs layer. The annealed samples are then rinsed with deionized water and blow-

dried with dry nitrogen. The sacrificial layer is then removed using cellophane tape. During the AlGaAs etching step, some arsenic can remain on the surface where it leaves a residue[11,27,28], which is identified by a brown discoloration by visual inspection. In the presence of oxygen, this arsenic residue reacts with oxygen from the air, eventually forming into arsenic oxide (As_2O_3) crystallites[28]. Arsenic residue and any As_2O_3 crystallites that may form are removed by flowing nitrogen during an anneal at a minimum temperature of 160 °C[27,29]. In this experiment, the samples are annealed at 300 °C for 30 minutes in a flowing nitrogen chamber. This 'soft anneal' is sufficiently below the decomposition temperature when arsenic sublimes from the surface, so no surface protection strategy is needed. The final structure is shown in Fig. 1(e).

The surface quality of the post-annealed samples is inspected using a scanning electron microscope (SEM). Energy-dispersive X-ray spectroscopy (EDS) is used to investigate the severe thermal degradation of the unencapsulated GaAs surface. Non-contact atomic force microscopy (AFM) is employed to verify the atomically smooth surface topologies of the GaAs/InGaAs/GaAs samples that underwent the complete ESL procedure. Compositional analysis is completed by dynamic SIMS, using an ionTOF TOF.SIMS 5 instrument. The concentration profiles obtained by SIMS analysis are used to calculate the diffusion parameters of indium in GaAs. The diffusion of indium is modeled with Fick's second law, assuming a position-invariant diffusion constant:

$$\frac{\partial C}{\partial t} = D\frac{\partial^2 C}{\partial z^2}. \tag{1}$$

$$D = D_o \exp\left(-\frac{E_a}{k_B T}\right) \tag{2}$$

where C is atomic concentration, D is diffusivity expressed in an Arrhenius relationship with temperature, and D_0 and E_a are the Arrhenius diffusion parameters.

Results and Discussion

SEM & EDS Analysis of Processed Gallium Arsenide Surfaces

Figure 2 shows the surface features after the thermal annealing process for the reference GaAs sample and the ESL sample. A GaAs(100) wafer is used as the reference GaAs sample to demonstrate the effects of thermal annealing on an unprotected surface. Both samples are annealed at 850 °C for 30 minutes. The damage to the unencapsulated substrate surface, shown in Fig. 2(a), is attributed to the sublimation of arsenic and the resulting pooling of metallic gallium[30]. This damage requires regeneration of the surface for further processing and impedes rigorous analysis of interdiffusion within the layered structure. The cross-sectional view of the reference GaAs sample reveals the degree of etching damage. In Fig. 2(c), deep trenches extend across the surface with vertical feature heights on the order of a micrometer. This damage is more than enough to alter the interdiffusion conditions within GaAs and would destroy the substrate's ability to perform in a device. Figure 2(d) depicts solidified droplets on the slopes of the trenches. These droplets, outlined by a dotted circle in Fig. 2(d), are assumed to be residual metallic gallium that has coalesced after arsenic sublimation. Lou *et al.* demonstrate that the presence of metallic gallium increases the rate of arsenic sublimation[31], while Kanjanachuchai *et al.* describe a mechanism in which metallic gallium etches and breaks down the GaAs crystal, releasing arsenic vapor and growing the metallic gallium droplets[30]. The etching phenomena brought about by arsenic loss thus explains the development of trench structures and the collection of gallium droplets.

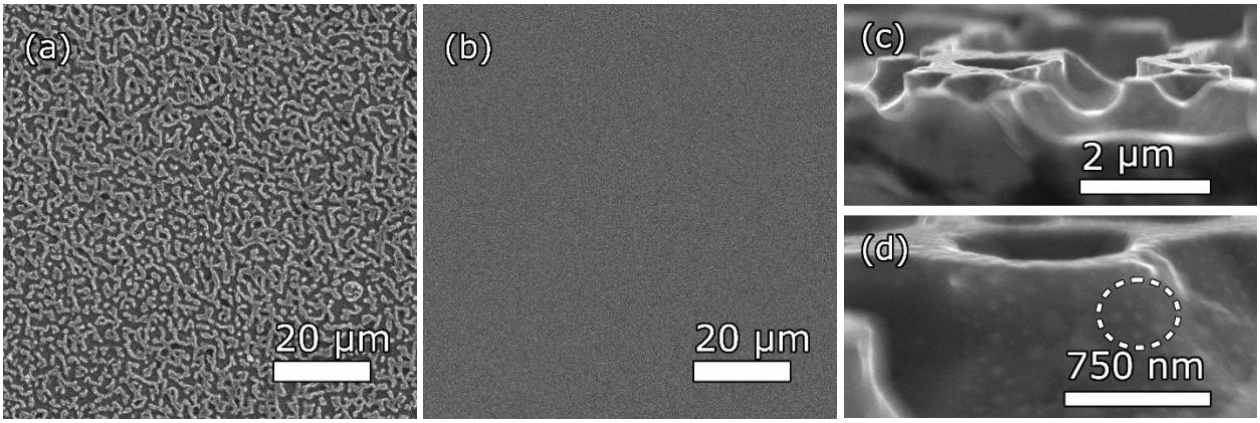

Figure 2: SEM images showing the GaAs surface after annealing (a) without the ESL method and (b) with the ESL method. Both surfaces are annealed at 850 °C for 30 minutes. (c) The damage from the annealing process on the unprotected GaAs surface is distributed across the sample's surface and features deep trench structures. (d) A closer look at these structures reveals solidified metallic gallium droplets speckling the surface. A cluster of solidified metallic gallium droplets has been circled.

Figure 3 shows the EDS results depicting gallium and arsenic concentrations of the GaAs substrate. The compositional analysis of Fig. 3(b) and 3(c) indicates a stoichiometric imbalance between gallium and arsenic due to arsenic leaving the GaAs system. Across the scanned region, the average atomic gallium content decreases to 48.2%, while the atomic arsenic content decreases to 47.3%. The remaining 4.5% is attributed to oxygen which is found throughout the sample. The presence of oxygen is likely a result of oxide formation after the GaAs reference sample is removed from the RTA furnace. Figs. 3(b) and 3(c) show that a surplus of metallic gallium has collected within the trenches while arsenic has been depleted from these same regions. A dotted circle outlines a mesa in Fig. 3 for ease of comparison. The local concentrations of atomic gallium, arsenic, and oxygen within the trench features are measured to be 52.4%, 43.8%, and 3.8%, respectively.

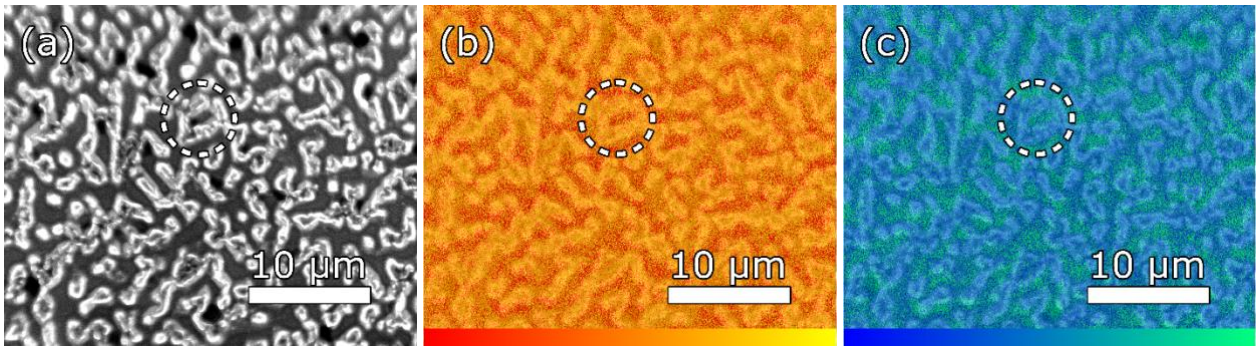

Figure 3: (a) SEM image of the area probed by the EDS instrumentation. EDS analysis of the annealed unprotected sample showing local concentrations of (b) gallium and (c) arsenic. Atomic compositions of gallium and indium decrease from left-to-right for their respective color bars. The EDS images are overlaid on top of the SEM image to provide a visual aid. A mesa has been circled for ease of comparison.

The sample shown in Fig. 2(b) has undergone the same thermal annealing procedure and demonstrates the effectiveness of the ESL method. The Si_xN_y coating mitigates the sublimation of arsenic from the sample surface and further prevents vacancies and metallic gallium from entering

the crystal lattice[32]. However, using only a Si_xN_y layer to protect the surface is insufficient to prevent damage to the substrate. The high thermal processing temperatures can result in the Si_xN_y layer cracking due to thermal mismatch, allowing some arsenic to sublimate. The sacrificial layer acts as a buffer for the minor damage that may occur because of localized cracking of the Si_xN_y. After the removal of the sacrificial layer, the resulting sample surface appears undamaged under SEM.

AFM Imaging & Surface Roughness Characterization of the ESL-Processed QW

AFM measurements are recorded to determine the roughness-mean-squared (RMS) values for the MBE grown structure and the ESL GaAs/InGaAs/GaAs quantum well structure, as shown in Fig. 4. The MBE reference structure is shown in Fig. 1(a). Figure 4(a) compares the height distribution histograms for each sample, and Fig. 4(b) depicts the smooth topography of the MBE reference's surface. The MBE reference is measured to have an RMS value of 3.9 Å and represents 30 μm^2 of the sample. Similar RMS values are expected for epi-ready surfaces[11].

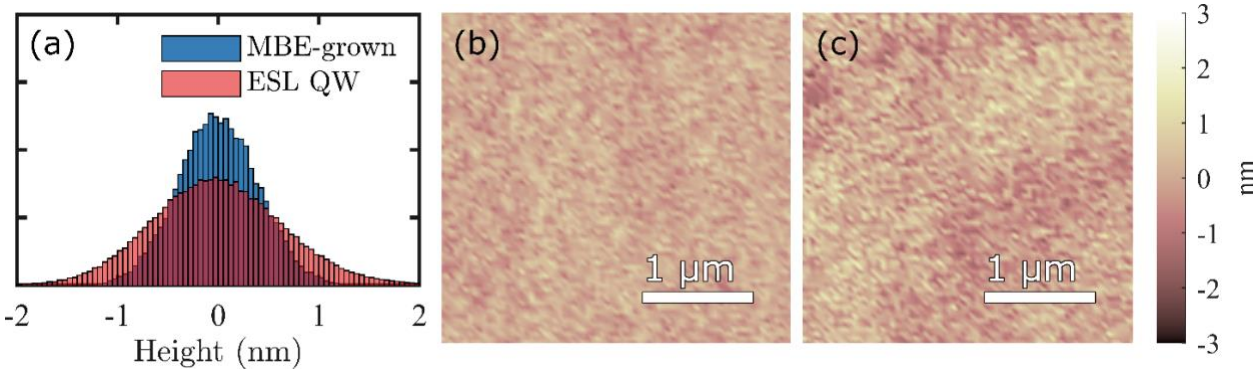

Figure 4: Non-contact AFM imaging is used to measure RMS values for the MBE-grown sample and the ESL QW sample. (a) The normalized histogram describes the smooth surfaces of the MBE-grown (blue) and the ESL QW (red) samples The AFM images of the (b) MBE-grown surface and the (c) ESL QW surface depict the surface roughness.

Figure 4(c) shows the roughness profile for a representative region of the ESL QW sample. The ESL QW surface is measured to have an RMS value of 6.5 Å over an area of 200 μm^2. The analysis is recorded over a larger region to demonstrate the extensively flat topography. While the HF wet-etch process is highly selective to the sacrificial AlGaAs layer, the acid passivates and weakly etches the GaAs interface[33,34]. AFM analysis is not completed on the annealed GaAs reference sample because of the AFM probe's inability to track the surface, likely caused by the sharp changes in surface topography and the probe laser melting the metallic gallium. The combined results of the AFM and SEM analysis show a featureless, smooth surface which is sufficient for further device fabrication, and the roughness is well below the threshold to enable high-resolution surface characterization.

Diffusion Parameter Extraction from InGaAs Quantum Well Structures

Preserving an undamaged and smooth GaAs surface is necessary for repeatable diffusion results. In the case of an unencapsulated surface, metallic gallium can enter the crystal lattice as interstitials. The interstitial gallium combines with vacancies, reducing the point defect mediated diffusion rate[12], resulting in a non-repeatable or unpredictable experiment. Additionally, preserving a smooth surface allows for a reliable compositional analysis as the sample roughness

limits the SIMS resolution for depth profiling. Without using the ESL procedure, SIMS analysis is impossible due to the destruction of the near-surface quantum well.

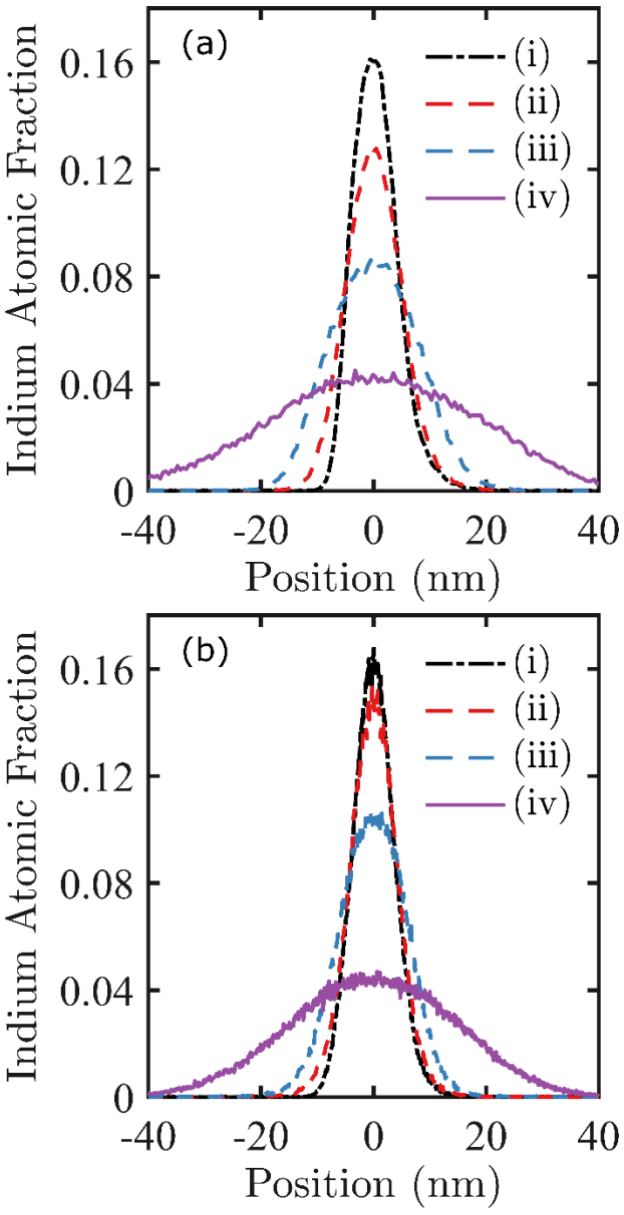

Figure 5: SIMS composition profiles of the indium atomic fraction as a function of position from the center of the quantum well. The samples annealed without removal of the arsenic residue are shown in (a). The samples that underwent the full ESL procedure are shown in (b). The processing conditions are: (i) unannealed sample, (ii) 775 °C for 15 minutes, (iii) 825 °C for 30 minutes, (iv) 875 °C for 30 minutes.

Figure 5 shows compositional profiles of a GaAs/InGaAs/GaAs QW under various annealing conditions. Figure 5(a) depicts the results of a sample that underwent the ESL procedure but

omitted the final soft-bake step. This was done to demonstrate how even a mildly roughened surface caused by arsenic crystallites can alter the precision of diffusion analysis of an annealed QW structure. The arsenic crystallites observed in this study were comparable to those seen in previous studies[27–29]. This sample is referred to as 'Partial ESL.' The figure shows the effect of a roughened surface due to arsenic residue and As_2O_3 crystallites, which broadened the indium atomic fraction peaks. This results in a wider perceived quantum well width. The full width at half maximum (FWHM) is calculated to be 7.0 nm for the (i) unannealed sample and 30.4 nm for the sample annealed at (iv) 875 °C for 30 minutes. Figure 5(b) demonstrates the soft anneal's effect on removing the arsenic residue, which reduces the surface roughness and improves the sample analysis resolution. This sample is referred to as 'Full ESL.' The FWHM is determined to be 6.7 nm for the (i) unannealed sample and 26.2 nm for the sample annealed at (iv) 875 °C for 30 minutes. The impact of surface roughness increases as the indium concentration profile broadens.

The indium atomic fraction results in Fig. 5 have been fit to determine the Arrhenius parameters, D_0 and E_a, using a Fickian model, shown in Table 1. The activation energies, E_a, for 'Partial ESL and 'Full ESL' are calculated to be 3.12 eV and 3.19 eV, which fall within the bounds of literature values[35]. The calculated interdiffusion pre-factors, D_0, are $0.034\ \mathrm{cm^2 s^{-1}}$ and $0.035\ \mathrm{cm^2 s^{-1}}$, respectively. 'Full ESL' shows a higher degree of precision compared to 'Partial ESL' for both calculated parameters, as shown in Table 1, suggesting the roughened surface hinders the ability to collect accurate diffusion data. D_0 is reported in Table 1 as a natural log value to be consistent with the method of analysis used in the diffusion parameter estimation. Compared to the roughened 'Partial ESL' surface, the 95% confidence interval (CI) is significantly improved. More information on the diffusion parameter calculations is available in the supplementary material associated with this text[36].

Many studies have suggested that semiconductor diffusion may be concentration or strain-dependent[37–42]. Bollet *et al.* demonstrate this behavior in the InGaAs/GaAs system and make a comparable claim that Fick's law with a constant diffusion coefficient is incorrect[38]. The ESL method allows for definitive analysis of thermal interdiffusion to determine the impact of concentration and strain on atomic diffusivity in semiconductors.

	E_a (eV)	95%-CI	$\ln(D_0)$	95%-CI
Partial ESL	3.12	$\pm 4.65\%$	-3.38	$\pm 46.2\%$
Full ESL	3.19	$\pm 0.01\%$	-3.34	$\pm 0.82\%$

Table 1: The Arrhenius parameters, D_0 and E_a, are calculated using a constant diffusion coefficient model for the indium concentration profiles depicted in Fig. 5. The 95%-confidence interval is improved significantly due to preserving a smooth surface compared to the roughened 'Partial ESL' surface.

Summary and Conclusion

A methodology for high-temperature processing of III-V materials is demonstrated, which preserves surface quality for high-resolution atomic composition analysis and further processing.

A GaAs/InGaAs/GaAs quantum well is grown with a sacrificial AlGaAs layer in an MBE chamber. Si_xN_y is deposited on the top and bottom of the sample for further protection. After an RTA treatment step, the Si_xN_y and AlGaAs layers are removed, and the sample is characterized to demonstrate the success of the ESL method.

SEM analysis shows the atomically smooth ESL-protected GaAs surface in contrast to the damage present on the reference GaAs surface. EDS confirms the stoichiometric imbalance due to the sublimation of arsenic and coalescence of metallic gallium on the reference GaAs. AFM imaging provides an RMS value of 6.5 Å over a large substrate area after the ESL method. The limiting factor in compound semiconductor diffusion analysis is repeatability and ill-defined experimental conditions, which readily alter diffusion outcomes and introduce substantial uncertainty. The ESL method enables high-resolution SIMS analysis to study the mechanisms of thermal interdiffusion in compound semiconductors. Further optimization of the ESL process, particularly the wet-etching procedure, would allow for epi-ready, passivated surfaces.

Acknowledgments

This material is based upon work supported by the National Science Foundation under Grant Nos. (DMR-1809095 and DMR-1808065). This material makes use of the TOF-SIMS system at the Colorado School of Mines, which was supported by the National Science Foundation under Grant No.1726898.

Data Availability Statement

The data that support the findings of this study are available from the corresponding author upon reasonable request.

References

[1] T. Sebestyen, M. Menyhard, and D. Szigethy, Electron. Lett. **12**, 96 (1976).
[2] C.D. Yerino, B. Liang, D.L. Huffaker, P.J. Simmonds, and M.L. Lee, J. Vac. Sci. Technol. B **35**, 010801 (2016).
[3] J.R. Arthur, Surf. Sci. **43**, 449 (1974).
[4] D. Haneman, J. Appl. Phys. **31**, 217 (1960).
[5] C.W. Wilmsen, editor , *Physics and Chemistry of III-V Compound Semiconductor Interfaces* (Springer US, Boston, MA, 1985).
[6] D. Ning, Y. Chen, X. Li, D. Liang, S. Ma, P. Jin, and Z. Wang, J. Semicond. **41**, 122101 (2020).
[7] H.H. Yee and C.-P. Yu, Appl. Opt. **42**, 2695 (2003).
[8] H. Morota and S. Adachi, J. Appl. Phys. **105**, 043508 (2009).
[9] T.D. Lowes and M. Zinke-Allmang, J. Appl. Phys. **73**, 4937 (1993).
[10] G.J. Bauhuis, P. Mulder, E.J. Haverkamp, J.J. Schermer, E. Bongers, G. Oomen, W. Köstler, and G. Strobl, Prog. Photovolt. Res. Appl. **18**, 155 (2010).
[11] C.-W. Cheng, K.-T. Shiu, N. Li, S.-J. Han, L. Shi, and D.K. Sadana, Nat. Commun. **4**, 1577 (2013).
[12] E.H. Li, editor , *Semiconductor Quantum Wells Intermixing* (Gordon and Breach Science Publishers, Amsterdam, The Netherlands, 2000).
[13] W.P. Gillin and D.J. Dunstan, 5 (1998).

[14] L.J. Guido, N. Holonyak, K.C. Hsieh, R.W. Kaliski, W.E. Plano, R.D. Burnham, R.L. Thornton, J.E. Epler, and T.L. Paoli, J. Appl. Phys. **61**, 1372 (1987).
[15] B.L. Olmsted and S.N. Houde-Walter, Appl. Phys. Lett. **60**, 368 (1992).
[16] A. Furuya, O. Wada, A. Takamori, and H. Hashimoto, Jpn. J. Appl. Phys. **26**, L926 (1987).
[17] N. Baba-Ali, I. Harrison, and B. Tuck, J. Mater. Sci. Mater. Electron. **6**, (1995).
[18] J. Dreybrodt, A. Forchel, and J.P. Reithmaier, Phys. Rev. B **48**, 14741 (1993).
[19] F. Alexandre, L. Goldstein, G. Leroux, M.C. Joncour, H. Thibierge, and E.V.K. Rao, J. Vac. Sci. Technol. B Microelectron. Nanometer Struct. **3**, 950 (1985).
[20] S. Ogawa, N. Uehara, M. Ohmukai, and Y. Tsutsumi, MRS Proc. **638**, F5.28.1 (2000).
[21] M.A. Moram, C.F. Johnston, M.J. Kappers, and C.J. Humphreys, J. Phys. Appl. Phys. **42**, 135407 (2009).
[22] Y. Kaynak and E. Tascioglu, Procedia CIRP **71**, 500 (2018).
[23] S.V. Baryshev, A.V. Zinovev, C.E. Tripa, M.J. Pellin, Q. Peng, J.W. Elam, and I.V. Veryovkin, Rapid Commun. Mass Spectrom. **26**, 2224 (2012).
[24] S. Fearne, *An Introduction to Time-of-Flight Secondary Ion Mass Spectrometry (ToF-SIMS) and Its Application to Materials Science* (IOP Publishing, 2015).
[25] R. Liu, C.M. Ng, and A.T.S. Wee, Appl. Surf. Sci. 4 (2003).
[26] N. Rahimi, A.A. Aragon, D.M. Shima, C. Hains, T. Busani, O. Lavrova, G. Balakrishnan, and L.F. Lester, J. Vac. Sci. Technol. B Nanotechnol. Microelectron. Mater. Process. Meas. Phenom. **32**, 04E109 (2014).
[27] T. Nakata, K. Watanabe, H. Sodabanlu, D. Kimura, N. Miyashita, Y. Okada, Y. Nakano, and M. Sugiyama, in *2017 IEEE 44th Photovolt. Spec. Conf. PVSC* (IEEE, Washington, DC, 2017), pp. 854–857.
[28] N.J. Smeenk, J. Engel, P. Mulder, G.J. Bauhuis, G.M.M.W. Bissels, J.J. Schermer, E. Vlieg, and J.J. Kelly, ECS J. Solid State Sci. Technol. **2**, P58 (2013).
[29] U. Resch, N. Esser, Y.S. Raptis, W. Richter, J. Wasserfall, A. Förster, and D.I. Westwood, Surf. Sci. **269–270**, 797 (1992).
[30] S. Kanjanachuchai and C. Euaruksakul, ACS Appl. Mater. Interfaces **5**, 7709 (2013).
[31] C.Y. Lou and G.A. Somorjai, J. Chem. Phys. **55**, 4554 (1971).
[32] M. Kuzuhara, T. Nozaki, and T. Kamejima, J. Appl. Phys. **66**, 5833 (1989).
[33] P. Kumar, S. Kanakaraju, and D.L. DeVoe, Appl. Phys. A **88**, 711 (2007).
[34] S. Adachi and D. Kikuchi, J. Electrochem. Soc. **147**, 4618 (2000).
[35] O.M. Khreis and I.S. Al-Kofahi, Semicond. Sci. Technol. **20**, 320 (2005).
[36]See supplementary material at [URL will be inserted by AIP Publishing] for the method for diffusion parameter estimation.
[37] L.L. Chang and A. Koma, Appl. Phys. Lett. **29**, 138 (1976).
[38] F. Bollet and W.P. Gillin, J. Appl. Phys. **101**, 013502 (2007).
[39] F. Bollet, W.P. Gillin, M. Hopkinson, and R. Gwilliam, J. Appl. Phys. **97**, (2005).
[40] H. Temkin, S.N.G. Chu, M.B. Panish, and R.A. Logan, Appl. Phys. Lett. **50**, 956 (1987).
[41] Y. Dong, W. Chern, P.M. Mooney, J.L. Hoyt, and G. (Maggie) Xia, Semicond. Sci. Technol. **29**, (2014).
[42] G. (Maggie) Xia, Sci. Bull. **64**, 1436 (2019).

Supplementary Information: Method For Diffusion Parameter Estimation

Formalism to describe solid state diffusion in semiconductor systems

Fick's First Law relates the diffusive flux $\boldsymbol{J}$ to the concentration gradient ∇C where the flux goes from a high concentration region to low concentration as

$$\boldsymbol{J} = -D\nabla C, \tag{1}$$

where D is the chemical diffusion coefficient. The number of diffusing particles is conserved, assuming no reactions occur. The continuity equation for diffusion is

$$\frac{\partial C}{\partial t} = -\nabla \cdot \mathbf{J}. \tag{2}$$

Combining Fick's First Law Eq. (1) and the continuity equation (2) yields the diffusion equation, also known as Fick's Second Law. The general diffusion equation, assuming no convection, is given by

$$\frac{\partial C}{\partial t} = \nabla \cdot (D\nabla C). \tag{3}$$

For GaAs semiconductor systems the diffusion coefficient is commonly assumed to be isotropic and independent of concentration or coordinate, which reduces Eq. (3) to

$$\frac{\partial C}{\partial t} = D\nabla^2 C. \tag{4}$$

In this experiment, a quantum well containing InGaAs was grown between two layers of GaAs, which reduces the problem to a 1-D case where there is only a concentration gradient in the z-direction. The 1-D diffusion equation for a quantum well is

$$\frac{\partial C}{\partial t} = D\frac{\partial^2 C}{\partial z^2}. \tag{5}$$

The temperature dependence of the diffusion coefficient is modelled with the Arrhenius equation as

$$D = D_o \exp\left(-\frac{E_a}{k_B T}\right), \tag{6}$$

where the diffusion coefficient is a function of the preexponential factor D_o, the activation energy E_a, Boltzmann constant k_B and the absolute temperature T.

Thermal History vs. Constant Temperature Approximation

For diffusion to occur, the sample must be heated significantly above room temperature. For GaAs, diffusion processes become more prominent beyond 500 °C. In this work, the annealing temperature is gradually ramped up for 20 minutes to prevent damage to the samples from thermal mismatch, which are then annealed at the target temperature. The rapid thermal annealer (RTA) used in this experiment is cooled by convection driven by the flow of nitrogen in

and out of the annealing chamber. During the ramp up and ramp down phases, the samples undergo significant diffusion, even though they are below the annealing temperature. Often, the ramp up and ramp down are ignored in numerous studies, and the anneal is assumed to be occurring at a constant temperature. However, since the ramp up/down times are comparable to the overall annealing time, diffusion during these stages contribute significantly to diffusion length L_D. As such, it is necessary to account for the temperature history to properly estimate the diffusion parameters.

The diffusion length L_D is a measure of how far the concentration has propagated in a direction over some timeframe, shown by Eq. (7) below. The time dependent diffusion coefficient $D(t)$ is integrated over the whole high temperature processing time from t_i to t_f.

$$L_D = 2\sqrt{\int_{t_i}^{t_f} D(t)dt} \tag{7}$$

The temperature profile for the 775 °C and 15-minute anneal is shown in Fig. 1. The RTA chamber starts at room temperature after the sample is loaded. The sample is heated to 200 °C, and the air inside the chamber is purged and replaced with nitrogen gas. The heating up then starts at t_1. The heating continues until it reaches the annealing temperature at t_2.The sample is then annealed at constant temperature from t_2 to t_3. Once the anneal is complete at t_3, the RTA chamber is cooled down by the convection of N_2 till t_4,where diffusion becomes negligible. We have conducted the diffusion simulation for when the samples are heated above 500°C, which is set as the cutoff temperature as diffusion below that temperature would not change the diffusion length noticeably.

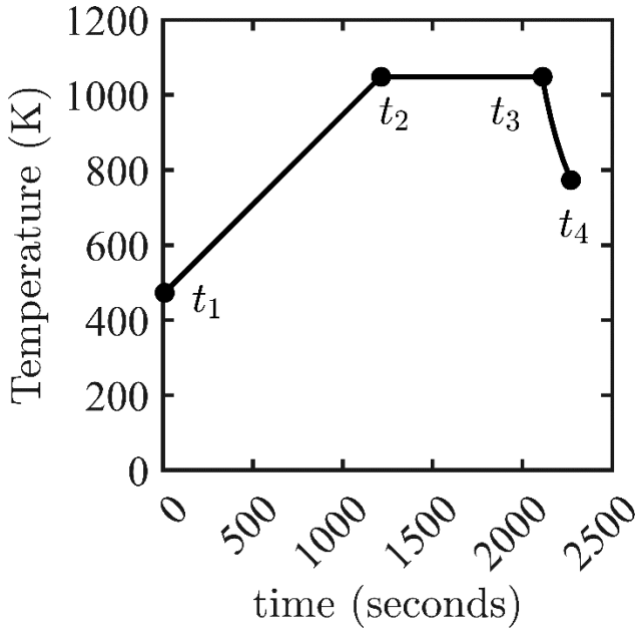

Figure 1: Temperature history profile for the 775 °C and 15-minute anneal

To determine if it is necessary to account for the full temperature profile, the error introduced by a constant temperature approximation can be estimated by considering the ratio between diffusion lengths which accounts for temperature history case, $L_{D,TH}$, and the constant temperature case, $L_{D,CT}$:

$$\frac{L_{D,TH}}{L_{D,CT}} = \frac{2\sqrt{\int_{t_1}^{t_4} D(t)dt}}{2\sqrt{\int_{t_2}^{t_3} Ddt}}. \tag{8}$$

For the constant temperature case, only diffusion between t_2 and t_3 is considered, which simplifies Eq. (8) to

$$\frac{L_{D,TH}}{L_{D,CT}} = \frac{\sqrt{\int_{t_1}^{t_4} D(t)dt}}{\sqrt{D(T_{Anneal})(t_3 - t_2)}}. \tag{9}$$

The Arrhenius equation from Eq. (6) is used to relate D with the temperature profile $T(t)$ to obtain Eq. (10). Since D_o is a constant for both cases it will cancel out, which gives

$$\frac{L_{D,TH}}{L_{D,CT}} = \frac{\sqrt{\int_{t_1}^{t_4} \exp\left(-\frac{E_a}{k_B T(t)}\right) dt}}{\sqrt{\exp\left(-\frac{E_a}{k_B T_{Anneal}}\right)(t_3 - t_2)}}. \tag{10}$$

In the 775 °C and 15-minute anneal case, the ratio of $L_{D,TH}$ to $L_{D,CT}$is 1.02 which can considerably affect the confidence interval of the estimated diffusion parameters using the literature value of $E_a = 3.07\ eV$[1]. The ratio varies between 1.02 to 1.04 for our annealing temperature range. For the constant temperature assumption to be valid, the heating/cooling cycles must be significantly shorter than the annealing time.

Nonlinear Least-Squares Sample Calculation

To determine the Arrhenius parameters for the diffusion coefficient, Fick's second law is numerically solved, and the parameters are estimated using a non-linear least squares curve fitting approach

$$\underset{\ln \mathrm{D}_o, E_a}{\operatorname{argmin}} \left\| \mathrm{C}_{sim}(\mathrm{E}_a, \mathrm{D}_o, \mathbf{z}) - \mathrm{C}_{data}(\mathbf{z}) \right\|_2^2 \tag{11}$$

The diffusion processes are simulated with a given E_a and $\mathrm{D}_o$and then compared with the observed concentration C_{data} at all positions $\mathbf{z}$. The 775 °C, 825 °C, and 875 °C temperature cases are solved simultaneously. The sum of the squares of $(\mathrm{C}_{sim}(\mathrm{E}_a, \mathrm{D}_o, \mathbf{z}) - \mathrm{C}_{data}(\mathbf{z}))$ are calculated. The E_a and $\mathrm{D}_o$values are refined using the Trust Region Reflective Algorithm until convergence is achieved[2]. To maintain the same model stiffness to the parameters, the two fitting parameters used are E_a and D_{sim}, where $D_{sim} \equiv \ln D_0$ so that

$$D_o = \exp(D_{sim})\,. \tag{12}$$

For the first iteration, $E_a = 3.00\ eV$ and $D_{sim} = -4.30$ are the initial guess values, and the simulated normalized concentration and the normalized experimental concentration profiles are plotted in Fig. (2).

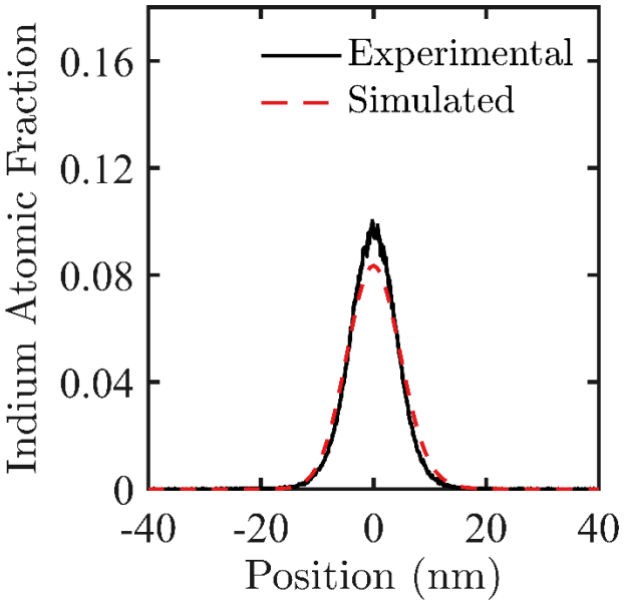

Figure 2: First iteration of the parameter estimation with the initial fitting parameters for the 775 °C and 15-minute case.

The fully converged simulated normalized concentration profile and the normalized concentration profile are shown in Fig (3).

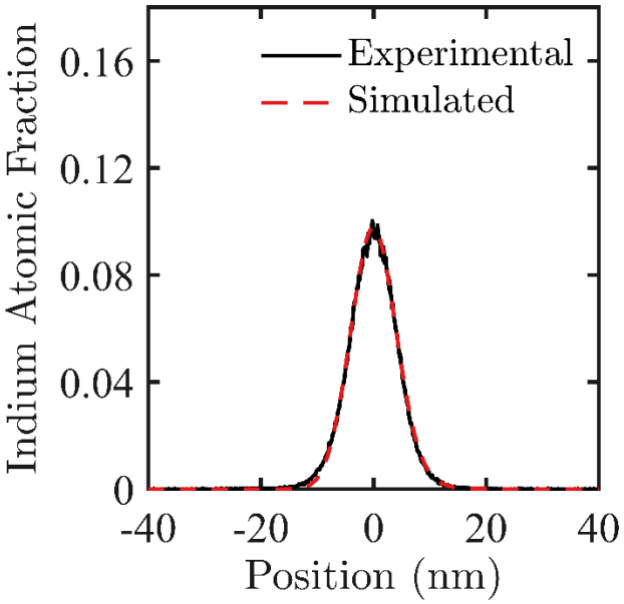

Figure 3: Fully converged parameter estimation with $E_a = 3.19\ eV$ and $D_{sim} = -3.34$.

References

[1] O.M. Khreis and I.S. Al-Kofahi, Semicond. Sci. Technol. **20**, 320 (2005).
[2] M.A. Branch, T.F. Coleman, and Y. Li, SIAM J. Sci. Comput. **21**, 1 (1999).

Figures for Maintaining Atomically Smooth GaAs Surfaces After High-Temperature Processing for Precise Interdiffusion Analysis and Materials Engineering

Leonid Miroshnik[1], Brian D. Rummel[2], Andrew Li[4], Ganesh Balakrishnan[3], Talid Sinno[4] and Sang M. Han[1,2,3‡] (meister@unm.edu)

[1]*Chemical & Biological Engineering, University of New Mexico, Albuquerque, New Mexico 87131, USA*

[2]*Nanoscience & Microsystems Engineering, University of New Mexico, Albuquerque, New Mexico 87131, USA*

[3]*Center for High Technology Materials, University of New Mexico, Albuquerque, New Mexico 87106, USA*

[4]*Chemical & Biomolecular Engineering, University of Pennsylvania, Philadelphia, Pennsylvania 19146, USA*

Figure 1

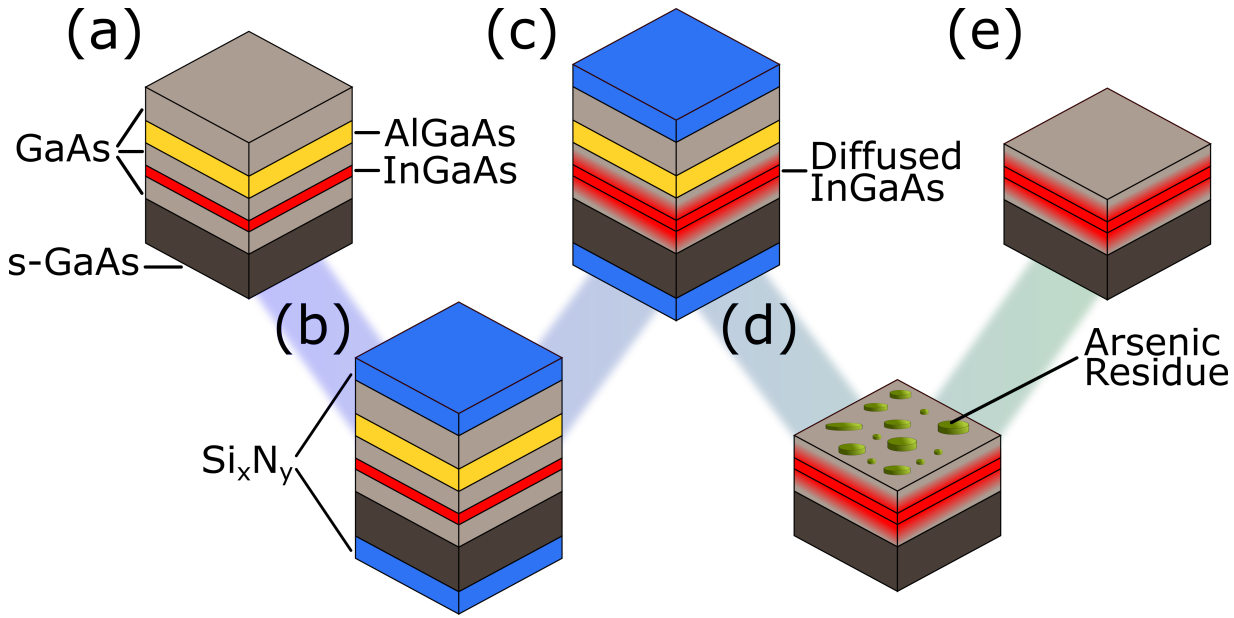

Figure 1: The layered structure for each step of the ESL procedure. (a) The process begins with an MBE-grown structure. (b) The structure is coated with Si_xN_y on the top and bottom surfaces before (c) annealing to diffuse the QW. (d) After the HF-etch and removal of the sacrificial layer, (e) a soft-anneal is used to remove arsenic residue and prepare the sample structure for SIMS analysis.

Figure 2

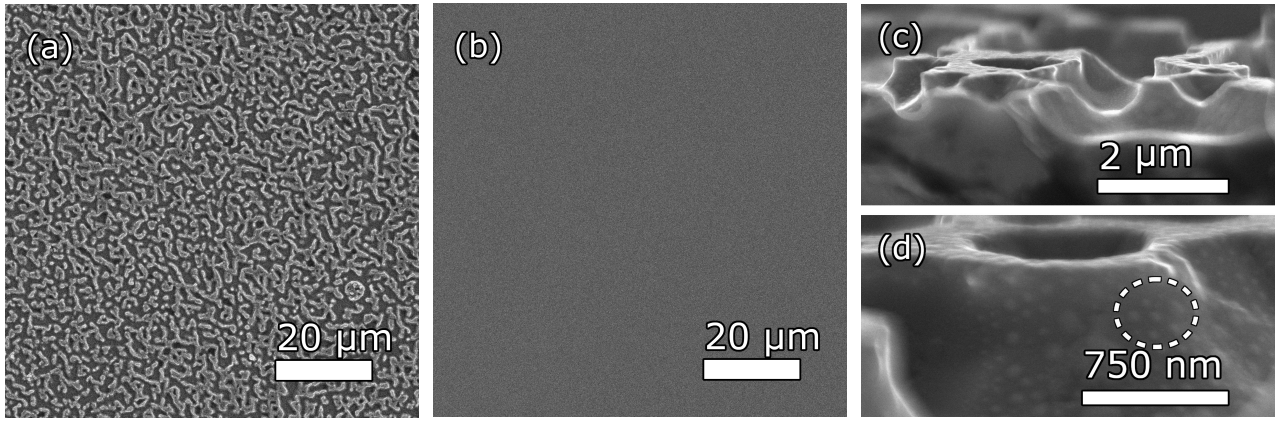

Figure 2: SEM images showing the GaAs surface after annealing (a) without the ESL method and (b) with the ESL method. Both surfaces are annealed at 850 °C for 30 minutes. (c) The damage from the annealing process on the unprotected GaAs surface is distributed across the sample's surface and features deep trench structures. (d) A closer look at these structures reveals solidified metallic gallium droplets speckling the surface. A cluster of solidified metallic gallium droplets has been circled.

Figure 3

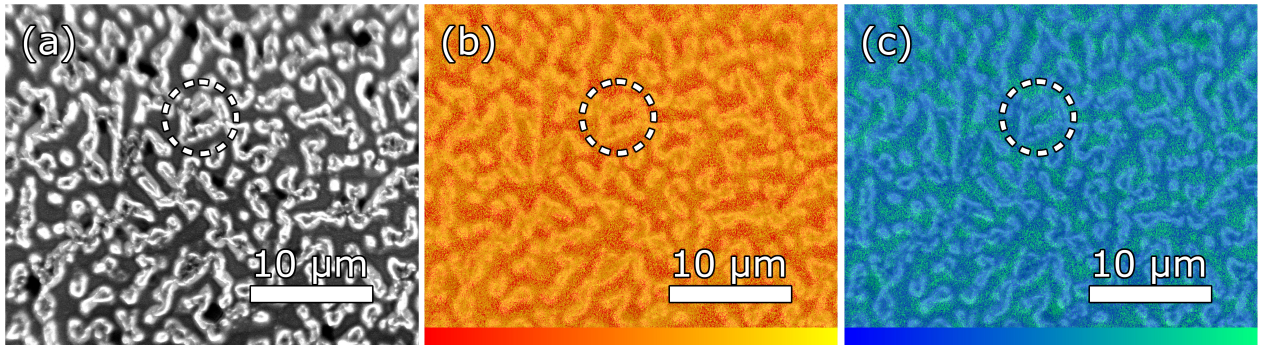

Figure 3: (a) SEM image of the area probed by the EDS instrumentation. EDS analysis of the annealed unprotected sample showing local concentrations of (b) gallium and (c) arsenic. Atomic compositions of gallium and indium decrease from left-to-right for their respective color bars. The EDS images are overlaid on top of the SEM image to provide a visual aid. A mesa has been circled for ease of comparison.

Figure 4

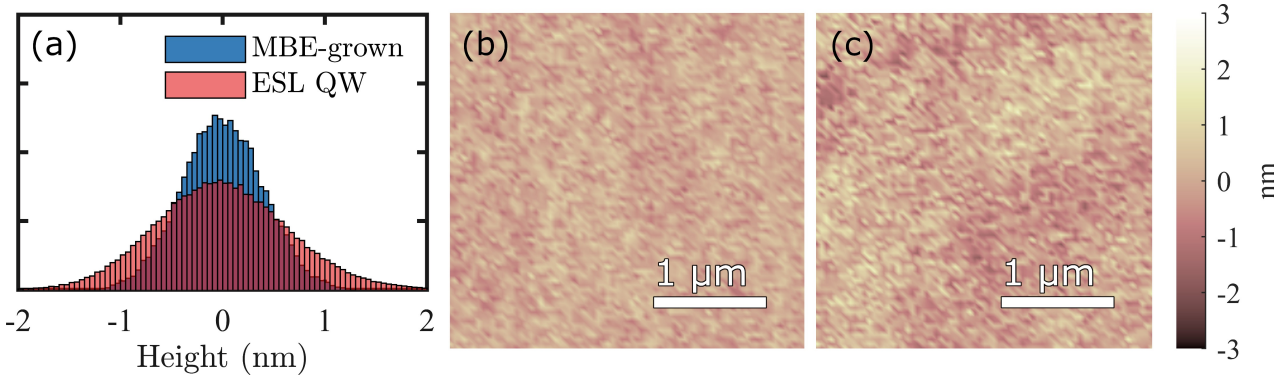

Figure 4: Non-contact AFM imaging is used to measure RMS values for the MBE-grown sample and the ESL QW sample. (a) The normalized histogram describes the smooth surfaces of the MBE-grown (blue) and the ESL QW (red) samples The AFM images of the (b) MBE-grown surface and the (c) ESL QW surface depict the surface roughness.

Figure 5

Figure 5: SIMS composition profiles of the indium atomic fraction as a function of position from the center of the quantum well. The samples annealed without removal of the arsenic residue are shown in (a). The samples that underwent the full ESL procedure are shown in (b). The processing conditions are: (i) unannealed sample, (ii) 775 °C for 15 minutes, (iii) 825 °C for 30 minutes, (iv) 875 °C for 30 minutes.