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A Generalized Power Supply Induced Jitter Model Based on Power Supply Rejection Ratio Response

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Abstract

In this work, a generalized power supply induced jitter (PSIJ) model is proposed. The PSIJ sensitivity is obtained based on the evaluation of driver power supply rejection ratio (PSRR) response. The voltage ripple at the driver output is transformed into driver output jitter with the slope of the switching edge. The time averaged effect of power noise during the time range of driver propagation delay is also considered. The proposed model is applied to estimate the PSIJ sensitivity for typical inverter type of drivers as well as a low-voltage differential signaling (LVDS) type of current mode differential transmitter. Depending on the transistor working region in the driver, the PSIJ sensitivity frequency dependency could be either dominated by the propagation delay or the PSRR response. The accuracy of the predicted PSIJ sensitivity is verified by simulation. Reasonably good accuracy has been achieved in terms of both the magnitude and phase.

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Yin Sun received the B.S. degree in micro-electronics from Fudan University, Shanghai, China in 2013, the M.S. degree in electrical and computer engineering from Hong Kong University of Science and Technology (HKUST), Hong Kong, China, in 2016, the Ph.D. degree in electrical engineering at the Electromagnetic Compatibility (EMC) Laboratory, Missouri University of Science and Technology (formerly University of Missouri-Rolla), Rolla, MO, USA in 2020. She is currently with the Zhejiang Lab, Hangzhou, China, as a research fellow. Her research interests include radio frequency interference in mobile devices, EMI source modeling and prediction, power supply induced jitter in I/O buffer, power distribution network target impedance design, signal/power integrity in high-speed digital systems and acoustic noise in multilayer ceramic capacitors

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Introduction

The timing budget for today's I/O interfaces becomes tighter as the transition speed of I/O keeps increasing. Along with the continuously decreasing of unit interval, the requirements for allowable jitter also becomes stricter and the jitter prediction becomes more important. The power supply induced jitter (PSIJ) has become one of the major concerns for high-speed system.

The PSIJ sensitivity for inverter type of buffers has been widely studied. However, there are not much discussion about PSIJ sensitivity of drivers that are not based on an inverter. The other type of drivers is also implemented in many designs [1] and the PSIJ sensitivity for these drivers is also important. For PSIJ sensitivity derivation, some treat the inverter type of buffers as voltage-controlled delay line (VCDL) [2] and the PSIJ sensitivity can be easily derived with the form of a sinc function. However, this delay-based method cannot be generalized for the other type of drivers, as the other type of drivers cannot be simply regarded as a VCDL. A numerical method is proposed to estimate PSIJ for a current mode differential driver using a root-finding approach by classical Newton's method [3], but the expression is not straight-forward and the physical meaning is not clearly revealed. In addition, a statistical method based on response surface model combined with Latin Hypercube Sampling (LHS) is used to model jitter in short pulse generation circuits [4]. However, the model is purely mathematical and is lack of physical meanings. Some works have provided analytical method based on the piecewise transistor linear model using transient analysis [5]. The jitter is estimated as the ratio of the output voltage ripple versus the switching edge slope. However, the analytical derivation in time domain is complicated and difficult to apply to other type of drivers.

In this paper, a generalized PSIJ sensitivity model based on power supply rejection ratio (PSRR) response is proposed. The output voltage ripple to the power rail voltage ripple relationship could be easily established through the PSRR response in the frequency domain, allowing easier derivation while maintaining some physical insights. The proposed model is applied for a single stage inverter, an inverter chain and a voltage differential signaling (LVDS) type of current mode differential transmitter. The PSIJ sensitivity derivation is based on the frequency domain PSRR response, slope of the switching edge and the time averaged effect of power noise in the time range of propagation delay. The obtained PSIJ sensitivity expressions are validated through comparison with transistor level circuit simulation for both the magnitude and phase. Depending on the transistor working region in the driver, the frequency dependency of PSIJ sensitivity can be determined by different factors.

PSRR Based PSIJ Sensitivity Model

Conceptually, the PSIJ sensitivity can be written as the ratio of the output time interval error (TIE) Δt to the voltage ripple level on the power rail ΔV_{dd}, when a single frequency sinusoidal noise exhibits on the power rail. This ratio can be reformed into the ratio of PSRR to switching edge slope [6] as follows:

$$\frac{\Delta t}{\Delta V_{dd}} = \frac{\Delta V_o / \Delta V_{dd}}{\Delta V_o / \Delta t} = \frac{PSRR}{Slope} \tag{1}$$

where ΔV_o is the variation of output voltage. This concept can also be derived from the decomposed multiple output voltage transition edges as illustrated in Fig. 1.

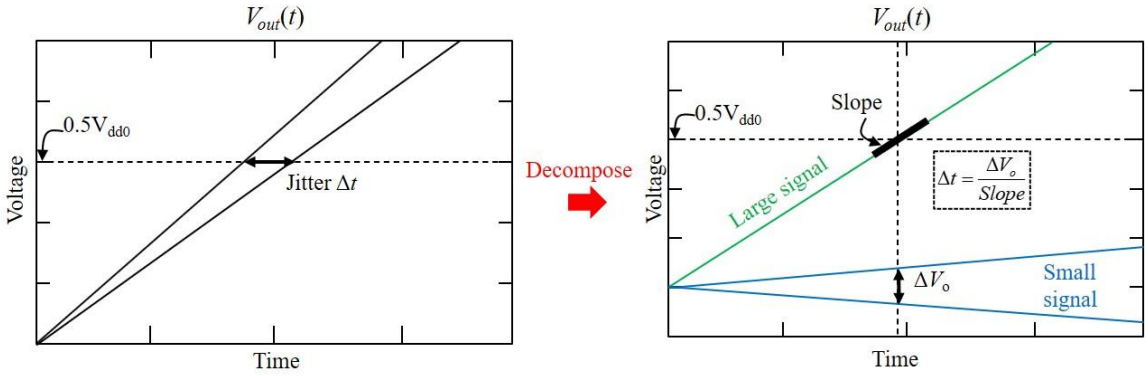


Fig. 1. Jitter derivation from decomposed multiple output voltage transition edges.

The two low to high transition edges are the minimum and maximum delay cases corresponding to the maximum and minimum of a sinusoidal power voltage fluctuation, respectively. At half the nominal power rail voltage V_{dd0}, the timing difference between the two edges is jitter Δt. The multiple output transition edges can be decomposed into a large signal portion, where the transition happens with power rail voltage V_{dd0}, and a small signal portion, which is introduced by the power rail voltage fluctuation [5]. At half the V_{dd0}, the slope can be determined from the large signal portion and the variation of output voltage ΔV_o can be extracted from the small signal portion. The jitter can then be estimated as $\Delta t = \Delta V_o / \text{Slope}$.

The frequency domain PSRR response $PSRR(\omega)$ can be separated into the peak value portion $PSRR_p$ and the normalized frequency dependency portion $PSRR'(\omega) = PSRR(\omega)/PSRR_p$. In low frequency ranges where the voltage ripple period is much larger than the propagation delay, the power rail ripples affect the driver output noise in the same manner as a DC offset [5]. In this low frequency ranges and DC condition, the PSRR is constant and has the peak value since it is determined only by the amplitude of the power rail noise. The $PSRR_p$ can be written as the ratio of output fluctuation to power rail voltage fluctuation at DC, $\Delta V_o/\Delta V_{dd}|_{DC}$. The slope can be expressed as the ratio of output fluctuation to delay change at DC, $\Delta V_o/\Delta t|_{DC}$. Equation (1) can then be reformed as:

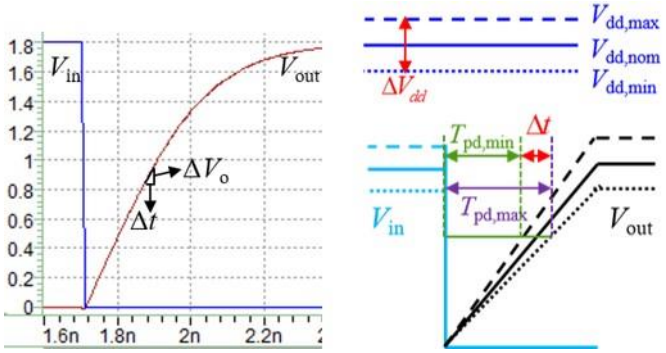
$$\frac{PSRR(\omega)}{Slope} = \frac{PSRR_p \cdot PSRR'(\omega)}{Slope} = \frac{\Delta V_o/\Delta V_{dd}\big|_{DC}}{\Delta V_o/\Delta t\big|_{DC}} PSRR'(\omega) = \frac{\Delta t}{\Delta V_{dd}}\bigg|_{DC} PSRR'(\omega) \qquad (2)$$

where ω is the angular frequency. Since the jitter is evaluated at half V_{dd0}, it is a common practice to extract the slope of the transition edge near this voltage level, as illustrated in Fig. 2(a). By taking a small variation of output voltage and recording the corresponding timing difference, the slope of the rising edge can be calculated. However, in practice, the rising edge is not a perfect straight line and the output edge slope during propagation delay time range will not be a constant. Applying the slope value read from output edge near half V_{dd0} can lead to inaccurate PSIJ sensitivity results, as the slope effect during the entire propagation delay time range is neglected. In order to obtain a slope value that can

give a better result for PSIJ sensitivity estimation, the slope is extracted from the driver delay change test under different power rail voltage level at DC, as depicted in Fig. 2(b). With maximum power rail voltage level $V_{dd,max}$, the corresponding propagation delay of the driver will be the smallest $T_{pd,min}$. With minimum power rail voltage level $V_{dd,min}$, the driver will exhibit a maximum propagation delay as $T_{pd,max}$. The ratio of the variation in power voltage ΔV_{dd} to the corresponding variation of propagation delay Δt is related to slope, as represented in the following equation:

$$\frac{Slope}{PSRR_p} = \frac{\Delta V_{dd}}{\Delta t}\bigg|_{DC} = \frac{V_{dd.\max} - V_{dd.\min}}{T_{pd,\max} - T_{pd,\min}} \tag{3}$$

which is the inverse of the DC jitter sensitivity $(T_{pd,max} - T_{pd,min})/(V_{dd,max} - V_{dd,min})$.



(a) (b)

Fig. 2. Rising edge slope estimation. (a) Direct estimation; (b) From DC delay change test.

As previously mentioned, the noise presented on the power rail will influence the output switching edge during the entire time range of the driver propagation delay T_{p0}, as illustrated in Fig. 3. In addition, the rise time of input signal is assumed to be negligible. Moreover, the amplitude of power noise is small so the jitter magnitude is proportional to noise amplitude. Under these conditions, if the period of the sinusoidal noise on the power rail is the same as the propagation delay of the driver, regardless of the actual value of the power rail noise at the time when output voltage is half V_{dd0}, the output switching edge delay time will not change. This is also true if the noise period is a multiple of the propagation delay. This is because the time averaged effect of the noise at this specific frequency is zero during the time range of the propagation delay [2,5]. For the PSIJ sensitivity derivation, this effect should be taken into consideration.

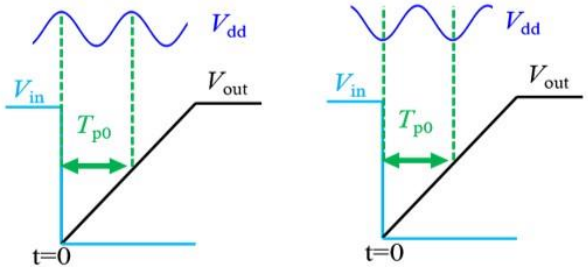


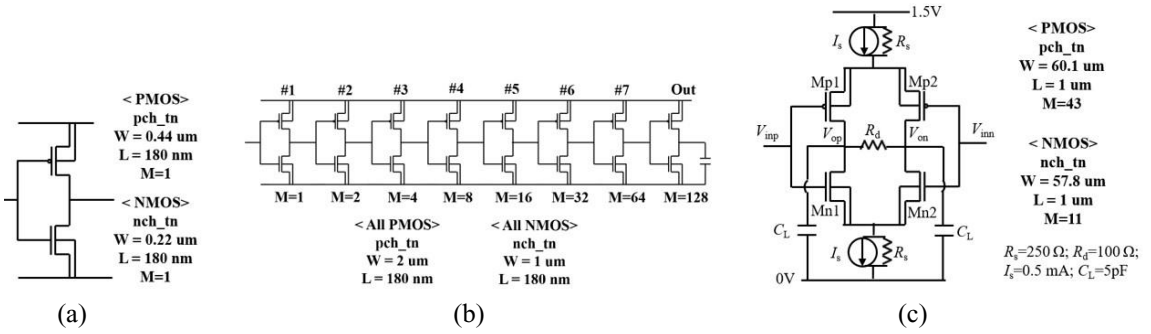
Fig. 3. Power noise time averaged effect during propagation delay.

Based on the above discussion, the PSIJ sensitivity formulation can be derived. Substituting (3) into (2) and taking the time harmonic form of *PSRR*(ω) for the time averaged effect consideration, the PSIJ sensitivity is expressed as follows:

$$PSIJsensitivity(\omega) = \int_0^{T_{p0}} \frac{PSRR(\omega)\cdot e^{j\omega t}}{Slope\cdot T_{p0}} dt = \frac{PSRR_p}{Slope} PSRR'(\omega) e^{j\frac{\omega}{2}T_{p0}} \mathrm{sinc}\left(\frac{\omega}{2}T_{p0}\right) \quad (4)$$

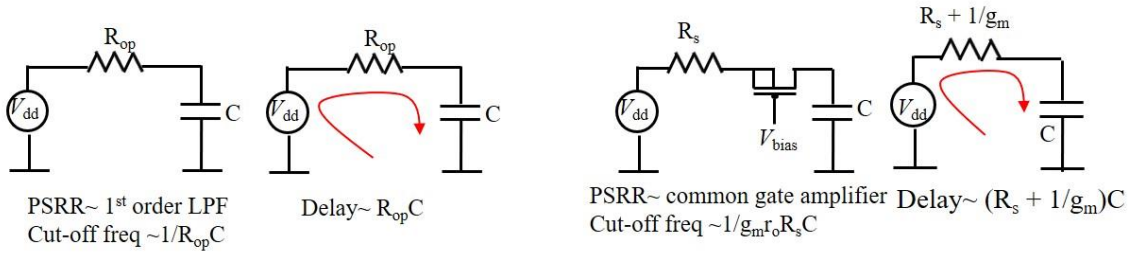
The left-hand side of (4) indicates the jitter sensitivity transfer function and can be a complex number. From (4), it can be observed that the PSIJ sensitivity is related to the DC jitter sensitivity and the frequency dependency originates from the normalized PSRR response and the time averaged effect induced sinc function portion. This sinc function portion is also shown in the previously derived expressions [2].

In this work, the proposed model is applied for the PSIJ analysis for the three different drivers as shown in Fig. 4. For different type of drivers, the PSIJ sensitivity frequency dependencies are expected to be different. Since the driver PSIJ sensitivity frequency behavior is related to the PSRR response and the propagation delay, the different PSIJ sensitivity frequency behavior can be understood by the analysis of PSRR response and the equivalent RC delay of the circuit, as illustrated in Fig. 5.



(a) (b) (c)

Fig. 4. Tested drivers. (a) Inverter; (b) Inverter chain; (c) Current mode differential driver.



(a) (b)

Fig. 5. Comparison of frequency dependency due to PSRR and propagation delay. (a) Inverter; (b) Differential driver.

The analysis for a single stage inverter is shown in Fig. 5(a). The PMOS can be regarded as a resistor when looking at the rising edge case. The PSRR analysis is close to the analysis for a first order low pass filter, with a cutoff frequency around $1/R_{op}C$, where R_{op} is the turn on resistance of PMOS. For the output delay of the inverter, it can be

roughly estimated as $R_{op}C$, and the corresponding frequency is the null frequency for the sinc function portion. In this case, the propagation delay related frequency roll-off is faster than the PSRR related frequency roll-off. As a result, the PSIJ sensitivity frequency dependency is dominated by the propagation delay related time averaged effect. For inverter chain, as the propagation delay is a linear accumulation of delay of each stage [7], the null frequency for the sinc function portion will be even smaller than the cutoff frequency of the PSRR response.

The analysis for current mode differential driver is shown in Fig. 5(b). For the designed driver, the transistors will have some amplification effects. For the simplest estimation, the PSRR analysis can be regarded as the analysis for a common gate amplifier. The cutoff frequency can be estimated as $1/g_m r_o R_s C$ [8], where g_m is the PMOS trans-conductance, r_o is the PMOS output resistance and R_s is the current source resistance. On the other hand, for the delay estimation, the transistor can be regarded as a resistor with value of $1/g_m$. So the propagation delay is roughly estimated as $(R_s+1/g_m)C$. In general, $g_m r_o R_s C$ is larger than $(R_s+1/g_m)C$ [8]. In consequence, the PSRR response will have smaller cutoff frequency and the PSRR frequency dependency will roll off faster than the propagation delay related sinc function frequency dependency.

In summary, for drivers working in the deep triode region, since the transistor can be treated as a resistor, the PSRR response frequency roll-off tends to be slower than the propagation delay related frequency roll-off. In this case, the PSIJ sensitivity frequency dependency is dominated by the propagation delay related time averaged effect. In addition, for drivers with multiple stages, as the total propagation delay is the accumulation of each single stage, the propagation delay related frequency roll-off tends to be faster than the PSRR related frequency roll-off. The PSIJ sensitivity frequency dependency will also be dominated by the propagation delay. On the other hand, for drivers working in the linear region or the saturation region, as the transistor has some amplification effects, the PSRR frequency roll-off tends to be faster than the propagation delay related frequency roll-off. The PSIJ sensitivity frequency dependency will be dominated by the PSRR response portion.

Validation on Different Drivers

Inverter

The proposed PSRR based PSIJ sensitivity model is firstly applied for a single stage inverter. The design parameters for the single stage inverter are shown in Fig. 4 (a). To obtain the PSRR response of the inverter, the circuit needs to be set to a proper DC status. For a single stage inverter, the power rail noise voltage will mainly influence the low-to-high transition. If the input switching edge transition time is assumed to be negligible, when the output transits from low to high, the input will always be low. For the PSRR simulation, the input is set to zero as plotted in Fig. 6. The nominal power rail voltage for this inverter is 1.8V and a sinusoidal source with 50mV amplitude is served as the noise source. The load capacitance for the test is set to 20fF. By conducting AC simulation and obtaining the ratio of the output voltage to the amplitude of sinusoidal noise

The simulated PSRR magnitude and phase for the inverter are shown in Fig. 7. At low frequency range, the magnitude of PSRR is one and at higher frequency range, the PSRR

begins to fall off. This is because for the PSRR simulation setup, the NMOS is set to off and PMOS is in linear region. At low frequency range, the PMOS is regarded as a resistor and the loading capacitor can be treated as open. As a result, the output will have the same amplitude as the input. With the increase of the frequency, the capacitor will start to take effect and the output voltage will begin to fall off.

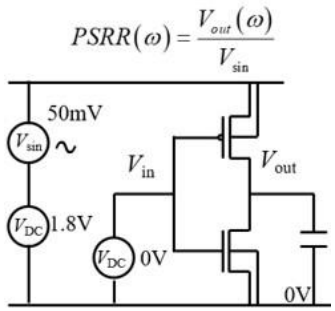


Fig. 6. PSRR simulation test for single stage inverter.

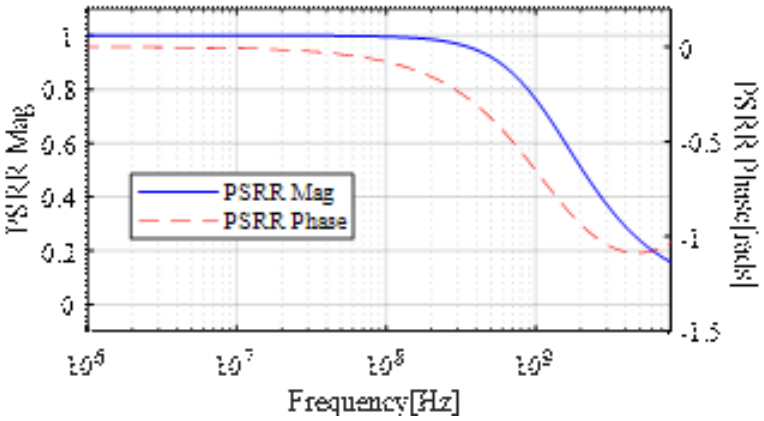
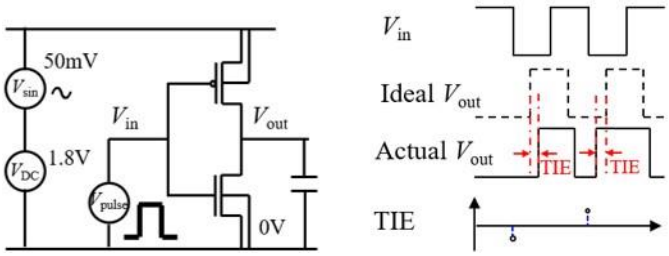


Fig. 7. PSRR simulation result for single stage inverter.

To validate the proposed PSIJ sensitivity expression (4), Hspice simulation is conducted to obtain the reference PSIJ sensitivity values at different frequencies. The simulation setup for jitter extraction is depicted in Fig. 8(a). In order to obtain both the magnitude and phase information, the TIE sequence is extracted as illustrated in Fig. 8(b). The TIE is calculated by subtracting actual output edge switching time from the ideal output edge switching. The obtained TIE value for each edge is plotted in time domain with respect to the input edge switching time, as in the derivation of (4), the time of input edge switching is treated as zero during the integration process. The extracted TIE sequence for the case with 100MHz power noise is shown in Fig. 9, from which the magnitude and phase of the PSIJ can be acquired. The comparison of the PSIJ sensitivity magnitude and phase results obtained from the PSRR based model and Hspice simulation are shown in Fig 10(a) and (b), respectively. The proposed PSIJ sensitivity model exhibits reasonably good estimation accuracy compared to the simulation results.



(a) (b)

Fig. 8. Simulation setup for jitter extraction. (a) Setup; (b) Extraction of TIE sequence.

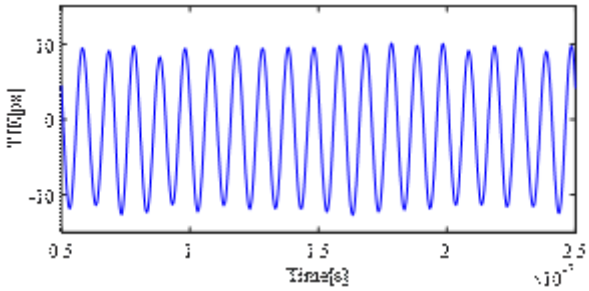
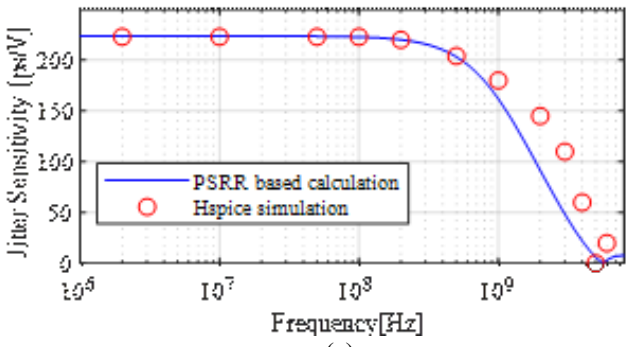
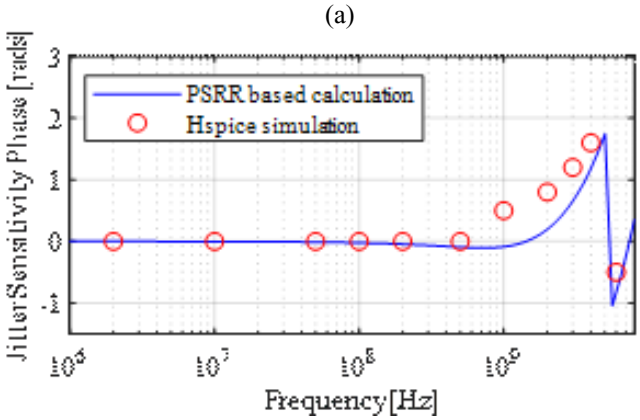


Fig. 9. Extracted TIE sequence for the case with 100 MHz power noise.



(a)



(b)

Fig. 10. Single stage inverter PSIJ sensitivity results comparison between PSRR based model and Hspice simulation. (a) Magnitude; (b) Phase.

Inverter Chain

The equation (4) can also be applied for inverter chain PSIJ sensitivity analysis with proper modification on the PSRR response and slope portion. Since each stage in the inverter chain will have their own PSRR response and slope, which will all contribute to the total PSIJ, the form of (4) needs to be adjusted accordingly. For the inverter chain, the total PSIJ at the final output stage can be obtained from the linear accumulation of local PSIJ at each stage [7], as illustrated in Fig. 11. Since the switching edge directions are opposite for the odd and even number stages in the inverter chain, the polarity of induced jitter for the adjacent stages will be opposite, as the slopes of rising and falling edges are opposite in sign.

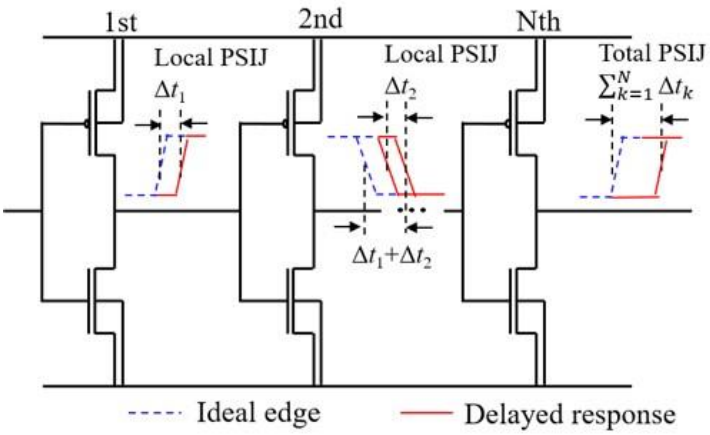


Fig. 11. Inverter chain total PSIJ as sum of each stage local PSIJ.

The design parameters for the tested inverter chain are shown in Fig. 4(b). The loading capacitance at the last stage is 10fF. This is an eight-stage inverter chain where each stage size is increased by the same factor of 2. For each stage, PMOS is twice the size of NMOS. For the inverter chain designed in this fashion, besides the last output stage, the propagation delay of #1 to #7 stages will be almost the same and the rising and falling edge propagation delays will also be very similar. In addition, the PSRR response of #1 to #7 stages are almost identical.

For each stage, the PSRR response for the rising edge case can be obtained by setting the input of each stage as low. The PSRR response for the falling edge case can be extracted by setting the input of each stage high. The PSRR response of each stage for both the rising and falling edges in the inverter chain are summarized in Fig. 12. The PSRR response for #1 to #7 stages are identical and are plotted in Fig. 12(a) while the last stage PSRR response is shown in Fig. 12(b).

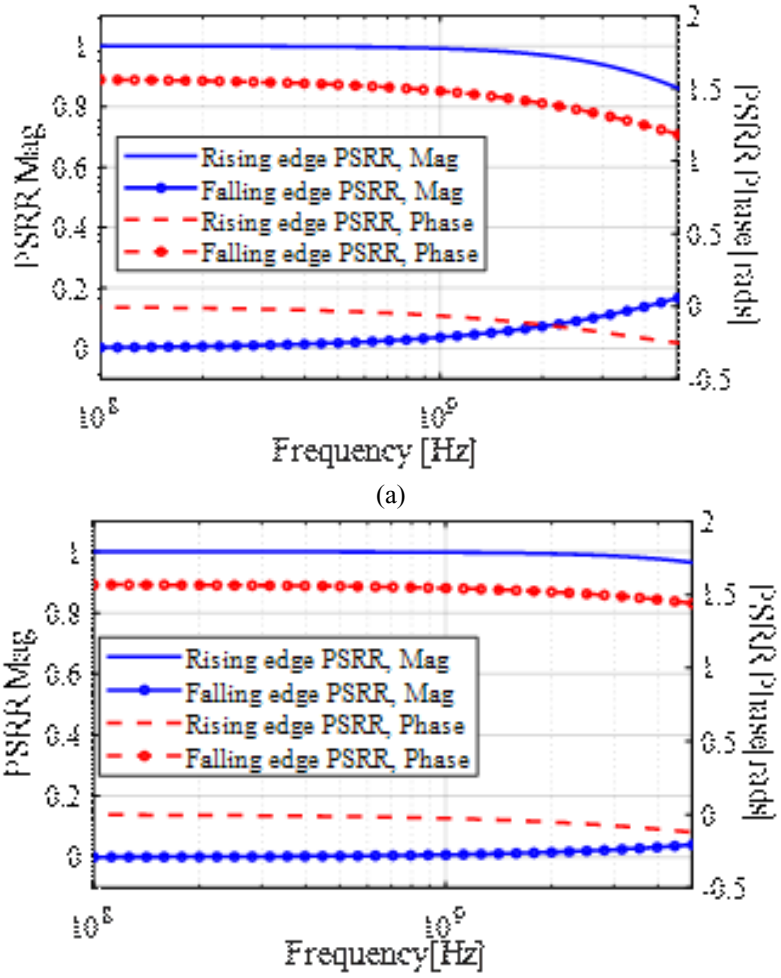


Fig. 12. PSRR for each stage in inverter chain. (a) #1-#7 stages; (b) output stage.

For the inverter chain output rising edge case, the total jitter can be calculated by the linear summation of the local PSIJ as follows:

$$\left.\frac{PSRR_p}{Slope}\right|_{\#1-\#7}\left(3\cdot PSRR'(\omega)_{rise}-4\cdot PSRR'(\omega)_{fall}\right)+\left.\frac{PSRR_p}{Slope}\right|_{Vout}PSRR'(\omega)_{rise}|_{Vout}$$
$$=\left.\frac{PSRR_p}{Slope}\right|_{\#1-\#7}A_{R\_\#1-\#7}'(\omega)+\left.\frac{PSRR_p}{Slope}\right|_{Vout}A_{R\_Vout}'(\omega) \quad (5)$$

The local PSIJ of each stage is expressed as the form of the DC performance portion multiplied with the normalized frequency dependency portion as shown in (2). Since the #1 to #7 stages share the same PSRR and rising/falling edge characteristics, the DC performance portion are the same and is written as $PSRR_p/Slope|_{\#1\text{-}\#7}$. On the other hand, the DC performance portion for the final stage is different and is expressed as $PSRR_p/Slope|_{Vout}$. For the case where the final output stage is rising, there will be four falling edges and three rising edges in the previous seven stages. All the rising edge stages will have the same normalized PSRR frequency dependency portion $PSRR'(\omega)_{rise}$,

while all the falling edge stages will have the same normalized PSRR frequency dependency portion $PSRR'(\omega)_{fall}$. The normalized PSRR frequency dependency portion for the last output stage is $PSRR'(\omega)_{rise}|_{Vout}$. The signs of local PSIJs for the adjacent stages are opposite and are explicitly expressed since the slope is treated as a magnitude value. For simplification, the normalized frequency dependency portion of the #1 to #7 stages is written as $A_{R\_\#1\text{-}\#7}'(\omega)$ and for the last stage the normalized frequency dependency portion is expressed as $A_{R\_Vout}'(\omega)$.

The DC performance portion can also be estimated by the DC delay change test. The DC performance portions for the #1 to #7 stages can be evaluated together. By recording the DC delay change at the #7 stage of the inverter chain, the DC jitter sensitivity for the stages from #1 to #7 is written as $(T_{\mathrm{pd,max}}- T_{\mathrm{pd,min}})/(V_{\mathrm{dd,max}}- V_{\mathrm{dd,min}})|_{\#1\text{-}\#7}$. Since the PSRR response for the falling edge case is zero at DC, the DC jitter sensitivity is determined by the three rising edge stages and it can be concluded as follows:

$$\left.\frac{PSRR_p}{Slope}\right|_{\#1-\#7} = \left.\frac{T_{pd\max}-T_{pd\min}}{V_{dd\max}-V_{dd\min}}\right|_{\#1-\#7} \Big/ 3 \tag{6}$$

The DC performance portion for the last stage can be extracted by isolating this stage and treat it as a single stage inverter, keeping the original loading capacitance. The DC performance portion is estimated as the DC jitter sensitivity of the output stage $(T_{\mathrm{pd,max}}- T_{\mathrm{pd,min}})/(V_{\mathrm{dd,max}}- V_{\mathrm{dd,min}})|_{Vout}$, as presented in equation 7.

$$\left.\frac{PSRR_p}{Slope}\right|_{Vout} = \left.\frac{1}{Slope}\right|_{Vout} = \left.\frac{T_{pd\max}-T_{pd\min}}{V_{dd\max}-V_{dd\min}}\right|_{Vout} \tag{7}$$

As all the stages in the inverter chain are consecutive in time, the time averaged effect of power rail noise should be considered in the propagation delay time range of the entire chain. Based on the above analysis, the application form of equation (4) for the inverter chain rising edge case is as follows:

$$PSIJsensitivity(\omega) = \left[\begin{array}{l} \left.\frac{PSRR_p}{Slope}\right|_{\#1-\#7} A_{R\_\#1-\#7}'(\omega) \\ +\left.\frac{PSRR_p}{Slope}\right|_{Vout} A_{R\_Vout}'(\omega) \end{array}\right] e^{j\frac{\omega}{2}T_{pR0}} \sin c\left(\frac{\omega}{2}T_{pR0}\right) \tag{8}$$

where T_{pR0} is the inverter chain propagation delay for the rising edge case. The PSIJ sensitivity formulation for the falling edge case can be derived similarly.

The obtained PSIJ sensitivity expressions for the rising and falling edge cases are validated using Hspice simulation. For rising edge, the comparison results of PSRR based model and Hspice simulation for PSIJ sensitivity magnitude and phase are plotted in Fig. 13 (a) and (b), respectively. For falling edge, the comparison results of PSRR based model and Hspice simulation for PSIJ sensitivity magnitude and phase are plotted in Fig. 14 (a) and (b), respectively. The proposed model can estimate the inverter chain PSIJ sensitivity with reasonably good accuracy for both the magnitude and phase.

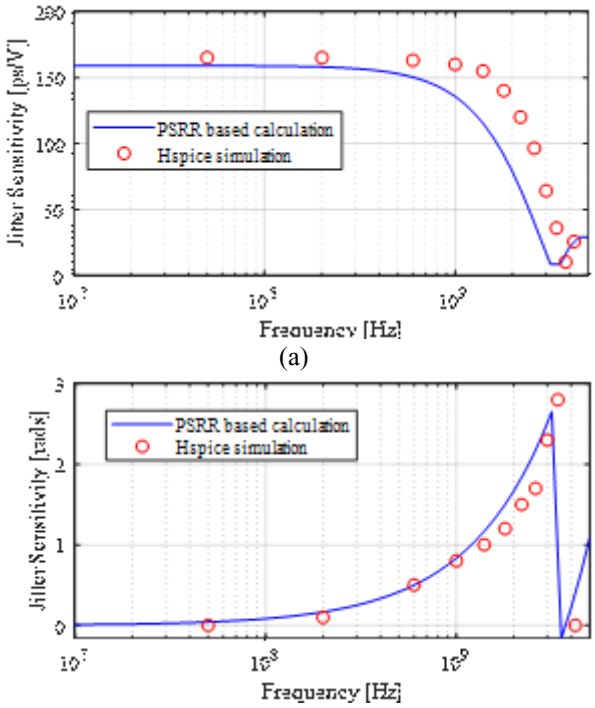


Fig. 13. Inverter chain rising edge PSIJ sensitivity simulation vs. model. (a) Magnitude; (b) Phase.

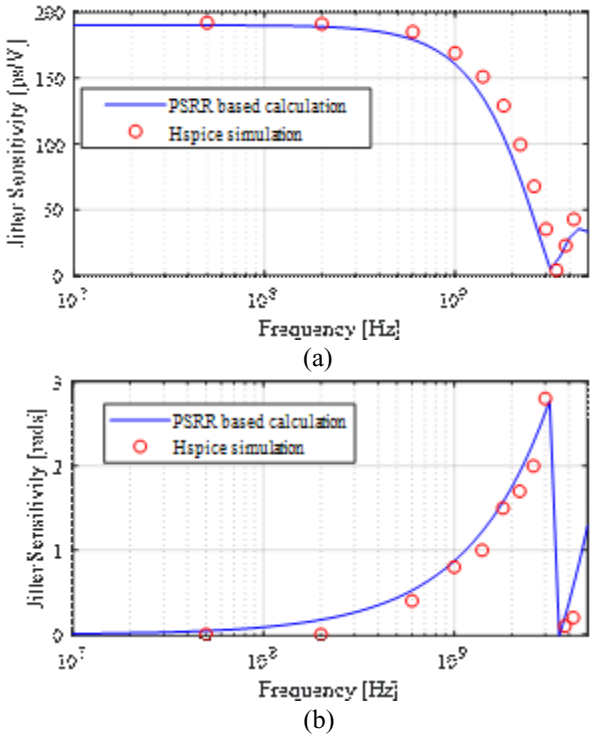


Fig. 14. Inverter chain falling edge PSIJ sensitivity simulation vs. model. (a) Magnitude; (b) Phase.

Current Mode Differential Driver

For current mode differential driver PSIJ sensitivity analysis, equation (4) can also be applied with proper modification on the PSRR response and slope portion. The PSRR response and slope of both the positive node and negative node need to be considered for PSIJ analysis. Since the slope of the positive node and negative node may be different, if only differential output PSRR response and slope is considered, the effect of the different slope in the positive and negative node to the PSIJ will be missed. The design parameters for the current mode differential driver are shown in Fig. 4(c). The nominal power rail voltage is 1.5V. The voltage levels for the single ended output are designed to be 0.625V for the low state and 0.875V for the high state. The differential output swing will be 500mV.

In order to obtain the PSRR response of the current mode differential driver, the circuit needs to be set to a proper DC status, as the input switching time is assumed to be negligible. The differential driver is switching between two DC statuses. For the case where the positive side input is low and the negative side input is high, the magnitude and phase of the PSRR response are plotted in Fig. 15(a). For the case where the positive side input is high and the negative side input is low, the magnitude and phase of the PSRR response are plotted in Fig. 15(b). At a fixed DC status, the PSRR response for the positive and negative side are different. It should be noted that even though the PSRR response will change for the positive and negative side output when the DC status changes, eventually only two PSRR response will be obtained, as Mp1 and Mp2 are the same and Mn1 and Mn2 are also the same. The PSRR response with larger value is denoted as $PSRR_{nl}= V_{nl}/V_{sin}$, where V_{sin} is the amplitude of the power rail noise. The PSRR response with smaller value is written as $PSRR_{ns}=V_{ns}/V_{sin}$.

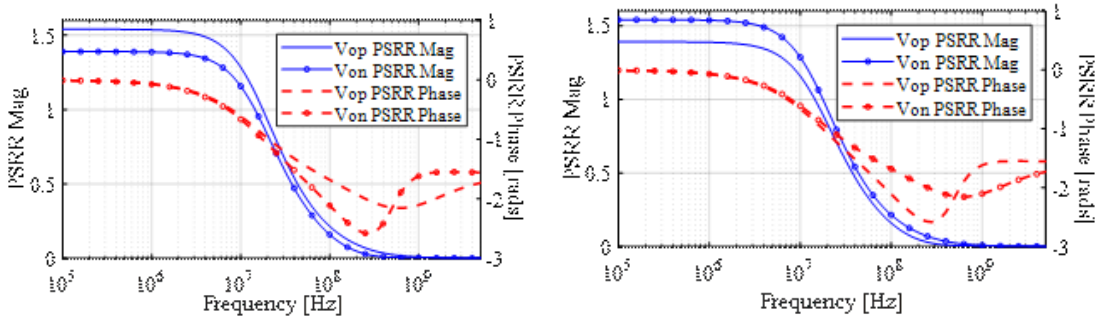


Fig. 15. PSRR of differential driver. (a) Positive input low, negative input high; (b) Positive input high, negative input low.

The process to derive the differential TIE from PSRR response is illustrated in Fig. 16. The positive and negative node output with ideal power voltage are denoted as *OP* and *ON*, respectively. The voltage value for the low and high states are denoted as V_2 and V_1, respectively. The crossing time location of *OP* and *ON* under the nominal power voltage is denoted as t_c. The crossing voltage level at t_c is represented as V_{cross}. When the power voltage is increased, the changed positive and negative node output are indicated as *OP*' and *ON*', respectively. The difference between the new crossing time location t_c' and the original t_c is the differential output TIE. At the original t_c, *OP*' will increase to V_{pnx} while

ON' will increase to V_{nnx}. The *OP*' and *ON*' crossing point, *OP*' and t_c crossing point, as well as *ON*' and t_c crossing point has formed a triangle. The length of the triangle vertical edge is V_{pnx}-V_{nnx} and differential TIE will be the height at this edge. The slope of the other two edges in the triangle are *SR* and *SF*, which are the magnitude of the rising and falling edge slope. From basic geometry theory, the differential TIE can be calculated as (V_{pnx}-V_{nnx})/(*SR*+*SF*). For simplicity, the *SR* and *SF* are assumed to be obtained under nominal power voltage. Similarly, the original crossing time t_c, can be expressed as (V_2-V_1)/(*SR*+*SF*). From this analysis, it is clearly shown that the differential TIE is related to the PSRR response and the rising/falling edge slopes.

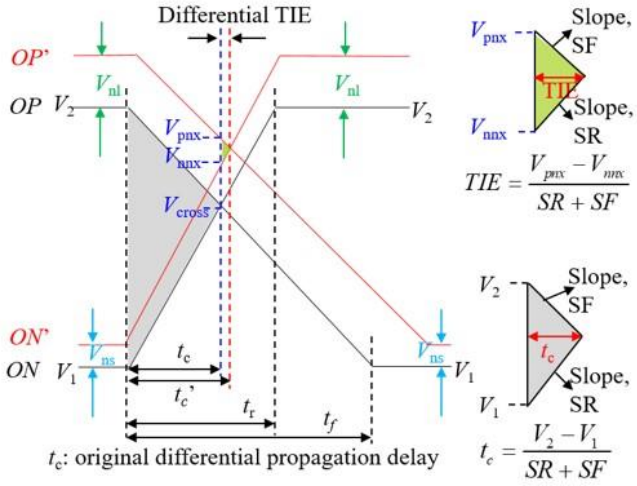


Fig. 16. Differential driver output TIE analysis illustration.

The V_{nnx} can be estimated as

$$V_{nnx} = V_{cross} + V_{ns} + V_{nl}\frac{t_c}{t_r} = V_{cross} + V_{ns} + V_{nl}\frac{SR}{SR+SF} \tag{9}$$

when the power rail voltage is increased, before transition, *ON*' will increase by V_{ns} compared to *ON*. After transition, for the flipped DC status, *ON*' will increase by V_{nl}, compared to *ON*. During the transition, the negative node rising edge slope will also increase due to the PSRR response. At the original crossing time t_c, the voltage increase due to the increase of rising edge slope is estimated as $V_{nl}(t_c/t_r)$, where t_r is the time when the negative node output changes from V_1 to V_2 and can be written as (V_2-V_1)/*SR*. Plus the initial increase V_{ns}, V_{nnx} will be V_{cross}+ V_{ns}+ $V_{nl}(t_c/t_r)$.

Similar analysis is carried out for *OP*' and the V_{pnx} is expressed as follows:

$$V_{pnx} = V_{cross} + V_{nl} + V_{ns}\frac{t_c}{t_f} = V_{cross} + V_{nl} + V_{ns}\frac{SF}{SR+SF} \tag{10}$$

Plug V_{pnx} and V_{nnx} values in the differential TIE expression, normalize to the amplitude of power rail noise, extract the DC performance portion and consider the time averaged effect, the application form of equation (4) for the current mode differential driver is derived as follows:

$$PSIJsensitivity(\omega)=\frac{PSRR_p}{SF+SR}\begin{pmatrix}(1-\frac{SR}{SR+SF})PSRR_{nl}{}'(\omega)\\-(1-\frac{SF}{SR+SF})PSRR_{ns}{}'(\omega)\end{pmatrix}e^{j\frac{\omega}{2}T_{p0}}\sin c\left(\frac{\omega}{2}T_{p0}\right) \quad (11)$$

T_{p0} is the differential output propagation delay. The DC performance portion is estimated with the differential output DC jitter sensitivity as:

$$\frac{PSRR_p}{SF+SR}=\left|\frac{T_{pd\max}-T_{pd\min}}{V_{dd\max}-V_{dd\min}}\right| \quad (12)$$

The normalized PSRR frequency dependency portion are $PSRR_{nl}$' and $PSRR_{ns}$' for $PSRR_{nl}$ and $PSRR_{ns}$, respectively.

From (11), the influence of PSRR and transition edge slope of the positive and negative nodes can be evaluated. If the PSRR of the negative node and positive node are the same, and the magnitude of *SR* and *SF* are also the same, the differential TIE should be zero; If the PSRR responses are the same but the *SR* and *SF* are different, the differential TIE will appear and is proportional to $PSRR(SR\text{-}SF)/(SR+SF)^2$; If the slopes are the same but the PSRR responses are different, the differential TIE will also exist and is proportional to $0.5(PSRR_{nl}\text{-}\ PSRR_{nl})/(2\text{Slope})$.

The PSIJ sensitivity expression for the current mode differential driver is also validated by comparison with the Hspice simulation results. The PSIJ sensitivity magnitude and phase are plotted in Fig. 17(a) and (b), respectively. The results from PSRR based calculation match reasonably well with the one obtained from transistor circuit simulation.

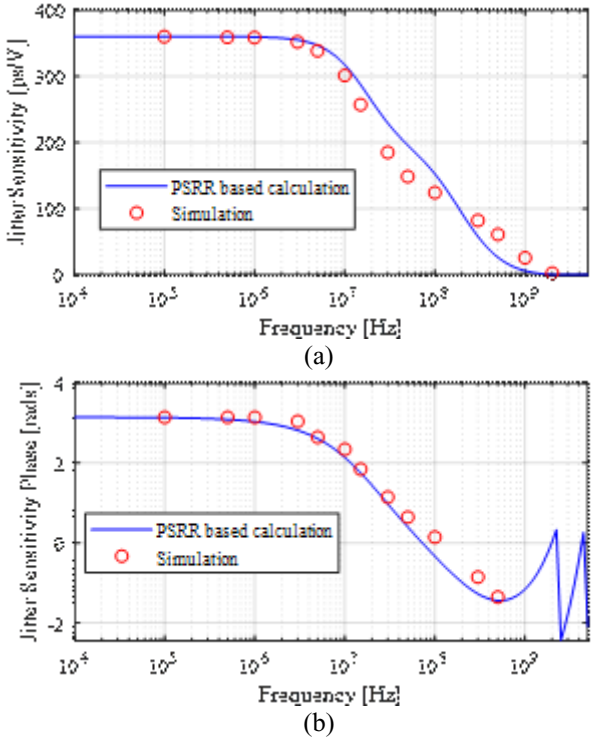


Fig. 17. Differential transmitter PSIJ sensitivity simulation vs. model (a) Magnitude; (b) Phase.

Conclusion

The PSIJ sensitivity model based on PSRR response is derived and validated using Hspice simulation. The obtained PSIJ sensitivity formulations contain both the magnitude and phase information. The proposed PSIJ sensitivity model can be generalized for the PSIJ study of different type of drivers. In general, the PSIJ sensitivity for different type of drivers is related to the PSRR response, transition edge slope and the propagation delay. With the proposed model, the factors influencing the PSIJ sensitivity behavior for different type of drivers can be clearly identified.

Acknowledgment

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