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Analysis of Electro-static Discharge to Through-silicon Via

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Abstract

This paper proposes the methodology to analyze electro-static discharge (ESD) to through-silicon via (TSV) under transmission line pulse (TLP) testing. Following the ESD test features, ESD to TSV characteristics under different voltage levels and rise time are analyzed. The ESD coupling model on TSV structure is proposed with respect to different TSV oxide capacitance and depletion effect depending on the bias voltage on the TSV. The models are applied to simulations to investigate the effectiveness and limitations. This model proposed one potential mitigation method for reducing ESD coupling effect.

Authors' Biography

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Introduction

Limited research on ESD to on-chip structures increases the level of difficulty to apply system level ESD design methodology to on-chip structures. Analysis of ESD to on-chip structures proposes guideline for reducing ESD effect on on-chip structures. As one example of on-chip structures, through-silicon via (TSV) technology is widely utilized in various 2.5-D and 3-D IC design [1]. Therefore, the impact of ESD on TSV requires a systematic evaluation approach to help provide a TSV design guide to reduce ESD effects. If the approach to reducing ESD effects on TSV is contrary to the merits of TSV technology (e.g., lower RC delay and lower input-output power consumption), then the TSV design guidelines should be modified to provide ESD immunity with minimal impact on the benefits of TSV technology. However, an approach that is highly compatible with the benefits of the technology will be the best choice for technology development.

In order to systematically evaluate the ESD effects on TSV structures, transmission line pulse (TLP) tests are applied to TSV structures. By applying the TLP test, the model investigates the ESD effect under different conditions, such as voltage level and rise time. The relationship between the ESD-induced current and different geometric design parameters of the TSV structure is modeled and verified by measurements, considering the depletion effect caused by the bias voltage. In addition, a trend analysis of the peak of the coupled waveform is presented to investigate the determinants of ESD coupling to the TSV.

This model provides insight on ESD coupling in the TSV structure for the first time. According to the analysis, a potential mitigation method for reducing ESD coupling effect is provided.

ESD to TSV Characterization Methodology

TSV coupling is mainly through the oxide of TSV and silicon substrate. In real products, there are two main types of coupling: TSV-TSV coupling and TSV-substrate contact coupling [2]. To simplify the problem, we focus on TSV-substrate contact coupling and study the effect of how ESD pulses pass through a typical TSV structure within a 3D IC product.

As shown in Fig. 1, the TSV structure consists of the TSV, the silicon oxide surrounding the TSV, the substrate contact, and the silicon substrate filling the rest of the space. For frequency domain measurements, DC bias and AC inputs are added to the top of the TSV and the substrate contact will be used as the second port. For time domain measurements, TLP injection is applied to the TSV section and the coupled waveform is monitored by a time domain measurement device connected to the substrate contact.

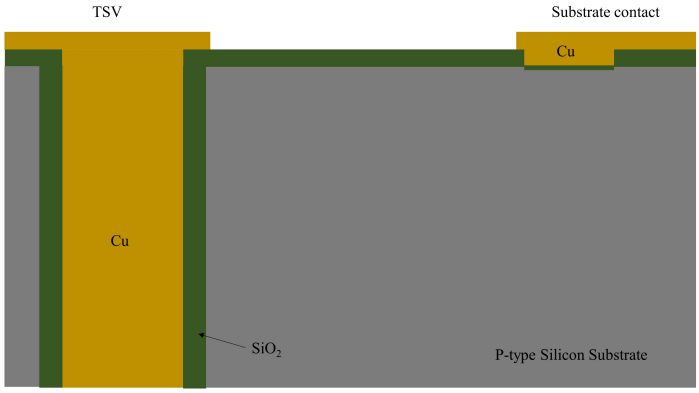
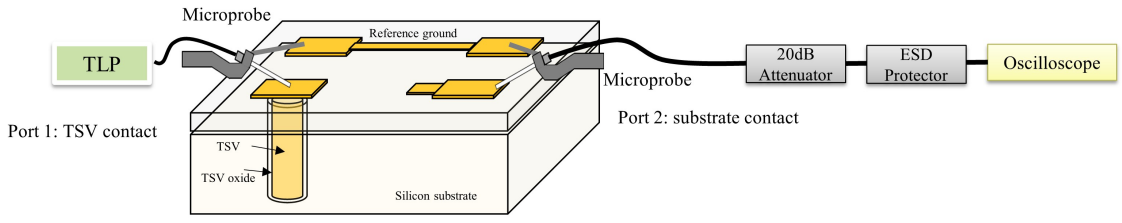


Fig. 1. Cross Section of the TSV-substrate contact samples.

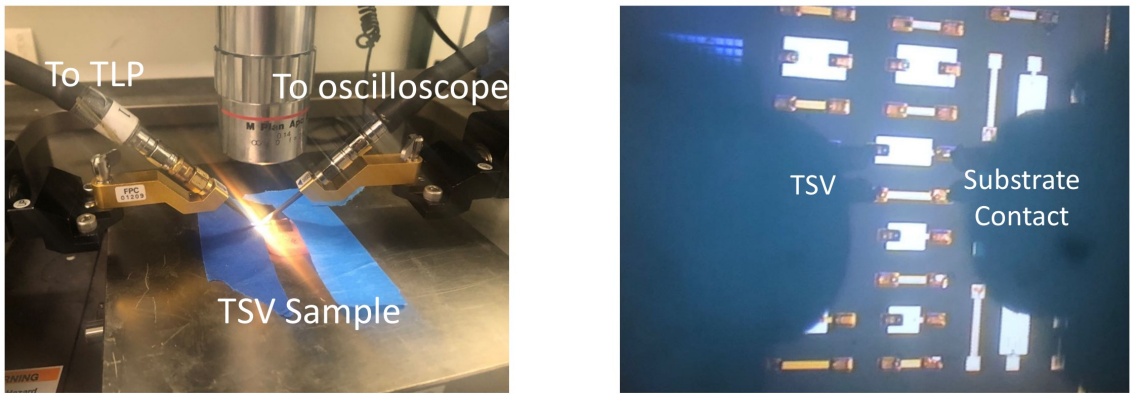
Referring to previous work on TSV structures [3], the coupling depends mainly on the oxide capacitance of the TSV and silicon substrate. It can be described as a capacitor in series with another capacitor, in parallel with a resistor. The TSV oxide capacitance can be divided into the oxide capacitance, C_{ox} and depletion capacitance, C_{depl}. When bias voltage changes, the depletion region thickness changes as well. Since C_{depl} is in series with C_{ox}, and C_{depl} is much smaller than C_{ox}, the change of C_{depl} will directly affect the total capacitance and change the coupling signal accordingly. Therefore, the bias voltage added to the TSV sample also contributes to the variation of the coupling. In the previous paper, a capacitance-voltage hysteresis model was proposed [4], but the effect caused by the hysteresis model on the coupled waveform was not analyzed in depth.

Analysis of coupling type

To investigate the type of coupling of ESD stresses through the TSV, the measurement setup shown in Fig. 2 was used to observe the coupling signal. The TLP-1000 was used to generate transmission line pulses to the TSV contact pad; the R&S RTO 1024 2GHz oscilloscope was used to observe the coupled waveform from the substrate contact. To protect the oscilloscope from potential breakdown discharges, a 20 dB attenuator and an ESD protector were connected to the oscilloscope's channels.



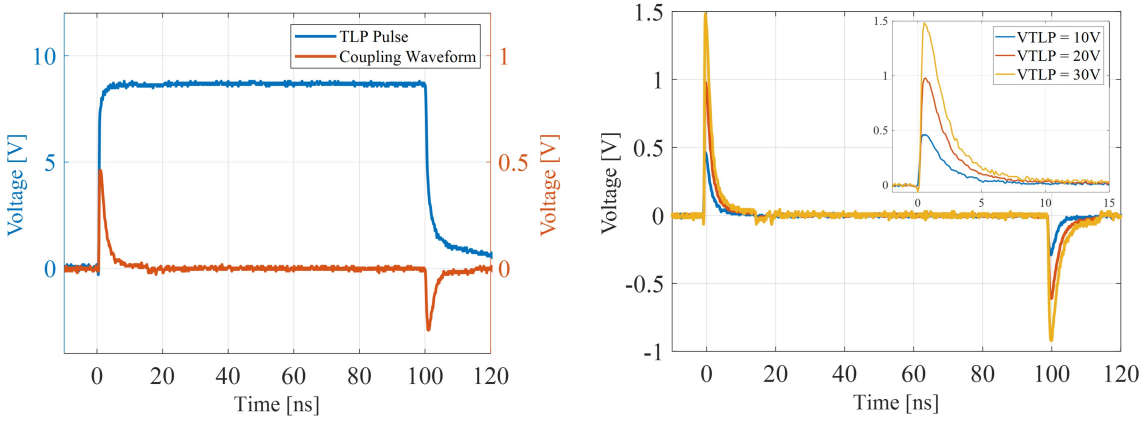
(a) Measurement setup diagram



(b) Use microprobe to contact the samples and use microscope to observe the landing

Fig. 2. Measurement setup for the analysis of coupling types.

The TLP pulse is generated by charging and then discharging a particular long cable. The pulse is a square wave-like pulse with 100 ns pulse width. The rise time of the pulse is about 850 ps, and the minimum output TLP level is set to about 9 V. A comparison of the original TLP pulse and the coupled waveform is shown in Fig. 3(a). The coupled waveform shows only the rising and falling edges of the TLP pulse. This behavior provides evidence that the coupling of ESD stress depends on the capacitive part of the path from the TSV to the substrate contact. The dominant part of the pulse is the edge in the coupling event, as well as the rise time/fall time.



(a) TLP Pulse vs. Coupled Waveform

(b) Coupled waveforms at different VTLP level

Fig 3. Waveform comparison. (a) The TLP pulse and the corresponding coupled waveform are compared. The peak of the coupling signal is around 5% of the TLP level. (b) Coupled waveforms under different discharge TLP levels. The peak of the signal is proportional to the discharge level.

Depending on the characteristics of the capacitive coupling, the peak is determined by the capacitance and the dv/dt of the original TLP pulse. Another test, i.e., applying different discharge levels, is performed to investigate deeply the trending behavior of the ESD coupling results. From Fig. 3(b), we can easily find that the peak of the signal is proportional to the discharge level. However, in order to determine the exact factors of ESD coupling, the test needs to involve more validation methods.

From the two measurement cases shown above, we can come up with the following conclusion:

- When ESD pulse passes through the TSV structure, noise coupling will occur and it's capacitive coupling.
- The coupling's dominant factors are the capacitance and the dv/dt.

Once the type of coupling has been determined, measurements can be continued to find out the relationship between the factors of TSV, the characteristics of the ESD pulse and the coupling signal.

Investigation on the factors of ESD to TSV

While previous measurements provide some support that coupling should depend on capacitance and dv/dt values, the results are not strong evidence. To dig deeper into the real factors, we propose an improved measurement setup to observe the relationship between the factors and the coupling signal. In Fig. 4, the substrate contact part is kept the same while some changes are made from the source side.

As described in the previous section, the depletion region of the TSV can be changed by adding a bias voltage to the TSV, which in turn changes the entire capacitance of the outer layer of the TSV. Thus, a bias tee is used to combine the dc supply and the TLP signal, and then injected into the TSV. Furthermore, while changes in discharge level cause changes in dv/dt, the measurements shown in Fig. 3(b) do not provide strong evidence that dv/dt is the exact factor in coupling. To provide stronger evidence, the setup here fixes the discharge level and varies the rise time. Three rise time filters are used at the output of the TLP, namely 1ns, 5ns and 10ns rise time filters. And according to the previous results, high level of TLP can easily lead to breakdown of the oxide, and in this test, multiple discharges were needed. Therefore, a 20dB attenuator was also added to the output of the TLP to reduce the level of the TLP to avoid damaging the TSV sample.

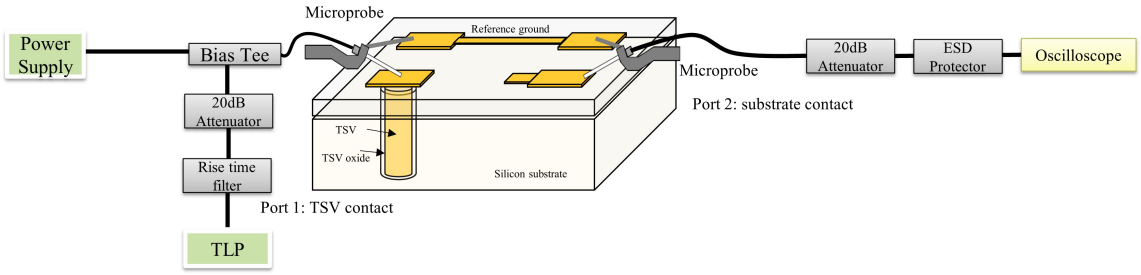


Fig. 4. Measurement setup for investigation on rise time and bias voltage

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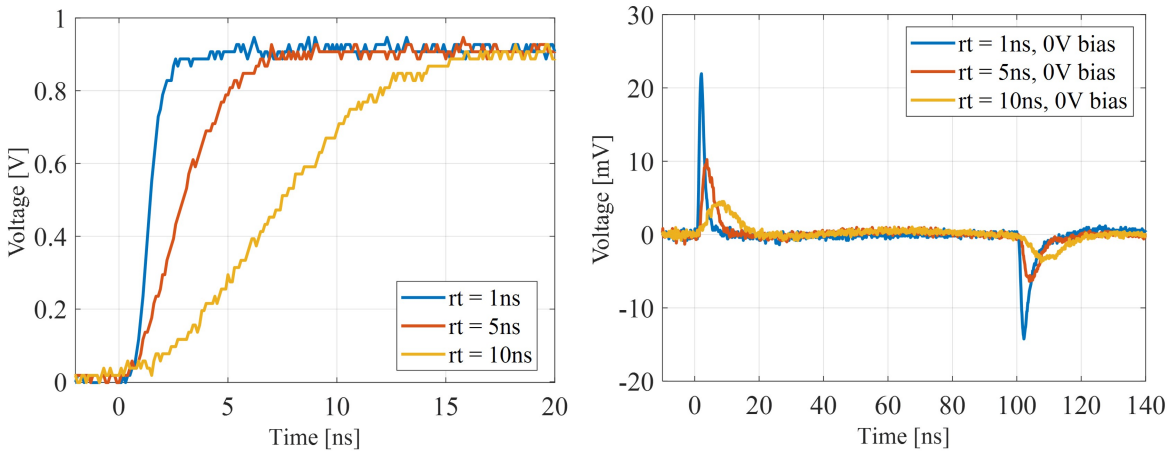
A. Rise Time Test

There are three types of rise time filters: 1ns, 5ns and 10ns. The rise time is defined as the time taken by the pulse to change from 10% of the peak to 90% of the peak. The filter slows down the rise time of the TLP pulse but maintains the level of the original output. Fig, 5(a) shows the rising edge of the pulse at the output of the rising time filter. Fig. 5(b) shows the waveform observed from the substrate contact. According to the observation in the first part, the dv/dt value is one of the factors for the peak of the coupled waveform. Compared to Fig. 3(b), the result shown in Fig. 5(b) indicates that dv/dt does contribute to the final peak, but the change in rise time also affects the rising edge of the coupled waveform. This should be related to the secondary derivation of the voltage to substrate contact on TSV



(a) Original TLP pulse with different rise time

(b) Coupled waveforms with different rise time

Fig. 5. Test with different rise time. (a) The original TLP pulse with different rise time. (b) The corresponding coupled waveforms when using different rise time.

B. Different Bias Voltage Test

In [4], the capacitance-voltage hysteresis model has been discussed and extracted. Different bias voltages show different depletion capacitances and in turn affect the capacitance of the whole TSV. Following the same steps, the hysteresis model of the TSV sample is modeled in this section using the setup shown in Fig. 4. This hysteresis model matches the model shown in [4].

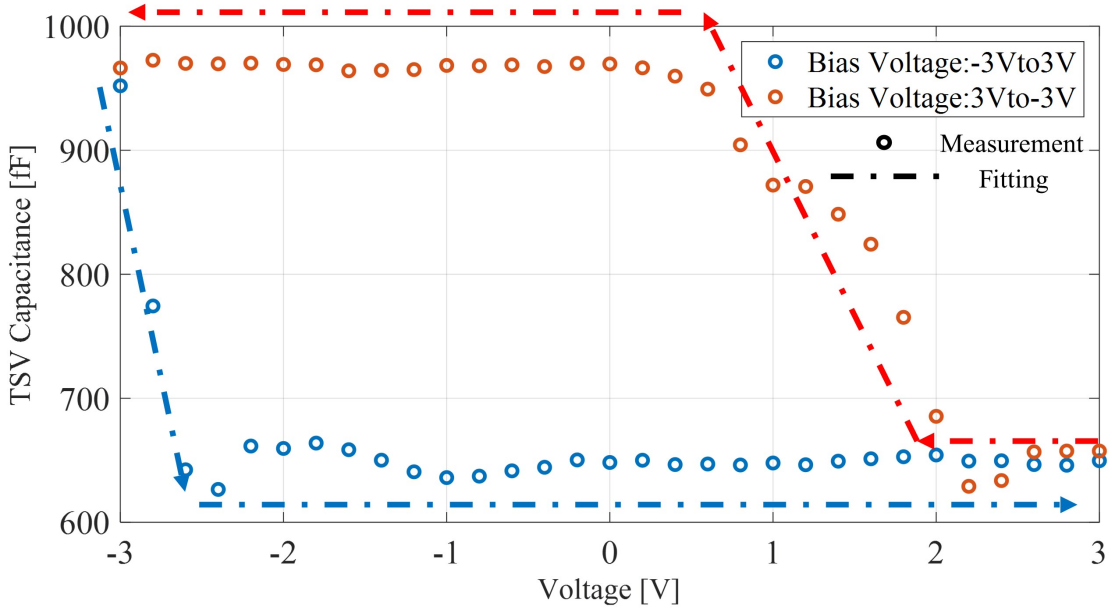
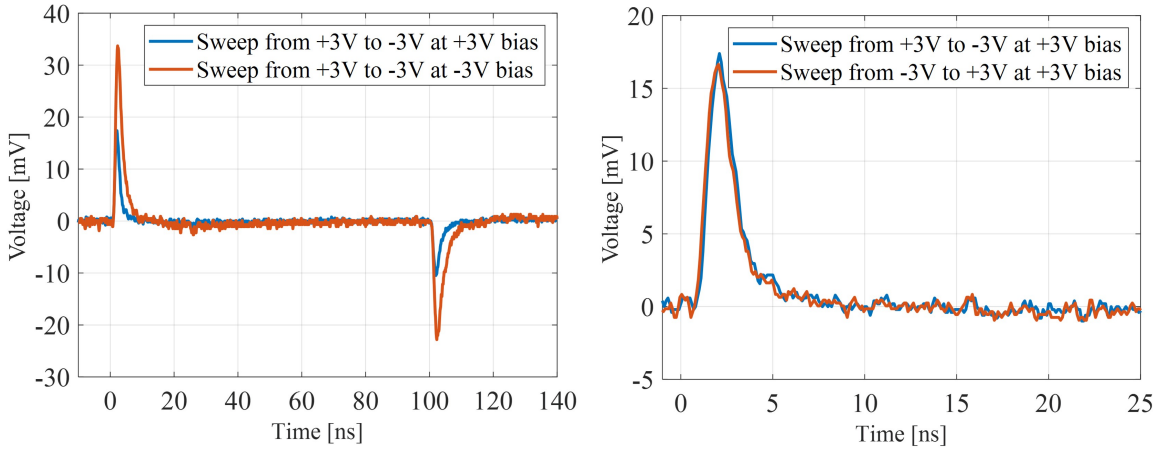


Fig. 6. Capacitance-Voltage Hysteresis Model for the TSV sample at 10MHz

To verify the role of capacitance in the coupling process, TLP tests are done at different bias voltages and different bias voltage sweep directions. In Fig. 7(a), the sweep direction is from +3V to -3V, and the discharge occurs at each end of the sweep range. When sweeping through the bias voltage, the TSV capacitance varies according to the depletion region. This result demonstrates that the capacitance directly affects the coupling waveform. In Fig. 7(b), the coupling results at the beginning of the sweep from +3V to -3V and at the end of the sweep from -3V to +3V show that the coupling remains constant when the depletion region is recovered. However, this result is based on the condition that the maximum ESD voltage does not exceed the breakdown voltage of the TSV oxide. Once the breakdown voltage is reached, the ESD stress can easily pass through the silicon substrate and discharges directly into the active circuit connected to the substrate contact.



(a) Coupled waveforms when applying +3V and -3V bias voltage

(b) Coupled waveforms at different time of the sweep procedure

Fig. 7 . Coupled waveforms considering the bias voltage. (a) The coupled waveforms when sweeping from +3V to -3V and discharge at +3V and -3V. The waveform shows the impact of the depletion region to the coupling signal. (b) The coupled waveforms at the same +3V bias but one is at the beginning of the sweep and another is at the end of sweep. This result shows the depletion recovery won't affect the coupling result.

From the two tests down, the conclusions can be described in detail:

- Within the tolerance of the voltage applied to the TSV [5], the capacitive coupling will depend mainly on the TSV capacitance formed by the oxide and depletion capacitance in terms of the TSV structure. The bias voltage added to the TSV will significantly change the total capacitance of the TSV and affect the results. Therefore, the ESD coupling will vary considerably at different operating bias voltage levels.
- Taking ESD pulses into account, the rising edge dominates when the ESD voltage does not exceed the breakdown voltage of the TSV oxide. Therefore, the two main aspects worth considering when suppressing ESD coupling are slowing down the rise time and directly suppressing the signal in the path from the TSV to the silicon substrate.

ESD to TSV SPICE Model

The SPICE model of ESD coupling in the TSV structure is proposed. Disregarding the attenuator and ESD protector, it consists of two parts: the ESD source and the victim.

The first part is the source. As a transmission line pulse generator, it will be charged to the designed voltage level and then discharges to the victim. It can be equated to a simple square pulse source with a 50-ohm resistance. The instrument used in this measurement

has a 200ps rise time filter and a 3dB attenuator inside the instrument. A compensation parameter was applied to the voltage level of the TLP to obtain good matching results.

The second part is the victim: TSV-substrate contact model. This part has been modeled in [4]. With the capacitance of the TSV (both oxide capacitance and depletion capacitance) and the silicon substrate part in series. The silicon substrate can be described as the substrate capacitance in series with the substrate resistance.

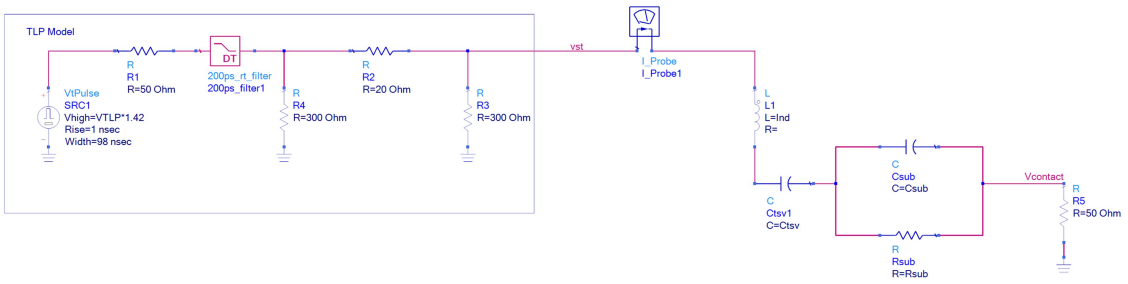
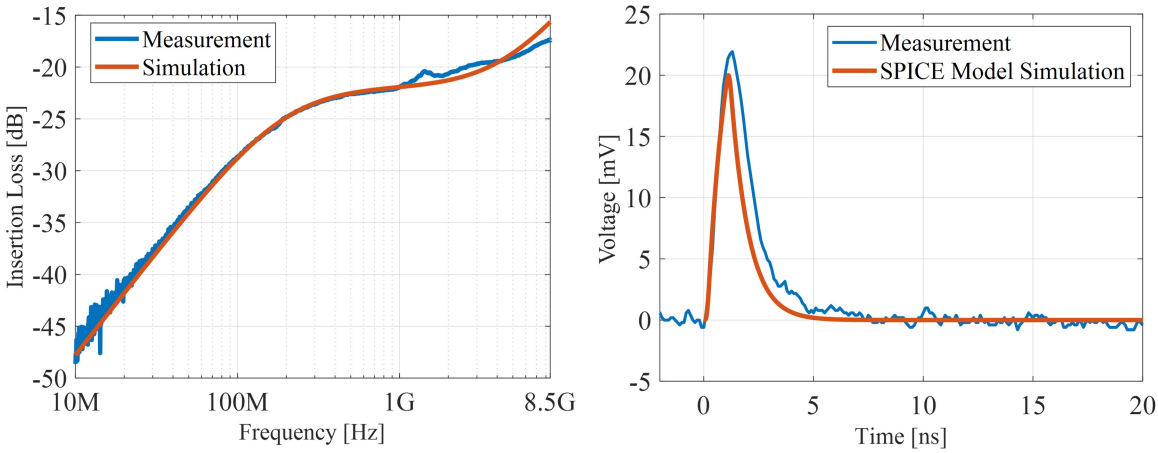


Fig. 8. ESD to TSV SPICE Model

The entire SPICE model of TLP discharge to TSV-substrate contact is shown in Fig. 8. The values of C_{tsv}, C_{sub} and R_{sub} need to be adjusted to match the insertion loss (S_{21}). The unknown values of the variables can be extracted by adjusting the results to match S21, as shown in Fig. 9(a). In this case, the inductor does not significantly affect the coupling results. At 0V bias and 10MHz, the extracted variables are: C_{tsv} = 650fF, C_{sub} = 31fF, R_{sub} = 1105Ohm. By applying the extracted variables to the SPICE model, we can generate the coupled signal and see a perfect match to the measured results in Fig. 9(b).



(a) Insertion Loss of the TSV to substrate contact

(b) SPICE Simulation and measured coupled waveform

Fig. 9. SPICE Model simulation result. (a) Tune C_{tsv}, C_{sub} and R_{sub} to get a good match to the Insertion Loss. (b) Apply the tuned value back to the TLP discharge to TSV SPICE model and compared with the measurement. It shows a good match as well.

Mitigation Method for Reducing ESD coupling in TSV structure

From the analysis above, we can derive a method to mitigate ESD coupling based on the TSV structure. The shield of the TSV is an oxide along with the silicon substrate. Around each TSV, the expected signal always passes directly with the TSV and the signal line, so we can design a different structure around the TSV to help mitigate the unwanted coupling while protecting the original signal from being suppressed.

Around the TSV, there will be enough area for a cylindrical ring. After passing through the oxide of the TSV, the ESD coupling will pass through the silicon substrate. If there is a cylindrical ring attached to the oxide of the TSV with n-type doped silicon, the structure could form a PN junction with the p-type doped silicon substrate.

As shown in Fig. 10, an additional cylindrical ring is added around the depletion region of the TSV, and this structure forms a PN junction and additional junction capacitance in the travel path from the TSV to the substrate contact. The PN junction enhances the robustness of the outer shield of the TSV and provides mitigation of coupling accordingly. This structure utilizes the extra space around the TSV within the silicon substrate and does not affect the RC delay and input-output power consumption in the 3D-IC system.

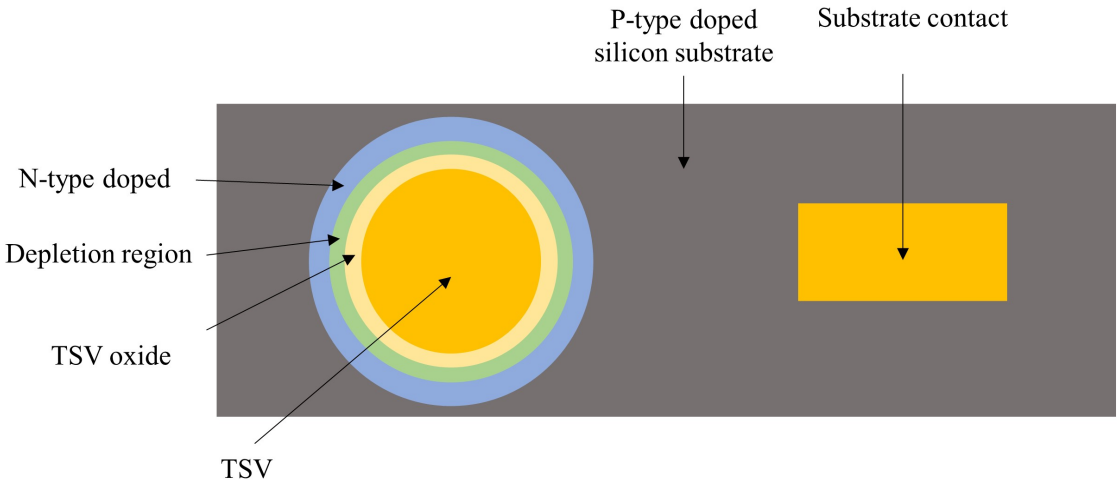


Fig. 10. Potential mitigation structure to reduce the coupling from TSV to substrate contact. Top view of the TSV-substrate contact structure. Add another layer of N-type doped silicon around the TSV oxide.

Summary

This paper proposes a method to analyze ESD to TSV under TLP testing. Applying different test levels and rise times and considering the dv/dt values, it can be concluded that the coupling is a capacitive behavior. Based on the capacitance-voltage hysteresis model of TSV, the coupling waveforms at different bias voltages are analyzed. The depletion capacitance greatly affects the total capacitance of the TSV and the coupling results accordingly. To improve the robustness of the TSV structure, we propose a structure with n-type doped silicon enclosed on the TSV. The additional cylindrical ring with the p-type silicon substrate can form a PN junction to help suppress the coupling while avoiding the suppression of the desired signal.

Acknowledgment

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Reference

[1] A. W. Topol et al., “Three-dimensional integrated circuits,” IBM J. Res. Develop., vol. 50, nos. 4–5, pp. 491–506, Jul./Sep. 2006

[2] J. Cho et al., "Modeling and Analysis of Through-Silicon Via (TSV) Noise Coupling and Suppression Using a Guard Ring," in IEEE Transactions on Components, Packaging and Manufacturing Technology, vol. 1, no. 2, pp. 220-233, Feb. 2011

[3] J. Cho et al., "Through-silicon via (TSV) depletion effect," 2011 IEEE 20th Conference on Electrical Performance of Electronic Packaging and Systems, 2011, pp. 101-104

[4] D. -H. Kim et al., "Through-Silicon Via Capacitance–Voltage Hysteresis Modeling for 2.5-D and 3-D IC," in IEEE Transactions on Components, Packaging and Manufacturing Technology, vol. 7, no. 6, pp. 925-935, June 2017

[5] H. Choi, S. Choi, M. Yeo, S. Cho, D. Baek and J. Park, "An experimental study on the TSV reliability: Electromigration (EM) and time dependant dielectric breakdown (TDDB)," *2012 IEEE International Interconnect Technology Conference*, 2012, pp. 1-3