Multi-Channel Monolithic-Cascode HEMT (MC^2-HEMT): A New GaN Power Switch up to 10 kV

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Abstract—This work presents a new device concept, the Multi-Channel Monolithic-Cascode high-electron-mobility transistor (MC^2-HEMT), which monolithically integrates a low-voltage, enhancement-mode (E-mode) HEMT based on single 2DEG channel and a high-voltage, depletion-mode (D-mode) HEMT based on stacked 2DEG multi-channel. This device can exploit the low sheet resistance of the multi-channel, realize an E-mode gate control, and completely shield the gate region from high electric field. It also obviates the need for nanometer-sized fin-shaped gates used in prior multi-channel HEMTs, thus relaxing the lithography requirement. We experimentally demonstrated the multi-kilovolt AlGaN/GaN MC^2-HEMTs on a 5-channel wafer with breakdown voltage from 3.45 kV up to over 10 kV. The 10-kV MC^2-HEMTs show a 1.5-V threshold voltage and a 40-m$\Omega\cdot$cm^2 specific on-resistance, which is ~2.5-fold smaller than that of 10-kV SiC MOSFETs and well below the SiC 1-D unipolar limit. To date, this is the first report of 3-kV+ E-mode GaN devices, and our MC^2-HEMTs show the highest Baliga's figure-of-merits in all 6.5-kV+ transistors. The MC^2-HEMT is also applicable to other materials, e.g., (Al)GaO and Al(Ga)N, as a platform design for multi-channel power transistors.

I. Introduction

Medium-voltage (MV) power electronics are widely used in renewable energy processing, electric grids, and transportation electrification. Today's commercial MV devices (also referred to as 'high-voltage' for 1.7-kV+ devices in many context) are dominated by bipolar Si IGBTs up to 6.5-kV, but they suffer from slow switching speed. Recently, 3.3~10-kV unipolar SiC MOSFETs have enabled performance boost in MV systems, and engineering samples are available from a few vendors [1].

GaN has superior physical properties as compared to Si and SiC. Lateral GaN HEMTs have been commercialized up to 900-V class; industrial vertical GaN FETs are available at 1.2 kV [2]. These devices have a breakdown voltage (BV) up to ~2 kV for a large overvoltage margin, e.g., 1.4~2.2-kV BV in 650-V rated GaN HEMTs [3], [4]. Whereas there were only a few reports of 3-kV+ GaN FETs [5]-[9]. All of them are depletion-mode (D-mode) HEMTs with a specific on-resistance (R_{ON}) higher than SiC MOSFETs. Panasonic reported the highest BV (10.4 kV) in GaN with a large specific R_{ON} of 186 m$\Omega\cdot$cm^2 [6].

The multi-channel structure can effectively reduce R_{ON} and could be a game changer for lateral high-voltage GaN devices. Recently, 3.3~10-kV multi-channel GaN Schottky rectifiers have been demonstrated with specific R_{ON} below the SiC 1-D unipolar limit [10-12]. Whereas it is very challenging to design multi-channel HEMTs, as their planar gate is in deep D-mode. Nanometer-sized fin-shaped gates were used in multi-channel RF and power HEMTs [13], [14] to shift the threshold voltage (V_{TH}) towards zero, e.g., 1300-V E-mode devices enabled by 15-nm gated fins [14]. However, such a demanding lithography is rarely used in power device manufacturing (180-nm+ nodes dominantly in industry). These nm-sized gates may also make the electric field management and voltage upscaling difficult.

This work proposes a new design to realize the E-mode in high-voltage (HV) multi-channel HEMTs by combining a low-voltage (LV) E-mode HEMT and a HV planar multi-channel HEMT in the Cascode connection. The LV HEMT is integrated monolithically by using one channel in the multi-channel wafer. This design enables the first demonstration of multi-kilovolt E-mode GaN HEMTs up to >10-kV. A low specific R_{ON} of 40-m$\Omega\cdot$cm^2 is demonstrated in 10-kV device, setting a new record in Baliga's figure-of-merit (FOM=BV^2/R_{ON}) for MV transistors.

II. Device Design and Simulation

Fig. 1 shows the schematics, equivalent circuit, and key geometries of our Multi-Channel Monolithic-Cascode HEMT (MC^2-HEMT). In a 5-channel AlGaN/GaN wafer, the 5th 2DEG channel is used for making the LV E-mode HEMT with gate recess. A plurality of Ohmic vias function as the effective drain for the single-channel LV-HEMT and the source for the multi-channel HV-HEMT. The HV-HEMT gate is connected to the LV-HEMT source, forming a Cascode. In the HV-HEMT, a p-GaN cap layer balances the net donors in the multi-channel and thus functions as a reduced surface field (RESUFR) structure, similar to that described in [12]. The BV of the LV-HEMT (~200 V) is designed to be higher than the magnitude of the multi-channel-HEMT's V_{TH} ($V_{TH}^{MC} \approx$ -100 V). The smallest geometric feature is 2-µm. *This MC^2-HEMT is different from commercial Cascode GaN HEMTs, in which the LV device is a Si MOSFET in a separate chip, or the all-GaN Cascode reported in [15], in which the HV-HEMT is on a single channel.*

3-D TCAD simulations in Silvaco Atlas were used to verify the device working principles. At gate bias $V_{GS} > V_{TH}$, Ohmic vias allow current flows from the single channel into 5 channels (Fig. 2(a)). In the OFF state ($V_{GS} < V_{TH}$), when the drain voltage $V_{DS} < |V_{TH}^{MC}|$, the LV-HEMT is depleted (Fig. 2(b)-(c)); when $V_{DS} > |V_{TH}^{MC}|$, the HV HEMT starts to be depleted and the voltage drop across the LV-HEMT is clamped at ~$|V_{TH}^{MC}|$. Hence, the device gate is shielded from high V_{DS} and E-field (Fig. 2(d)-(f)). The RESURF in HV-HEMT spreads the E-field, allowing a BV scaling with the multi-channel gate-drain distance (L_{GD}^{MC}).

III. Device Fabrication

The wafer consists of 20-nm p^+-GaN, 350-nm p-GaN ([Mg] ~ 4×10^{18} cm^{-3}), five $Al_{0.25}Ga_{0.75}N$ (23 nm)/GaN (100 nm) hetero channels, and a buffer layer, all continuously grown on a 4-inch sapphire substrate by MOCVD. Hall measurements reveal a 178-Ω/sq sheet resistance (R_{SH}), 2010-cm^2/V·s 2DEG mobility, and 1.75×10^{13}-cm^{-2} total 2DEG density for the multi-channel.

Fig. 3 shows the main fabrication steps. Patterned dry etches were first performed for p-GaN and four AlGaN/GaN channels using Cl_2/BCl_3 gases. A $Cl_2/Ar/O_2$ etch followed, which has a ~20 selectivity for GaN over AlGaN and allows etch-stop at the 5th channel. The R_{SH} of the exposed 5th channel was measured to be 567 Ω/sq. Three types of LV-HEMTs were fabricated: the D-mode MOS-HEMT and Schottky-gate HEMT (Sch-HEMT), and E-mode MOS-HEMT. The E-mode device was made by an a BCl_3 etch for 18~19-nm AlGaN under gate. A high-k HfO_2 was deposited as the gate dielectric by atomic layer deposition.

Ohmic contacts were then formed on the 5th channel as the source, in the 5-channel vias, and over p-GaN and 5-channels as the drain. A self-aligned process [10] was used for the latter two processes. The p-GaN RESURF was made by a gradual etch to reach the charge balance condition. A portion of p-GaN close to the drain was completely removed to avoid the p-GaN punch through. Finally, Ni/Au gates were formed on single- and multi-channel HEMTs, followed by PECVD SiN_x passivation.

Fig. 4 shows the top-view and cross-sectional scanning electron microscopy (SEM) images of the fabricated device, showing the accurate etch controls in the single- to five-channel transition region, RESURF, and 5-channel p-gate region. Fig. 5 shows the RESURF p-GaN thinning process witnessed by C-V measurements of a test structure. When the acceptors in p-GaN balance total donors in the multi-channel, a capacitance drop is shown. The critical p-GaN thickness was identified as ~80 nm.

IV. Device Characteristics

Fig. 6 shows the transfer characteristics of the MC²-HEMTs with and without gate recess in the LV-HEMT, revealing a D-mode to E-mode transition. 10 devices at different locations were measured for each type, showing a small V_{TH} variability.

Fig. 7 and 8 show the transfer and output characteristics of the D-mode and E-mode 10-kV MC²-HEMTs with L_{GD}^{MC} = 103 µm, respectively, one with a Sch-HEMT and the other with a recess MOS-HEMT as the LV-HEMT. The two types of MC²-HEMTs show V_{TH} of -3.5 V and +1.5 V extracted at 1 mA/mm. Only a very small hysteresis was observed. The D- and E-mode 10-kV MC²-HEMTs show over 300-mA/mm I_D, and their R_{ON} is almost identical, suggesting a small gated-channel resistance in the LV recess MOS-HEMT using the high-k gate dielectric.

Fig. 9 shows OFF-state I-V curves of E-mode MC²-HEMTs with L_{GD}^{MC}= 28, 53, 78, 103-µm measured at zero V_G, revealing a ~µA/mm drain leakage current and BV of 3.453-, 6.576-, 8.864- and >10-kV, respectively. The p-GaN RESURF design enables an average lateral E-field (E_{AVE}=BV/L_{GD}^{MC}) of 1.24 MV/cm. The 103-µm-L_{GD}^{MC} device was repeatedly measured to 10 kV (our test limit) without breakdown, and its BV was estimated to be 10.7 kV based on E_{AVE}. The gate does not break at BV (I_G does not increase), verifying the low E-field at the device gate.

The analysis of R_{ON} component is key to understanding the design space of GaN MC²-HEMTs. The specific R_{ON} of E-mode 3.45-, 6.57-, 8.86- and 10-kV MC²-HEMTs were calculated as 9.35-, 17.5-, 27.6-, and 40-mΩ·cm^2, respectively, with a 3-µm contact finger length accounted in the calculation. As shown in Fig. 10, the R_{ON} of the LV HEMT is ~7 Ω·mm, accounting for 40% and 22% of the total R_{ON} in 3.45- and 10-kV MC²-HEMTs, respectively. Note that our LV-HEMT design has large margins (see Fig. 1(d)), suggesting a good room for further reducing the R_{ON} of GaN MC²-HEMTs, particular for lower voltage ratings.

Fig. 11 shows the C_D-V_{DS} characteristics measured at zero V_{GS} up to V_{DS} = 3 kV. The output capacitance C_D shows the successive depletion of multiple 2DEG channels, suggesting that it is dominated by the RESURF multi-channel HV-HEMT.

V. Benchmark and Summary

Fig. 12 benchmarks the specific R_{on} *vs.* BV of our 3.45~10-kV E-mode GaN MC²-HEMTs and the reported GaN, SiC and ultra-wide-bandgap (UWBG) AlGaN FETs with similar BV [1], [6]-[9], [16]. Table I compares the R_{on}, BV, V_{TH}, E_{AVE}, and FOM of state-of-the-art GaN, SiC, UWBG Ga_2O_3 [17] and AlGaN HV FETs. Our MC²-HEMT is the only WBG/UWBG E-mode power FET in the 3~10-kV range in addition to SiC MOSFETs. The R_{on} *vs.* BV performance of our 6.5-kV+ GaN MC²-HEMT exceeds the SiC 1-D unipolar limit, rendering a record Baliga's FOM of 2.84 GW/cm^2. Our 10-kV GaN MC²-HEMT has a 2.5-fold lower specific R_{ON} as compared to10-kV SiC MOSFETs.

In summary, we present a new device concept, the RESURF MC²-HEMT, which can concurrently exploit the low R_{SH} of multi-channel materials, realize the robust E-mode gate control without the need for sub-micron lithography, and shield the gate region from high E-field. We experimentally demonstrated E-mode 3.4~10-kV GaN RESURF MC²-HEMTs, and their FOMs set a new record in all 6.5-kV+ power transistors. Our results show the great potential of GaN MC²-HEMTs for MV power electronics. In addition, the MC²-HEMT concept is applicable to other WBG/UWBG materials, e.g., (Al)GaN and Al(Ga)N, as a platform design for multi-channel HV power devices.

Acknowledgement

We acknowledge the support from a US-UK NSF-EPSRC project (Grants ECCS-2036740, ECCS-2036915, and EP/W007614/1) and CPES Power Management Consortium.

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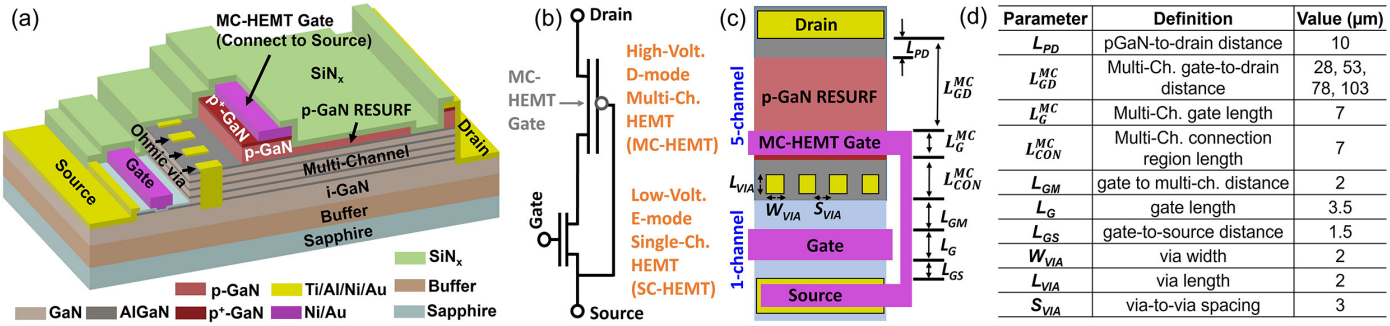

Parameter	Definition	Value (μm)
L_{PD}	pGaN-to-drain distance	10
L_{GD}^{MC}	Multi-Ch. gate-to-drain distance	28, 53, 78, 103
L_{G}^{MC}	Multi-Ch. gate length	7
L_{CON}^{MC}	Multi-Ch. connection region length	7
L_{GM}	gate to multi-ch. distance	2
L_G	gate length	3.5
L_{GS}	gate-to-source distance	1.5
W_{VIA}	via width	2
L_{VIA}	via length	2
S_{VIA}	via-to-via spacing	3

Fig. 1. (a) 3-D schematic of the AlGaN/GaN MC^2-HEMT fabricated in this work. The SiN_x passivation layer is partially removed to show the internal structure. (b) equivalent circuit model and (c) top-view schematic of the MC^2-HEMT, showing the Cascode configuration in which the gate of the multi-channel HEMT (MC-HEMT) is connected to the source. (d) the list of key geometric parameters (marked in (c)) and their values. The smallest feature is 2-μm; no sub-μm lithography is needed.

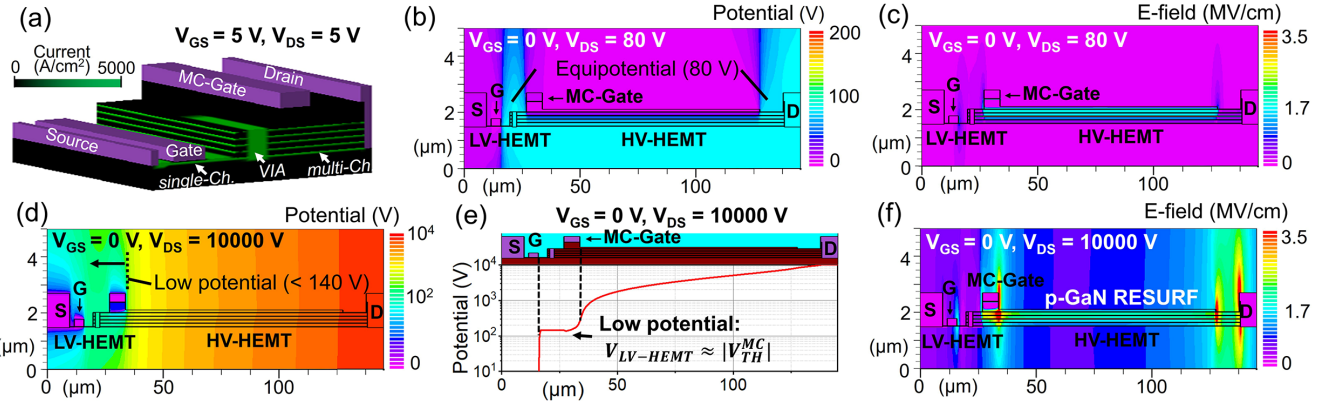

Fig. 2. (a) Simulated current density contours in a MC^2-HEMT unit-cell in the device ON-state, showing that the Ohmic via allows the current to flow from the LV-HEMT's single-channel into the HV-HEMT's multi-channel. Simulated cross-sectional (b) potential and (c) E-field contours when a 10-kV MC^2-HEMT is blocking 80-V, showing the V_{DS} drop almost entirely in the LV-HEMT. Simulated (d) potential contours, (e) potential distribution along a cutline in the 5th 2DEG channel, and (f) E-field contours when the MC^2-HEMT is blocking 10-kV, showing the voltage drop in the LV-HEMT clamped at ~140 V. The E-field distribution is well balanced with the peak E-fields located in the RESRUF and drain side. The E-field in the gate region is very small. The gate is completely shielded from high V_{DS} and E-field.

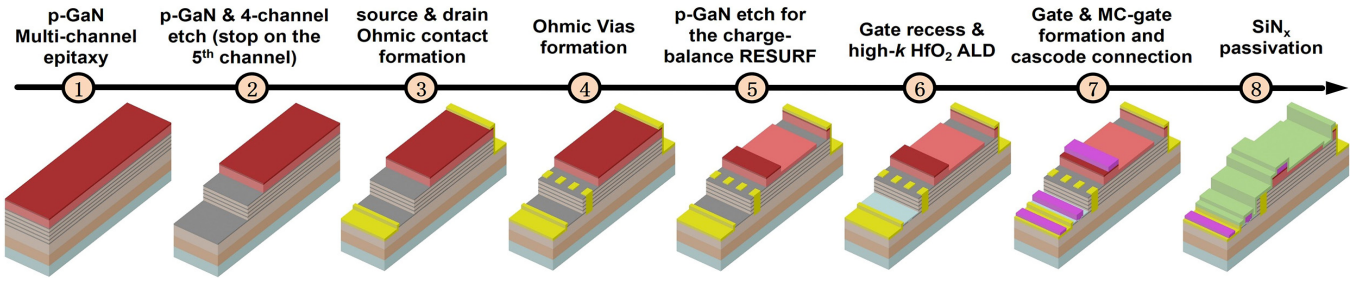

Fig. 3. Schematic illustration of the main steps in device fabrication. The self-aligned Ohmic process to form the vias and drain contact is similar to that in [10].

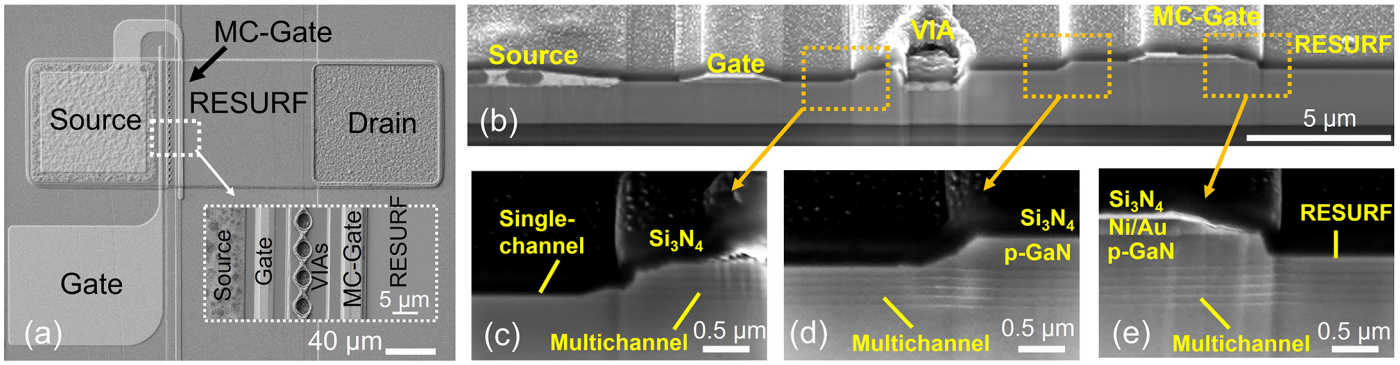

Fig. 4. (a) Top-view SEM image of the fabricated GaN RESURF MC^2-HEMT and the enlarged image of the source-to-multi-channel-HEMT region. (b) Cross-sectional SEM image of the single-channel LV-HEMT, Ohmic via, multi-channel-gate and RESURF regions in the MC^2-HEMT, with the enlarged images shown in (c)-(e).

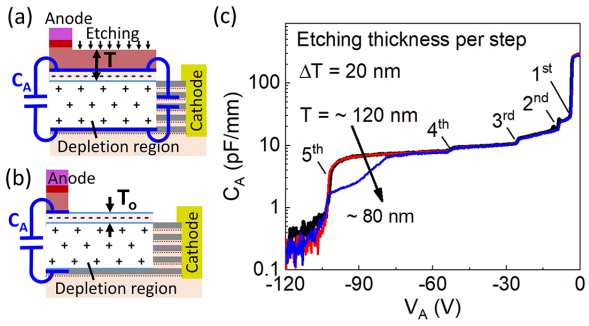

Fig. 5. Illustrations of charges and capacitances (a) before and (b) after reaching the critical p-GaN thickness (T_O) for charge balance condition, suggesting a drop in C-V characteristics at the critical condition. (c) Experimental C-V curves of the test structure with a step thinning in p-GaN, revealing $T_O \approx$ 80-nm.

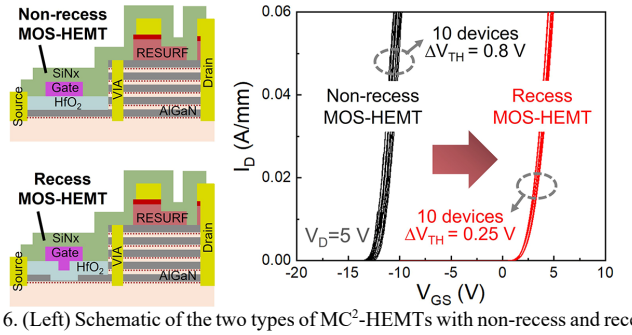

Fig. 6. (Left) Schematic of the two types of MC²-HEMTs with non-recess and recess MOS-HEMTs as the LV-HEMT. (Right) Transfer characteristics of 10 devices of each type of the MC²-HEMT, showing a positive V_{TH} shift enabled by the gate recess and relatively small V_{TH} variability in the E-mode MC²-HEMT.

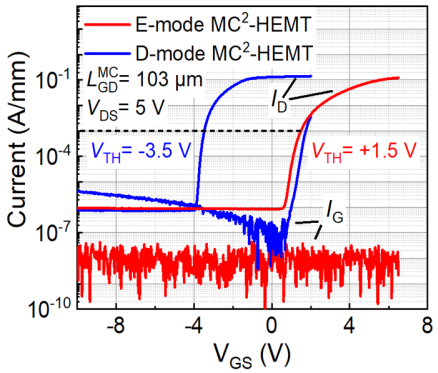

Fig. 7. Transfer characteristics of E-mode and D-mode MC²-HEMT with L_{GD}^{MC} of 103-μm. The D-mode device has a Shocttky gate and the E-mode device has a MOS gate. V_{TH} = 1.5 V in the E-mode device.

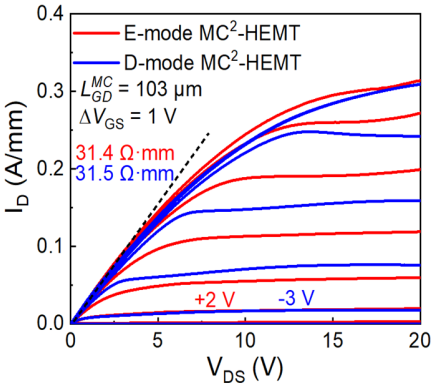

Fig. 8. Output characteristics of E-mode and D-mode MC²-HEMT with L_{GD}^{MC} of 103-μm. The E-mode device shows a very slightly lower R_{ON} as compared to the D-mode device. I_D exceeds 300 mA/mm.

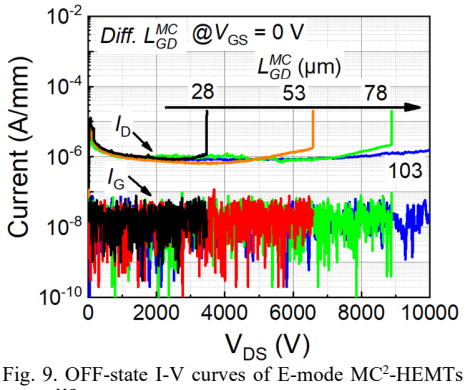

Fig. 9. OFF-state I-V curves of E-mode MC²-HEMTs with L_{GD}^{MC} of 28-, 53-, 78- and 103-μm, showing BV of 3.45-, 6.58-, 8.86- and >10-kV. The 103-μm device was tested to 10-kV (our setup limit) without breakdown. I_G does not increase at breakdown (gate does not break).

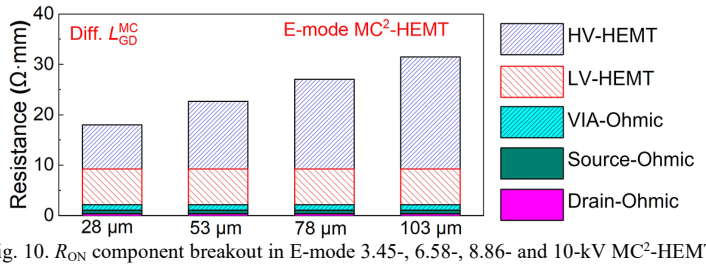

Fig. 10. R_{ON} component breakout in E-mode 3.45-, 6.58-, 8.86- and 10-kV MC²-HEMTs. The LV-HEMT portion accounts for the source to via, and the HV-HEMT accounts for the via to drain. The other three portions are the contact resistances of source, drain, and VIAs.

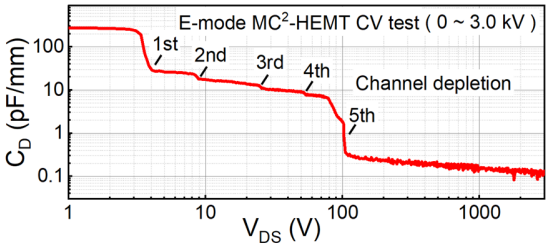

Fig. 11. C_D-V_{DS} characteristics of the E-mode MC²-HEMT up to 3-kV, showing the successive depletion of multiple channels. This suggests that the output capacitance of MC²-HEMT is dominated by the HV-HEMT.

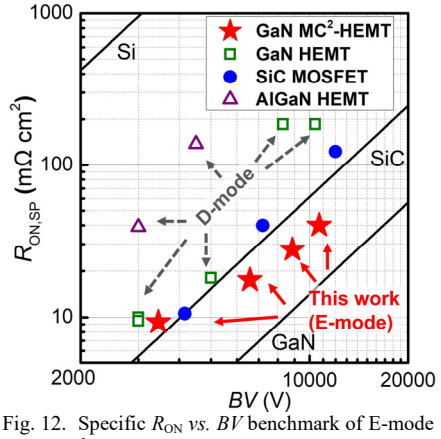

Fig. 12. Specific R_{ON} *vs.* BV benchmark of E-mode GaN MC²-HEMT and the state-of-the-art 3~10-kV GaN HEMTs, SiC MOSFETs, and AlGaN HEMTs.

TABLE I. Comparison of the state-of-the-art 3~10-kV wide-bandgap and ultra-wide-bandgap transistors.

Device	Key Design	Maker	BV (kV)	$R_{ON,SP}$* (mΩ·cm²)	BV / L_{GD} (MV/cm)	D/E-mode	V_{TH} (V)	FOM** (GW/cm²)
GaN HC²-HEMT	**Multi-Channel; Cascode; RESURF**	**VT (this work)**	**3.45~ >10**	**9.35~40**	**1.13~1.24**	**E-&D-mode**	1.5 & -3.5	2.84
GaN HEMT	through sapphire via	Panasonic [6]	10.4	186	0.83	D-mode	-4.5	0.58
	native GaN substrate	Fukui U [7]	5.0	18	1.0	D-mode	-3	1.38
	natural superjunction	Powdec [8]	3.0	9.5	0.75	D-mode	-4.5	0.95
	substrate removal	IEMN [9]	3.0	10	0.75	D-mode	-4.5	0.90
SiC MOSFET	pre-commercial vertical device	Wolfspeed [1]	4.16 ~12	10.6-123	N/A	E-mode	~2.2	1.17
Ga_2O_3 MOSFET	composite field plate	Buffalo U [17]	6.72~ 8.03	6240~ 18000	1.15~1.69	D-mode	-10	0.0072
AlGaN HEMT	AlN/AlGaN/AlN Ch.	IEMN [16]	4.5	~138***	1.13	D-mode	-25	0.15

*For lateral FETs with R_{ON} reported in Ω·mm, a 3-μm contact length was added to L_{SD} in $R_{ON,SP}$ calculation.
**$BV^2/R_{ON,SP}$. ***estimated from the reported I-V of 5-μm-L_{GD} devices and the R_{SH} (L_{GD}=40-μm for 4.5-kV).