Van der Waals Vertical Transistors with Run-time Reconfigurability

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Scaling down the size of transistors is one of the main driving forces for the development of semiconductor technologies. Vertical transistors with the channel perpendicular to the substrate allow for the overlap of source and drain contacts, which can effectively reduce the footprint of a transistor. In addition, the channel length of a vertical transistor is determined by the semiconductor thickness, which can be easily scaled down to below 5 nm without high-cost ultraviolet or e-beam lithography. Van der Waals materials can be thinned down to an atomic scale without any surface roughness and can be transferred on any substrate with controlled locations, making them promising candidates for vertical transistors. Several designs of vdW vertical transistors are reported recently, such as the resonant tunneling transistor and barrister [1-2]. Furthermore, the polarity of 2D transistors based on semiconductors with small to medium bandgaps can be tuned n-type or p-type by modulating the doping levels. Several reconfiguration schemes have been proposed to enable dynamic control of the polarity of transistors, including electrostatic doping from additional control gates and proximity doping from ferroelectric materials [3-4]. In this abstract, we report a compact vertical transistor with layered semiconductor $MoTe_2$ as channel. Without adding any additional control gate and ferroelectric materials, the transistor exhibits reconfigurable polarity (n-type or p-type) depending on the current flow direction.

The schematic of a $MoTe_2$ vertical transistor is shown in Fig. 1(a). The device was fabricated on a p-type Si substrate with 90 nm SiO_2. The $MoTe_2$ flake was transferred on the gold contact and another top gold contact is subsequently transferred on the $MoTe_2$ flake. The size of the overlap region is 3.62 μm by 3.81 μm. The optical image and the AFM topography of the $MoTe_2$ vertical transistor are shown in Fig. 1(b) and 1(c) respectively. The thickness of the $MoTe_2$ flake is 12 nm. The band diagrams of the $MoTe_2$ vertical transistor under the positive and negative gate voltages are shown in Fig. 1(d). The $MoTe_2$ under the top contact can be electrostatically doped by a back gate voltage. However, the doping in the $MoTe_2$ near the bottom contact is unaffected by the back gate due to the screening of the bottom electrode. Fig. 2 shows the transfer curves for a 22 nm thick $MoTe_2$ channel under different drain voltages. The bottom electrode is used as the drain contact. The drain current in the electron branch is much higher than that in the hole branch since the positive drain voltage facilitates the electron injection from the top electrode and n-type doping in $MoTe_2$ near the source contact can effectively reduce the Schottky barrier height for electrons at the source contact. As the drain voltage increases, an increased minimum conduction current was observed. An on/off ratio of 440 was achieved at $V_D = 0.5$ V. Fig. 3 shows the temperature dependence of the vertical drain current of the device. The drain current increases significantly as the temperature increases, indicating that thermo-ionic emission and thermal-assisted tunneling play important roles in the vertical transistor with Schottky contacts. An effective barrier height of 0.285 eV is extracted for the $MoTe_2$/Au contact under $V_{top} = 0.4$ V. Fig. 4 shows the transfer curves measured from the back gate under two different configurations: (i) bottom and (ii) top electrodes serving as the drain. Here the drain voltage is positive. In these two configurations (i.e. different current flow directions), the transfer curves show opposite polarities. The energy diagrams along the channel for these two scenarios are shown in Fig. 1(d). When the bottom electrode serves as the drain, the positive drain voltage will attract electrons to inject from the top electrode. Under a large positive gate voltage, the $MoTe_2$ under the top contact is electrostatically n-doped, which substantially decreases the tunneling barrier width for electrons. Therefore, a high electron current is observed. On the other hand, the injection from the bottom contact is limited by the original barrier without electrostatic doping, and

the electron current is low when the bottom contact is used as the drain contact. The output curves measured at a strong gate doping condition shown in Fig. 5 further confirms the different conduction with and without electrostatic doping. The two higher branches correspond to carrier injection from the top contact, and the two lower branches correspond to carrier injection from the bottom contact.

In summary, we investigated vertical transistors with thin $MoTe_2$ channels. The top and bottom contacts are asymmetrically doped under the electrostatic bias from the back gate. Reconfigurable polarity is observed in the vertical transistor under different current directions. Our results demonstrate short channel vertical transistors based on 2D semiconductor $MoTe_2$ and provide a simple way to achieve run-time reconfiguration without additional control gates, which will be helpful to the design of highly-scaled and high-efficient integrated circuits.

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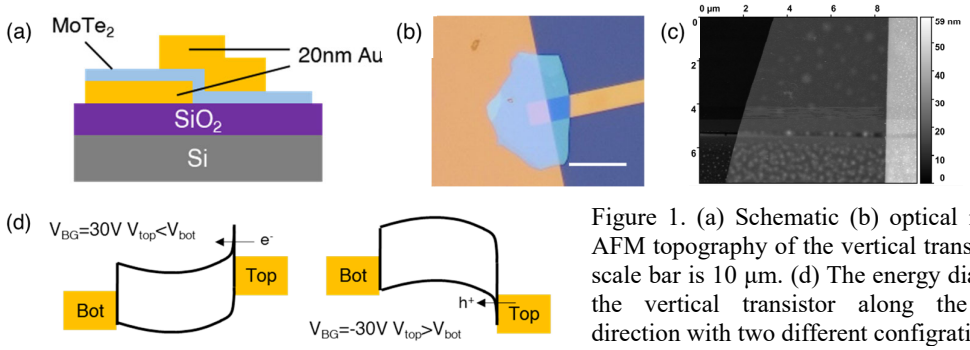

Figure 1. (a) Schematic (b) optical image (c) AFM topography of the vertical transistor. The scale bar is 10 μm. (d) The energy diagrams of the vertical transistor along the channel direction with two different configrations.

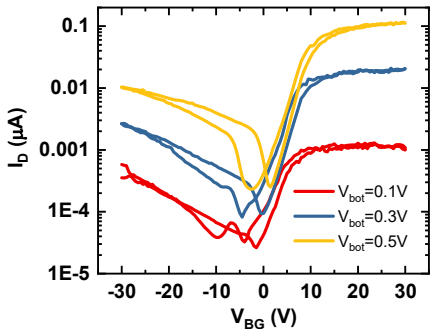

Figure 2. Transfer curves of the $MoTe_2$ vertical transistor measured at different drain voltages.

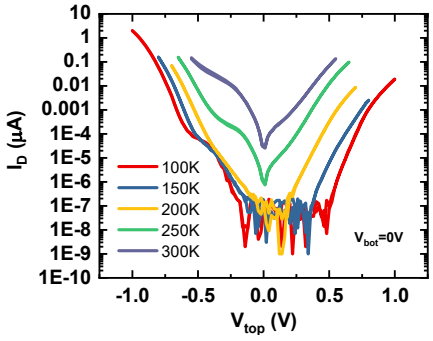

Figure 3. Temperature-dependent vertical conduction measured with floating gate terminal.

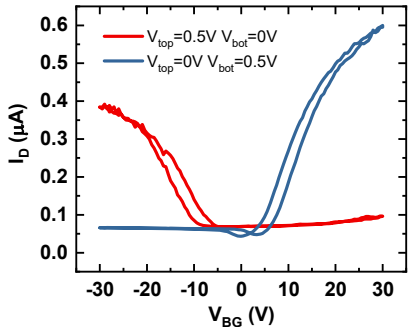

Figure 4. Transfer curves measured when the drain voltage is applied on bottom and top electrodes.

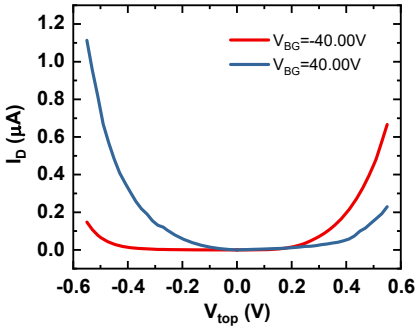

Figure 5. Output curves measured when the back gate voltage is -40 V and 40 V respectively.