Design of a CMOS Parametric Frequency Divider with 2.4-GHz Output Frequency for RF Systems-on-a-Chip

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***Abstract*—This paper presents a CMOS 2:1 differential parametric frequency divider (PFD) design with an output frequency of 2.4 GHz and an input voltage range of 450∼890 mV at 4.8 GHz. The topology is suitable for integration into RF Systems-on-a-Chip (SoCs), and has been constructed for sub-6 GHz applications. A design and optimization methodology for this on-chip PFD is also described in this paper. The simulation results show a performance improvement of the proposed differential PFD compared to a single-ended PFD designed for the same output frequency in the same 65nm CMOS technology.**

***Index Terms*—RF frequency divider, parametric circuits, varactor diode, nonlinear elements.**

I. Introduction

The phenomena of parametric resonance and relevant applications have caught attention of researchers over the past decades [1]. Among the applications of the parametric resonance, parametric amplifiers (paramps) operate and provide gain through a nonlinear process using nonlinear reactors (e.g., varactor diodes), and have been demonstrated with effectiveness such as for improving the noise performance of a low-noise amplifier (LNA) [2]. Apart from the deployment in LNA design, various works on varactor-based parametric circuits have also been reported by researchers. For example, the use of paramps allows the frequency up-/down-conversions of continuous signals with lower power consumption compared to transistor-based mixers [3], [4]. A CMOS implementation of a parametric frequency doubler at 100 GHz with low conversion loss is reported in [5], which also requires relatively low input power even without high performance devices. Meanwhile, parametric circuits start to play a role in wireless voltage sensing as well: a triple-frequency parametric oscillator was designed in [6] to wirelessly sense transmitted voltage signals using antenna power, which presents decent sensitivity and linearity with a more compact design.

Among the diverse applications based on the parametric phenomenon, parametric frequency dividers (PFDs) are becoming increasingly attractive in recent research efforts. In particular, the great potential of PFDs for Internet of Things (IoT) applications [7] and the need to design low-power wireless systems-on-a-chip (SoC) have encouraged new explorations in academia. For instance, the first on-chip PFD using a reflective distributed resonator was introduced in [8], which does not dissipate static power and is considered feasible to replace power-hungry digital dividers in the high-frequency domain (>20 GHz). To date, the design of integrated CMOS PFDs at sub-6 GHz frequencies with on-chip passive components has not been addressed yet. Considering the abundant wireless standards around 2.4 GHz, an on-chip differential PFD with sub-6 GHz output is presented in this paper, which is CMOS-compatible and designed for further integration into low-power RF SoCs in future works. In addition, this paper provides design insights through descriptions of circuit-level considerations and the employed optimization methodology.

This paper is organized as follows: Section II discusses fundamental PFD design aspects and exiting works on the printed circuit board (PCB) and chip levels. The proposed CMOS PFD topology designed in a 65 nm process is introduced in Section III, together with the corresponding design and optimization strategies. Simulation results of this differential PFD with an output buffer stage are presented in Section IV. Section V provides the conclusion.

II. Background

Frequency dividers are useful blocks in low-power RF SoCs where an on-chip phase-locked loop (PLL) is either required [9] or not [10]–[12], especially in architectures in which a local oscillator (LO) signal is generated with twice the frequency required by the mixer. Despite the fact that digital dividers can operate at frequencies up to several gigahertz, parametric frequency dividers (PFDs) still stand out because of their passivity [13] that is becoming more and more critical in scenarios such as IoT sensors [7], RF frequency-selective limiters with low power threshold ($\mathrm{P_{th}}$) [14] and other systems requiring ultra low-power operation.

Alongside the low-power characteristics, PFDs based on varactor diodes have shown high potential for resolving the ongoing RF design challenges related to LO phase noise reduction. A micro-electromechanical system (MEMS)-based PFD with extremely high quality factor (Q $\approx$ 81,000) was reported in [15], which demonstrated a 6 dB and 23 dB of phase noise improvement at frequencies close-to and far-from the carrier, respectively. However, the MEMS implementation demands a customized fabrication process to achieve such high Q values, for which a solution with an on-chip phase noise reduction system for CMOS technologies is more desirable. On the other hand, phase noise reduction through parametric filtering (PFIL) was introduced recently [16], [17], where the resonator dynamics of the closed-loop system is slowed down when the frequency division is triggered, such that the system is not fast enough to follow the phase fluctuations of the RF input signal,

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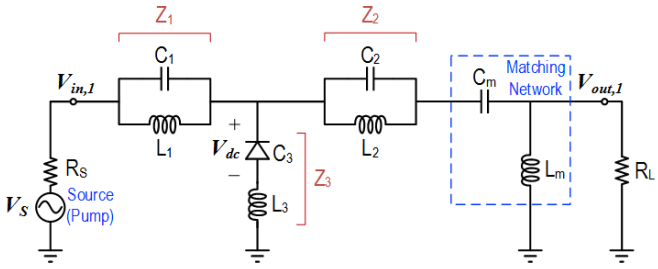

Fig. 1. Single-ended PFD with output matching network.

and thereby the phase noise of the oscillator can be reduced significantly [17]. The fundamentals of parametric frequency division via a varactor-based topology rely on the system operation close to the Hopf bifurcation region [18]. When the nonlinear reactive element (here, varactor capacitance) of the system is modulated by an RF input signal with voltage level larger than the parametric voltage threshold (V_{th}), the system inherently triggers a 2:1 frequency division through the bifurcation phenomenon. In other words, the output frequency (f_{out}) and the input frequency (f_{in} or f_{pump}) are governed by (f_{out} = $f_{in}/2$) when the parametric frequency division is triggered. The analysis of PFD operations has been thoroughly studied and derived in [13] and [19].

Despite of a number of discussions and explorations on the parametric frequency division mechanism, most of the reported works hitherto were implemented either through customized MEMS processes [15] or on PCBs [7], [13], [16], [17], [19]–[21], which can make on-chip integration quite challenging due to area limitations and low Q values of chip-level inductors and capacitors. The first on-chip PFD was developed in [8], where parallel nonlinear transmission lines and MOS varactors were utilized to realize a 20:10 GHz frequency division with zero static power consumption. However, when the operating frequency is brought down to the sub-6 GHz range, on-chip transmission lines become challenging to implement due to the longer wavelengths and large layout area requirements. To adapt to lower frequencies (e.g., 4.8:2.4 GHz division), the architecture introduced in this paper avoids the use of transmission lines. Our introduced architecture is based on a differential PFD topology constructed with regular foundry-provided devices models, including the inductor-capacitor (LC) combinations with values that are suitable for on-chip integration. To the best of the authors' knowledge, this is the first CMOS PFD with a relatively low frequency output around 2.4 GHz.

The classic single-ended varactor-based PFD topology [13], [19]–[21] is displayed as in Fig. 1. The T-shape PFD core consists of three impedance blocks: $Z_1(L_1//C_1)$, Z_2 $(L_2//C_2)$ and Z_3 $(L_3 + C_3)$ and a DC reverse-biasing voltage (V_{dc}) is applied to the varactor (C_3). The matching network at the PFD output (L_m and C_m) is tuned to match the output impedance to the load (e.g., 50 Ω). Based on a recently reported system synthesis approach and optimal design criteria [20], four resonance conditions should be satisfied to assure frequency division with decent V_{th}:

1) Z_1 is in parallel-resonance at $f_{out} = 2.4$ GHz,
2) Z_2 is in parallel-resonance at $f_{in} = 4.8$ GHz,
3) Z_1 and Z_3 are in series-resonance at $f_{in} = 4.8$ GHz,
4) Z_2 and Z_3 are in series-resonance at $f_{out} = 2.4$ GHz.

The varactor for the capacitance modulation (C_3) is realized with an N-type diode in this work, using the standard foundry-supplied device model in a commercial 65 nm CMOS process design kit. The details of the proposed PFD implementation and design strategy are described in Section III.

III. On-chip PFD Design, Implementation and Optimization Methodology

A critical PFD specification is V_{th}, which indicates the minimum input voltage that is required to trigger the 2:1 frequency division and to provide the distinctive output voltage waveform at the desired frequency. From the closed-form expression of V_{th} discussed in [20], V_{th} is proportional to the square of the varactor capacitance (C_3^2) at a certain DC bias (V_{dc}) divided by C_d as in equation (1), where C_d is the first-order coefficient (in Farad/Volts) of C_3 at the given V_{dc}.

$$V_{th} \propto -\frac{(C_3)^2}{C_d} \tag{1}$$

In order to obtain the lowest possible V_{th}, we start our PFD design approach with the strategic selection of the nonlinear component (i.e., N-type diode C_3 as in Fig. 1) such that the proportionality coefficient in equation (1) is as small as possible. Fig. 2 presents the characterization of the selected N-type diode (C_3) from the available 65nm CMOS process design kit at 2.4 GHz over a biasing (V_{dc}) range of -100 to $+200$ mV. The capacitance versus voltage curve is displayed in Fig. 2(a), whereas Fig. 2(b) shows the above-mentioned V_{th}−proportionality coefficient: $-C_3^2/C_d$. It can be observed that the optimal reverse DC biasing voltage occurs at $V_{dc} = 0$ V, where the varactor capacitance is $C_3 = 128$ fF. The dimensions of the selected N-diode are 30 µm × 30 µm in consideration of the resonance requirement for Z_3 (C_3 and L_3) as well as the area budget, since the on-chip inductors optimized for their Q-values [8] inevitably occupy a significant layout area.

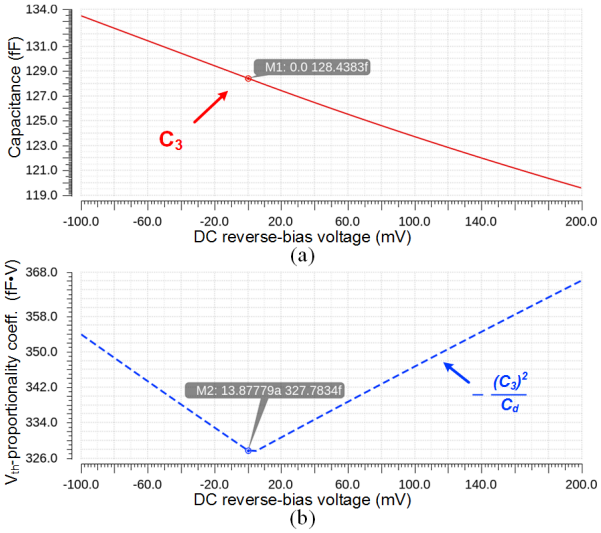

Fig. 2. Simulation-based characterization of the selected foundry-supplied varactor diode model from a 65nm CMOS process: (a) capacitance C_3 versus reverse-bias voltage, (b) V_{th}-proportionality coefficient ($-C_3^2/C_d$ vs. V_{dc}).

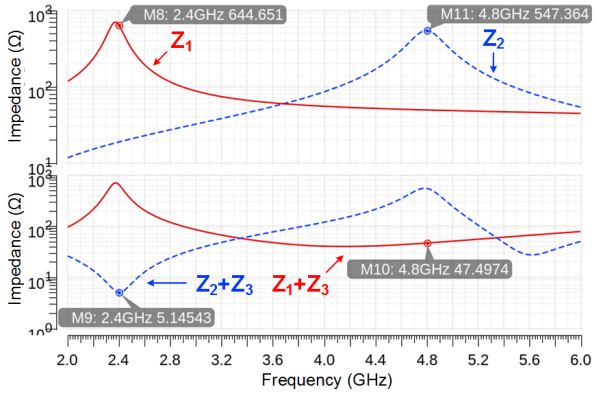

Fig. 3. Simulated impedances for PFD design optimization insights.

TABLE I
COMPONENT PARAMETERS OF THE SINGLE-ENDED PFD (FIG. 1)

Inductor	Values	Capacitor	Values
L_1	2.65 nH	C_1	1.82 pF
L_2	0.954 nH	C_2	1.12 pF
L_3	2.59 nH	C_3^*	0.128 pF
L_m	0.469 nH	C_m	9.47 pF

C_3^*: capacitance of the N-type diode with zero bias at 2.4 GHz.

As mentioned in Section II, four resonance conditions have to be satisfied while designing for low V_{th}. Therefore, the impedances Z_1, Z_2, $Z_1 + Z_3$ and $Z_2 + Z_3$ have been evaluated through simulations over $2 \sim 6$ GHz (Fig. 3). Considering the limited Q-factors (up to 18 in the sub-6 GHz range) resulting from the parasitic resistance of the on-chip inductors, the local optimization tool in Cadence was utilized to tune the dimensions of $L_1 \sim L_3$ (e.g., width, radius, spacing etc.) such that the parallel/series resonance conditions can be reached while the overall layout area is manageable. The optimized L and C values are included in Table I.

Based on the optimized LC values for the single-ended PFD, we propose a fully-differential topology for improved on-chip integration (Fig. 4). Since the proposed PFD is designed for use in RF SoCs, the next stage after the PFD in the system is very likely to provide high impedance (e.g., MOSFET transistor gate) instead of the typical low 50-Ω termination on the PCB. Therefore, the typical output matching network shown in Fig. 1 can be eliminated and the differential PFD outputs (PFDout±) are now extracted right from the joint connections of Z_1, Z_2 and Z_3 in Fig. 4. Since zero DC biasing ($V_{dc} = 0$) is desired (Fig. 2), the ground connections in the single-ended PFD are replaced with an AC coupling capacitor ($C_C = 10$ pF) that generates an AC ground during the operation. Both single-ended and differential PFDs are purely passive and do not consume static power. A simple differential input matching network ($L_{in} = 4.6$ nH, $C_{in} = 1.35$ pF) is included in the PFD to allow direct connections to the off-chip signal sources (or a single-ended source with a balun), which can be further adjusted for on-chip termination as well. The performance improvement achieved by using a differential design strategy (compared to the classic single-ended PFD) is presented and discussed in Section IV.

To enhance the output signal swing and purity at the desired

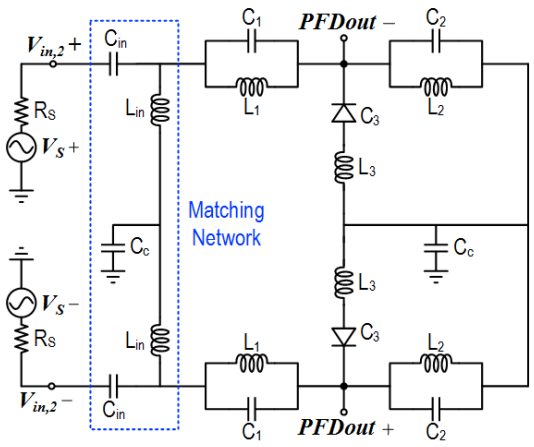

Fig. 4. Proposed differential PFD topology.

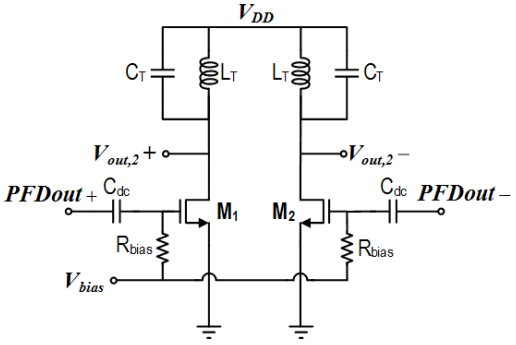

Fig. 5. Class-B switch-mode buffer amplifier stage.

frequency (i.e., $f_{out} = 2.4$ GHz), as well as to provide extra conversion gain, a Class-B switch-mode output buffer (Fig. 5) with a 2.4 GHz LC band-pass filter load was designed to extract the PFD outputs. Note that the load capacitor in the LC tank (C_T) includes the estimated load capacitance due to the next stage in an RF SoC (presumably the parasitic capacitance of one or multiple MOSFETs, which is estimated to be 0.5 pF). If the load capacitance is higher, then the C_T value can be reduced correspondingly. The buffer is supplied by a 0.6 V voltage source, which also provides the gate bias (V_{bias}) for the NMOS transistors. The bias-tee (C_{dc} and R_{bias}) is tuned to minimize the loading impact on the PFD. The component parameters of the designed output buffer are included in Table II.

IV. SIMULATION RESULTS

To evaluate and compare the performance of the proposed differential PFD and the classic single-ended topology, the input voltage of both PFDs was swept over the range of 0.4-1.18 V with transient noise activated using foundry-supplied device models for all active and passive components. Note that the same voltage amplitude is applied to the PFD inputs

TABLE II
COMPONENT PARAMETERS OF THE OUTPUT BUFFER (FIG. 5)

Component	Values	Component	Values
$\mathbf{L_T}$	1.1 nH	$\mathbf{C_{dc}}$	10 pF
$\mathbf{C_T}$	3.5 pF + 0.5 pF*	$\mathbf{M_1(M_2)}$	50 µm/0.5 µm
$\mathbf{R_{bias}}$	10 kΩ	$\mathbf{V_{DD}}$	0.6 V

∗ 0.5 pF is the estimated load capacitance from the next stage.

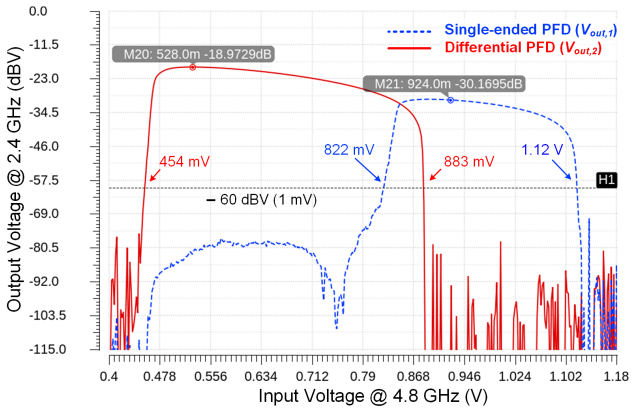

Fig. 6. Output voltage amplitude at f_{out} = 2.4 GHz when sweeping the input voltage at f_{in} = 4.8 GHz. The single-ended topology exhibits a V_{th} of 822 mV, while the differential topology has a V_{th} value of 454 mV.

in Fig. 1 and Fig. 4 (i.e., $V_{in,1} = V_{in,2+} = -V_{in,2-}$), and the input frequency f_{in} is set to 4.8 GHz. Fig. 6 displays the characteristic curves of the output voltage amplitudes ($V_{out,1}$ and $V_{out,2}$) at 2.4 GHz versus input voltage amplitude at 4.8 GHz. Considering the presence of thermal/system noise and signal purity, the -60 dBV (1 mV) level is annotated as the minimum detectable voltage level in Fig. 6, below which the parametric frequency division is "not functional". Hence, it can be observed that V_{th} of the differential PFD is reduced significantly (from 822 mV to 454 mV compared to the single-ended topology). Meanwhile, the operating range is extended from 298 mV to 429 mV, and the maximum output voltage level with parametric division is also increased by ~ 11 dB. Both of these characteristics show the advancement of the proposed PFD for sub-6 GHz on-chip applications.

Fig. 7 presents the output spectra of both PFDs, which was captured at the optimal operating point where the output signal contains the highest power at 2.4 GHz ($V_{in,1} = 924$ mV, $V_{in,2+} = -V_{in,2-} = 528$ mV from Fig. 6). The output voltage component of the classic single-ended PFD at 2.4 GHz is -30.17 dBV, whereas the proposed PFD with an output component of -18.96 dBV at 2.4 GHz shows an improvement of 11.21 dB. Meanwhile, the 2.4 GHz component (f_{out}) at the output of the differential PFD is 7.11 dB higher than the 4.8 GHz component (f_{in}), whereas that of the single-ended PFD remains -2.27 dB below the 4.8 GHz component, which also illustrates the improved spectral characteristics of the

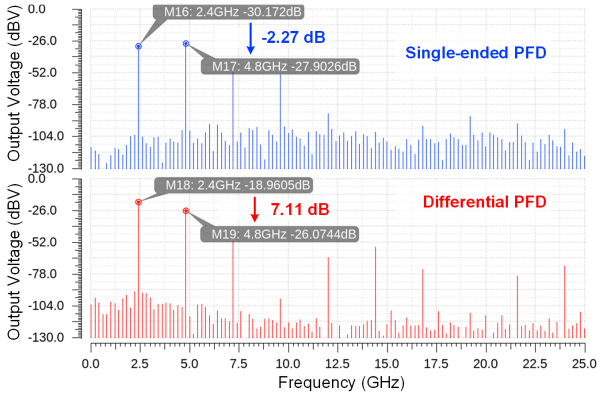

Fig. 7. Simulated output spectra of the proposed differential (bottom) PFD (Fig. 4, Fig. 5) and the classic single-ended (top) PFD (Fig. 1).

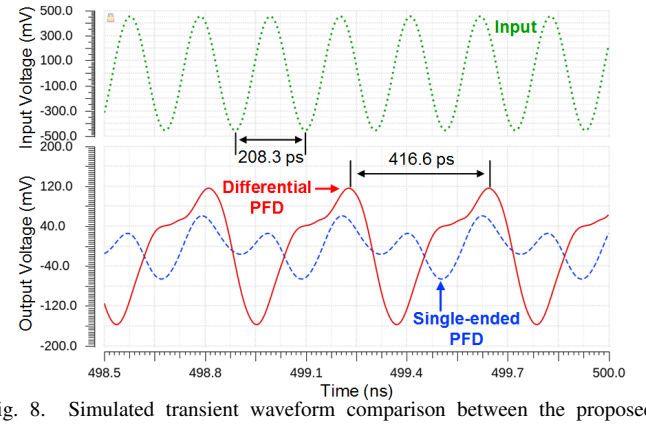

Fig. 8. Simulated transient waveform comparison between the proposed differential PFD (Fig. 4, Fig. 5) and the classic single-ended PFD (Fig. 1).

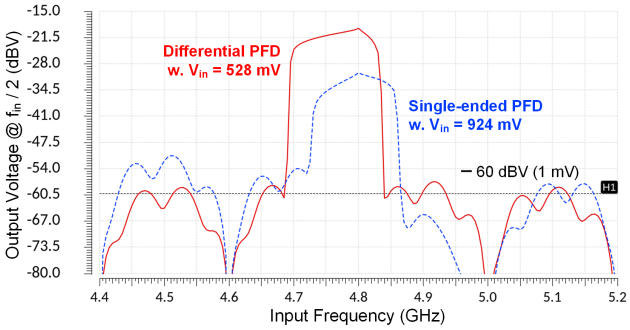

Fig. 9. Frequency responses of the differential and single-ended PFDs.

divided frequency. The corresponding transient waveforms of the PFD input and outputs ($V_{in,+}$, $V_{out,1}$, and $V_{out,2}$) are presented in Fig. 8, where the fundamental periods of the input and output are labeled. The total power consumption of the proposed PFD comes from the output buffer, which is 1.5 mW at the optimal operating point with a supply voltage (V_{DD}) of 0.6 V. On the other hand, the single-ended circuit does not consume any static power. Fig. 9 displays the frequency response of both PFDs at optimal operating points. The differential topology presents a slightly wider operating bandwidth over which the 2:1 frequency division remains functional (i.e., $V_{out1,2}@f_{in}/2$), as well as an overall ~ 10 dB higher output amplitude.

V. Conclusion

A fully-differential 2:1 CMOS parametric frequency divider (PFD) with f_{out} at 2.4 GHz was introduced in this paper. Compared to classic single-ended topology that was previously demonstrated as a PCB implementation, the proposed differential PFD design for on-chip applications significantly reduces the input voltage (V_{th}) level that is required to trigger the frequency division. Furthermore, it has an extended operating range and improved output signal purity over the classic single-ended PFD topology. Design methods and simulation results were discussed to provide insights into the potential of this PFD to be integrated into CMOS SoCs.

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