Application Driven Rapid Synthesis for Analog BIST Components

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***Abstract*—This work proposes rapid synthesis of analog built-in self-test (BIST) circuits using a streamlined design methodology that pulls BIST circuit architecture(s) from a library of components and synthesizes the circuit(s) using a circuit-level design automation (DA) algorithm that combines Multivariate Regression models with Geometric Programming optimization. The presented design methodology is verified through the design of two current-sense BIST circuits for insertion into two different DC-DC converter applications. For each of the two experimental cases, a topology is automatically selected for BIST current sensing, and then the BIST circuit is rapidly sized using the presented DA algorithm.**

***Index Terms*—Built in Self Test, Design Automation, Geometric Programming, Multi Variate Regression, Statistical GP**

I. Introduction

Analog and mixed signal integrated circuits (ICs) consist of numerous individual circuits interacting with one another, many of which are not direct inputs/outputs (I/O) of the IC. Furthermore, these ICs have multiple functions and numerous I/O, thereby motivating the need for built-in self-test (BIST) in ICs to reduce their test complexity and cost, both at post-production test and in the field once the IC has been deployed. BIST enables test/monitoring of I/O as well as internal nodes within the IC without requiring external test probes and equipment. BIST may also be used for in-field monitoring of IC (or individual circuit's) performance for failure prediction and potential system improvement [1], [4], [5].

BIST approaches mostly include fault detection and target and specification oriented testing methodologies, which have been more popularly explored in the digital realm [1]. However, there has been a recent demand in analog BIST methods to monitor critical circuits that may become single points of system failure, including power conversion and voltage reference circuits [5], [6]. BIST methodologies employing machine learning tools have been effectively demonstrated for fault detection/diagnosis in analog and RF circuits, using schemes that employ a non-volatile neural network [2] and statistical analog circuit characterization with a relevance vector and feature machine (RFVM) algorithm [3]. Although machine learning based testing methods have been used and debated [4], use of traditional analog BIST circuits that are inserted within the design under test still remains one of the most popular methods for analog circuit performance and reliability monitoring.

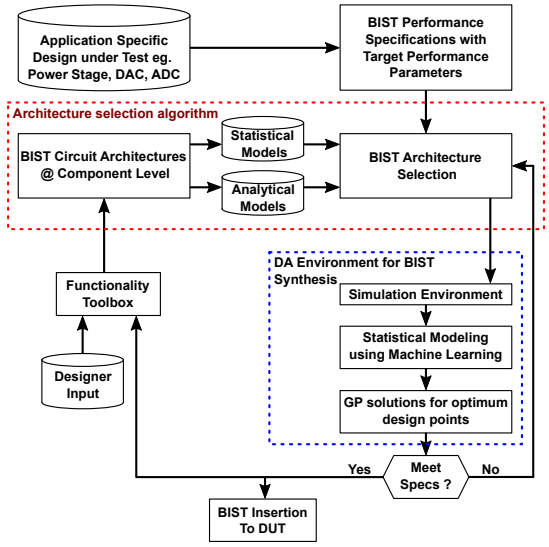

Fig. 1. Overview of synthesis for Analog BIST

The circuits used to enable BIST functionality can be broadly categorized into sense circuits (e.g. current sense, voltage sense, supply sense), signal generation circuits (i.e. test signal generation), and signal conversion circuits such as analog-to-digital (ADC) converters. BIST circuit design requirements depend upon the application, the system requirements, and the circuits which are being sensed, i.e. the design under test (DUT). This means that numerous BIST circuits per system must be generated without much exact design reuse, although architectures from a BIST circuit library can be reused. The excess BIST circuitry typically requires design time from senior designers, whose time often cannot be spared within a rapid hardware design cycle. Automation of these BIST circuits can save manual design time and allow circuit designers to focus on DUT and system level functionality.

This paper proposes the streamlined design flow illustrated in Fig. 1 to quickly and rapidly design analog BIST circuits once the BIST insertion point is determined at a system level. This flow selects the BIST circuit architecture using a collection of data and analytical models derived from DUT circuits, system level design information (e.g. insertion points, system level performance requirements), and BIST circuits. The selection methodology uses knowledge-based methods to select the required BIST circuit architecture. The flow then incorporates a simulation-based design automation (DA) algo-

rithm for circuit synthesis of the selected BIST architecture. The DA algorithm creates Multivariate Statistical Regression (MVR) models using a machine learning tool that relates sizing variables to BIST input and output requirements. The DA then utilizes constraints-based Geometric Programming (GP) to optimize these MVR models and synthesizes the BIST circuit's sizing parameters. If the BIST meets the desired specifications, then the circuit is sent into a functionality toolbox and remembered for later use. If BIST specifications are not met, the algorithm starts at architecture selection.

II. BIST Architecture Selection

BIST automation starts at the system level with DUT specifications, BIST monitoring requirements, and BIST insertion points. These system requirements are fed into the knowledge based decision algorithm to give us the BIST circuit architecture. This knowledge based decision algorithm is created from libraries that comprise of previous examples of DUTs, their BIST insertion points, and types of BIST circuits associated with various monitoring requirements on these DUTs. Some common system level designs that require BIST circuits include PLLs, SERDES, ADCs, and DACs, each having a set of pre-determined BIST circuit topologies. Some of the most widely used BIST sense/monitoring circuits include current sense, voltage sense, power sense in RF systems, frequency sense, and phase sense. Based on the sense requirement of the DUT and the proposed knowledge-based algorithm, a BIST circuit topology is selected.

The BIST is first considered as a part of the entire system, modeled by its inputs and outputs. These models may include input and output impedances to the BIST, as the BIST circuit loads the DUT at its insertion points. Other modeling parameters may include input and output voltages, currents, frequencies, and phase, based on what the BIST is trying to sense and its requirements on sense sensitivity, dynamic range, etc. The library of BIST circuit architectures is then used to select the BIST circuit based on the black box model that is created. This is illustrated in Fig. 2 for a DC-DC converter's power stage as the DUT and the BIST requirement is high-side current sense. The DUT specifications of power stage switching frequency, output load current, and output load voltage, along with the BIST circuit target specifications on input and output impedance at the BIST insertion point, current sense dynamic range, and current sense accuracy are used to model the BIST circuit as a black box. Using these black box models and previous analytical models from the library, the algorithm narrows down the BIST circuit architecture. For example, the DUT illustrated in Fig. 2 requires current sense, and therefore only current sense circuits available in the BIST library would be chosen. The most common examples of these BIST current sense circuits are summarized in Fig. 3. The DUT is used as the judging criteria to decide which of these current sense architectures is the most suitable.

The knowledge-based algorithm uses the DUT performance specifications and BIST functionality (e.g. current monitoring, DUT loop response) to select the BIST architecture. During

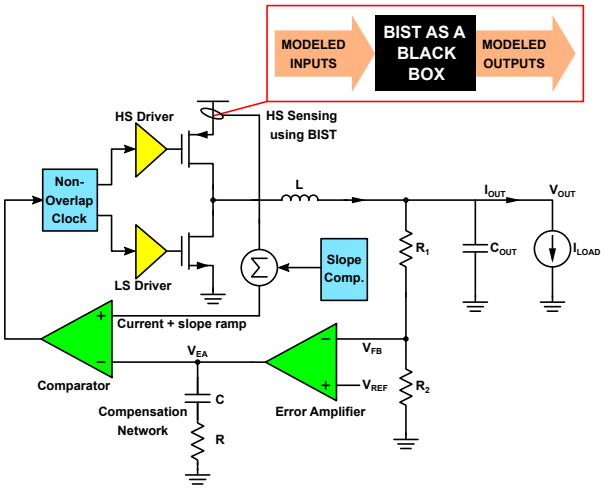

Fig. 2. Example of BIST insertion into a DC-DC Buck converter power stage

BIST circuit synthesis, the BIST target performance parameters are determined based on this chosen BIST architecture and DUT performance. This automated BIST design can be illustrated for the DC-DC converter's power stage as the DUT given in Fig. 2. In this example, the designer needs to monitor the converter's high-side switch current, with DUT specifications that include: the maximum and minimum current in the power stage, the DUT impedance at the BIST insertion point, and the maximum allowable DUT efficiency degradation with BIST insertion. Using the black box modeling approach, the algorithm selects the BIST architecture and defines the BIST target specifications. For example, the maximum load current flowing through the DUT would determine the current monitoring conversion ratio and BIST transistor sizes for a current mirroring BIST architecture. The BIST insertion point impedance translates to the BIST circuit's input impedance requirement. And, the maximum allowable efficiency degradation would limit the BIST circuit's power consumption and limit the minimum current ratio for a BIST current mirroring architecture such as that given in Fig. 3(e).

III. Proposed Design Synthesis Flow

Once the BIST architecture is selected, the algorithm used to synthesize (size) the BIST circuit is similar to that in [7]. The sizing algorithm is detailed in Fig. 4. The algorithm uses Multivariate Regression models to draw relationships between the BIST circuit design variables and BIST target specifications. This MVR model is then optimized using Geometric Programming. The design variables and target performance parameters are put through an analytical knowledge-based decision filter to sample only the most relevant design space for the BIST circuit sizing. Heatmaps and regression scores, which demonstrate the correlation coefficients between the BIST design variables and target performance are then extracted to confirm the strength of the linear relationship between the design variables and the target performance. If there is a linear relationship, we draw up a Multivariate Regression (MVR) model using Machine Learning tools as in [7]. The MVR model includes equations extracted from machine learning

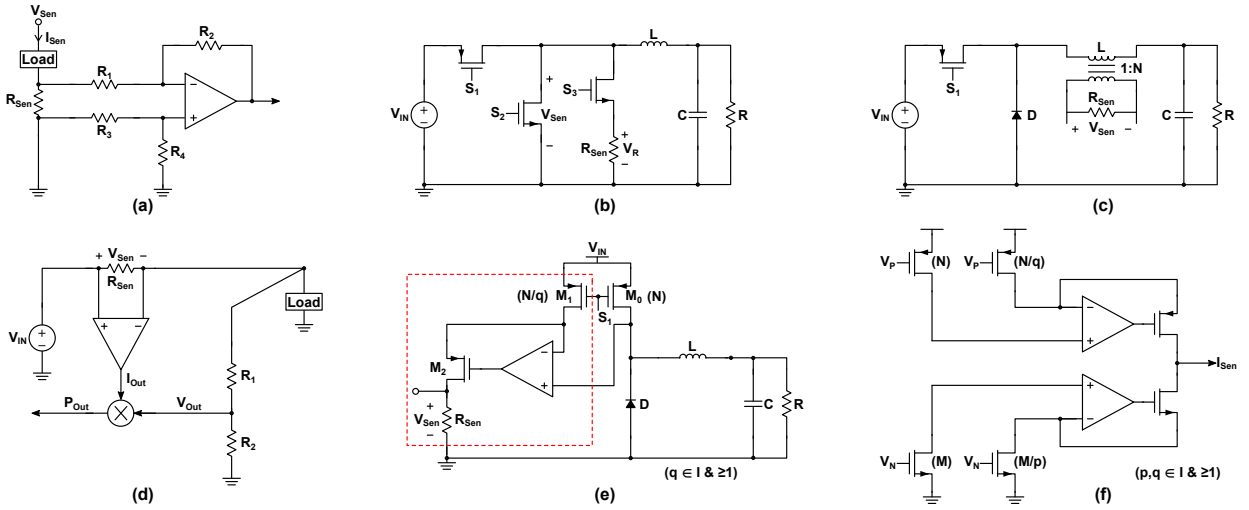

Fig. 3. Various current sensing architectures for BIST insertion.

tools that relate design variables of the BIST circuit, such as the transistor sizing of a current sense circuit, to the target specifications of the BIST circuits. The extracted equations are defined in eqs. (1) and (2), where ϕ is the target specification of the BIST, α terms are coefficients extracted from the ML algorithms, and x_i are the design variables of the BIST circuit.

$$\phi_r(x) = \sum_{j=1}^{j=K} \alpha_{rj} \prod_{i=1}^{i=n} x_i^{\beta_{rij}} \qquad \forall\, r \in \{1, ..., k\} \tag{1}$$

$$\alpha_{rj} \in \mathbb{R} \quad and \quad i, j \in \mathbb{I}, \tag{2}$$

These MVR models are then formulated as a Geometric Programming (GP) problem, similar to work in [7]. The presented algorithm optimizes the target performance of the BIST circuit, while restricting the component sizing to certain upper and lower limits. The GP equations used to optimize the circuit are given in [7]. The target specification of the BIST was decided based on specifications from higher levels of abstraction determined using knowledge-based library.

IV. Experimental Results

The presented design methodology for DA of BIST circuits was verified using a developed BIST current sense library and a DC-DC converter's power stage as the DUT (Fig. 2), where the BIST requirement was to monitor the high-side switch current. Two DC-DC converter power stages were designed (Case A and Case B) with specifications summarized in Table I. There are multiple ways of current sensing [8], for instance using MOSFET on-resistance (R_{ds}), a sense resistor (in series with inductor), filter-sense the inductor, a current transformer, etc. Each of these circuits and methods has tradeoffs in terms of linearity, power loss (efficiency degradation), load on the DUT, and cost (e.g. non-integrability). The trade-off analysis is performed using analytical data of the various current sense methods to select the best fitting sense circuit for a particular system. The algorithm chose the BIST current sensing circuit architecture of Fig. 3(e). This selection was made based on linearity, integratability, and minimal loading to the DUT, as the BIST is connected at a high impedance node of the DUT and exhibits low power consumption. The selected architecture is clearly linear when it comes to sensing the DUT current due to the current mirror structure. Additionally, it is integratable in the sense that it does not affect the main DUT circuit workings. There is minimal loading as the gate of the sense transistor is very high impedance thus causing minimal current to flow into the BIST circuit compared to other architectures. This is a part of the knowledge-based library.

The two converter power stages and associated BIST circuitry were designed in the ONSEMI I3T25 0.35 μm silicon

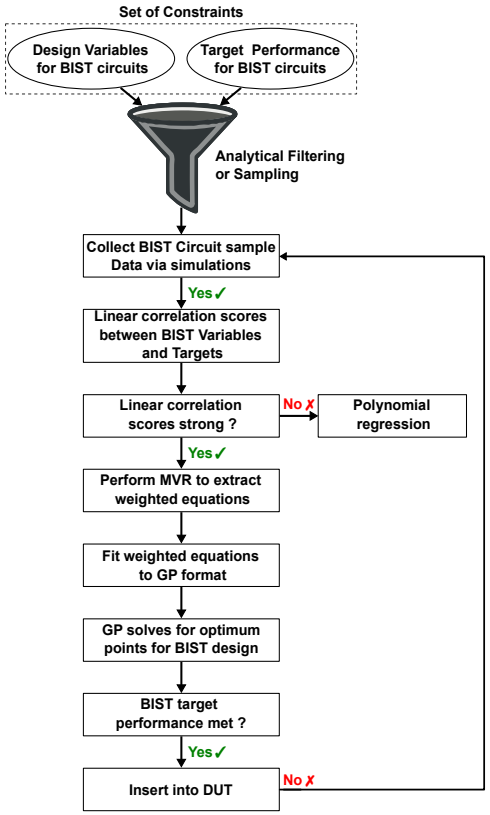

Fig. 4. Simulation-Based Design Automation Flow Diagram

TABLE I
AUTOMATION SIZING RESULTS FOR CASE A AND CASE B SPECIFICATIONS

Switching Converter Case-A:	**BIST Target**	**BIST Sizing**		**BIST Performance**	
Switching Frequency= 10 MHz Vin= 10 V, Vout= 5 V Imin=80.76 mA, Imax=140.7 mA $I_{ripple} = 5\%$ of Average Current $V_{ripple} = 10\ mV$ Efficiency= 89.63%	Current Sense Accuracy $\geq$ 95%	OpAmp Gain/BW	75 dB / 62 MHz	Current Sense Accuracy	98.5%
	Efficiency Degradation $\leq$ 2%	W_{Mirror} (M_1)	9.0 μm	Efficiency Degradation	0.86%
	Power Consumption $\leq$ 10 mW	W_{BIST} (M_2)	4.1 μm	Power Consumption	5.5 mW
Switching Converter Case-B:	**BIST Target**	**BIST Sizing**		**Performance**	
Switching Frequency= 1 MHz Vin= 12 V, Vout= 3.3 V Imin=70.13 mA, Imax=127.6 mA $I_{ripple} = 5\%$ of Average Current $V_{ripple} = 5\ mV$ Efficiency= 92.34%	Current Sense Accuracy $\geq$ 95%	OpAmp Gain/BW	75 dB / 62 MHz	Current Sense Accuracy	97.89%
	Efficiency Degradation $\leq$ 2%	W_{Mirror} (M_1)	6.7 μm	Efficiency Degradation	1.84%
	Power Consumption $\leq$ 5 mW	W_{BIST} (M_2)	6.0 μm	Power Consumption	2.7 mW

process technology used for high voltage power electronics. The power MOSFET device models were provided by the foundry. The BIST target performance parameters are current monitoring capability (current sense accuracy %), minimum (I_{min}) and maximum (I_{max}) load current sensing (based on DUT output power), system efficiency degradation (DUT + BIST), and BIST power consumption. Within the BIST circuit, the operational amplifier's gain was varied along with the transistors' widths (W_{Mirror} and W_{BIST}) and resistor (R_{SEN}) size to collect a dataset for the MVR model. A heatmap diagram and regression scores were extracted to judge the strength of the linear relationship between the BIST target performance parameters and BIST design variables. The regression scores are presented in Table II. A perfectly linear dependency between design and performance parameters would be seen with a perfect regression score of 1.0. In practice, an acceptable MVR score is above 0.3. The MVR model scores 0.6 and higher for the presented dataset which suggests our dataset shows strong linear relationship to build models. The MVR equations extracted using the $scikit - learn$ tool in Python are then put into the GP problem and optimized for best sizing. The algorithm selects optimum transistor widths with a process-fixed length (L) of 1.65 μm for all transistors. The BIST sizing results and performance parameters are summarized in Table I. The value of R_{SEN} was synthesized to be 100 Ω for both design cases. In both cases, the automatically designed BIST meets the required specifications. The transient waveforms for the high-side power stage current (M_0) and the BIST current tracking FET (M_2) for Case-A are shown in Fig. 5 demonstrates that the designed BIST is able to accurately sense the current, with a scaled-down magnitude (1/100) to reduce BIST power consumption. Therefore, the DA algorithm was verified for two test cases and produces successful BIST circuit designs within a few seconds by using MVR modeling with GP.

TABLE II
MULTIVARIATE REGRESSION MODEL SCORES (R^2) FOR THE BIST

	Current Sense Accuracy	**Power Consumption**	**Efficiency Degradation**
W_{Mirror}	0.26	0.32	0.30
W_{BIST}	0.25	0.33	0.32
OpAmp Gain	0.58	1.0	0.26
R_{SEN}	0.21	0.25	0.28
MVR (Set A)	0.63	0.71	0.74
MVR (Set B)	0.70	0.50	0.93

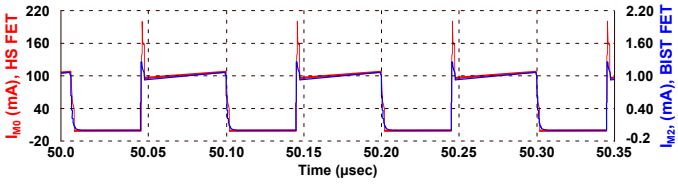

Fig. 5. Simulated steady state waveforms of High Side FET (M_0) current and BIST Sensed FET (M_2) current

V. CONCLUSION

This work presents a rapid method to design BIST circuits using a knowledge-based algorithm and BIST libraries paired with a circuit level DA algorithm that builds MVR models relating the BIST target parameters to the BIST circuit sizing variables. The BIST performance parameter outcomes are optimized using a statistical GP algorithm. While there is scope for improvements, this is a step towards automating analog BIST circuits, decreasing overall system design time and allowing designers to focus on the DUTs.

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