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Title: The effect of intrinsic layer on the performance of oxide-based p-i-n hetero junctions integrating p-SnOx and n-InGaZnO

The discovery of oxide electronics is of increasing importance today as one of the most promising new technologies and manufacturing processes for a variety of electronic and optoelectronic applications such as next-generation displays, batteries, solar cells, and photodetectors. The high potential use seen in oxide electronics is due primarily to their high carrier mobilities and their ability to be fabricated at low temperatures. However, since the majority of oxide semiconductors are n-type oxides, current applications are limited to unipolar devices, eventually developing oxide-based bipolar devices such as p-n diodes and complementary metal-oxide semiconductors.

We have contributed to wide range of oxide semiconductors and their electronics and optoelectronic device applications. Particularly, we have demonstrated n-type oxide-based thin film transistors (TFT), integrating In2O3-based n-type oxide semiconductors from binary cation materials to ternary cation species including InZnO, InGaZnO (IGZO), and InAlZnO. We have suggested channel/metallization contact strategies to achieve stable TFT performance, identified vacancy-based native defect doping mechanisms, suggested interfacial buffer layers to promote charge injection capability, and established the role of third cation species on the carrier generation and carrier transport.
More recently, we have reported facile manufacturing of p-type SnOx through reactive magnetron sputtering from a Sn metal target. The fabricated p-SnOx was found to be devoid of metallic phase of Sn from x-ray photoelectron spectroscopy and demonstrated stable performance in a fully oxide based p-n heterojunction together with n-InGaZnO. The oxide-based p-n junctions exhibited a high rectification ratio greater than 103 at ±3 V, a low saturation current of ~$2x10^{-10}$, and a small turn-on voltage of -0.5 V.

With all the previous achievements and investigations about p-type oxide semiconductors, challenges remain for implementing p-type oxide realization. For the implementation of oxide-based p-n heterojunctions, the performance needs to be further enhanced. The current on/off ration may be limited, in our device structure, due to either high reverse saturation current (or current density) or non-ideal performance.

In this study, two rational strategies are suggested to introduce an “intrinsic” layer, which is expected to reduce reverse saturation current and hence to increase the on/off ratio in between p-SnOx and n-IGZO. The carrier density of n-IGZO is engineered in-situ during the sputter process, by which compositionally homogeneous IGZO with significantly reduced carrier density is formed at the interface. Then, higher carrier density IGZO is formed continuously on the lower carrier density IGZO during the sputter process without any exposure of the sample to the air. Alternatively, heterogeneous oxides of MgO and SiO2 are integrated in between p-SnOx and n-IGZO, by which the defects on the surface can be passivated. The interfacial properties are thoroughly investigated using transmission electron microcopy and atomic force microscopy. The I-V characteristics are compared between the set of devices integrated with two types of “intrinsic” layers.

The current research results are expected to contribute to the development of p-type oxides and their industrial application manufacturing process that meet current processing requirements, such as mass production in p-type oxides semiconductors.

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