Strategies to Enhance the Capability of Carrier Injection to the Effective Channel for Bottom-gated Amorphous Oxide Thin Films Transistors

Mingyuan Liu[a], Hyeonghun Kim[a], Han Wook Song[b], Sunghwan Lee[a]*

[a]School of Engineering Technology, Purdue University, West Lafayette, IN 47907, USA.
[b]Center for Mass and Related Quantities, Korea Research Institute of Standard and Science, Daejeon 34113, South Korea.

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*Corresponding author: sunghlee@purdue.edu

Abstract

Over the two decades, amorphous oxide semiconductors (AOSs) and their thin film transistor (TFT) channel application have been intensely explored to realize high performance, transparent and flexible displays due to their high field effect mobility (μ_{FE}=5-20 cm^2/Vs), visible range optical transparency, and low temperature processability (25-300 °C).[1-2] The metastable amorphous phase is to be maintained during operation by the addition of Zn and additional third cation species (e.g., Ga, Hf, or Al) as an amorphous phase stabilizer.[3-5] To limit TFT off-state currents, a thin channel layer (10-20 nm) was employed for InZnO (IZO)-based TFTs, or third cations were added to suppress carrier generations in the TFT channel. To resolve bias stress-induced instabilities in TFT performance, approaches to employ defect passivation layers or enhance channel/dielectric interfacial compatibility were demonstrated.[6-7]

Metallization contact is also a dominating factor that determines the performance of TFTs. Particularly, it has been reported that high electrical contact resistance significantly sacrifices drain bias applied to the channel, which leads to undesirable power loss during TFT operation and issues for the measurement of TFT field effect mobilities. [2, 8] However, only a few reports that suggest strategies to enhance contact behaviors are available in the literature. Furthermore, the previous approaches (1) require an additional fabrication complexity due to the use of additional treatments at relatively harsh conditions such as UV, plasma, or high temperatures, and (2) may lead to adverse effects on the channel material attributed to the chemical incompatibility between dissimilar materials, and exposures to harsh environments. Therefore, a simple and easy but effective buffer strategy, which does not require any additional process complexities and not sacrifice chemical compatibility, needs to be established to mitigate the contact issues and therefore achieve high performance and low power consumption AOS TFTs.

The present study aims to demonstrate an approach utilizing an interfacial buffer layer, which is compositionally homogeneous to the channel to better align work functions between channel and metallization without a significant fabrication complexity and harsh treatment conditions. Photoelectron spectroscopic measurements reveal that the conducting IZO buffer, of which the work function (Φ) is *4.37 eV*, relaxes a relatively large Φ difference between channel IZO (Φ=*4.81 eV*) and Ti (Φ=*4.2-4.3 eV*) metallization. The buffer is found to lower the energy barrier for charge

carriers at the source to reach the effective channel region near the dielectric. In addition, the higher carrier density of the buffer and favorable chemical compatibility with the channel (compositionally the same) further contribute to a significant reduction in specific contact resistance as much as more than 2.5 orders of magnitude. The improved contact and carrier supply performance from the source to the channel lead to an enhanced field effect mobility of up to 56.49 cm^2/Vs and a threshold voltage of 1.18 V, compared to 13.41 cm^2/Vs and 7.44 V of IZO TFTs without a buffer. The present work is unique in that an approach to lower the potential barrier between the source and the effective channel region (located near the channel/dielectric interface, behaving similar to a buried-channel MOSFET [9]) by introducing a contact buffer layer that enhances the field effect mobility and facilitates carrier supply from the source to the effective channel region.

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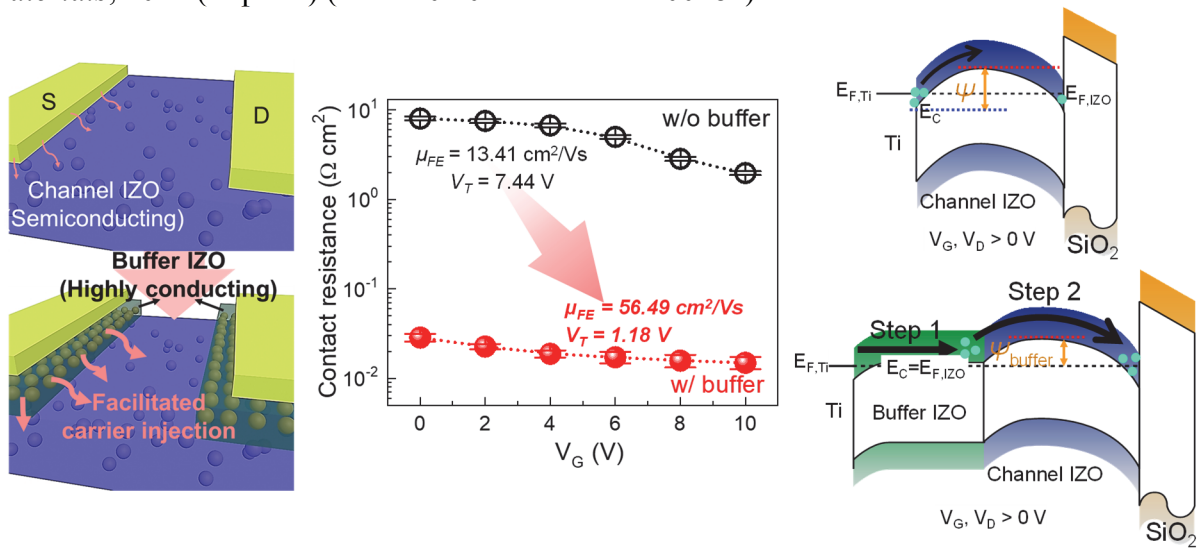

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