High Sensitivity Near-zero Power Wakeup Receiver for Backscattering RF Tags

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***Abstract*—We present a wake-up receiver amenable to integration in a node of RF backscattering tag-to-tag network. A high input impedance of a passive envelope detector (ED) is accomplished by backward bias that improves the passive voltage gain. Two differential outputs are ac-coupled to a baseband amplifier that operates in the subthreshold region. We develop a closed-form model of the passive ED in order to predict the output and ripple voltages and therefor the receiver's sensitivity. The wake-up receiver is implemented in 180 nm CMOS technology and consumes 2 nW with 0.8 V supply voltage while demodulating 915 MHz amplitude-shift keying (ASK) signal with data rate of 10 kbps. The receiver demonstrates -67.98 dBm sensitivity in resolving ASK modulated signal.**

***Index Terms*—envelope detector, wake-up receiver, sensitivity, rectifier, low power wireless communication**

I. Introduction

In the conventional wireless sensor networks, the energy cost of communication is typically orders of magnitude higher than the energy cost of computation [1]. The sensor nodes have to be in a sleep mode for long periods of time in order to conserve energy and extend battery lifetime. An event-based sensor node architecture that integrates a wake-up receiver (WuRx) has been widely exploited [2]–[4]. LNA-less receivers have been implemented with the gain shifted to the low IF frequencies [5] and these architectures achieve a sensitivity of -88 dBm at 250 kbps data rates [6]. However, the power consumption on the order of 10s of μW is prohibitive in large number of applications. Recently proposed WuRx architectures are based on the envelope detection and they operate at nW power level with sensitivity on the order of -80 dBm. This sensitivity is achieved using active envelope detectors that provide a high passive voltage gain [7], [8]. Passive envelope detectors exploiting passive voltage gain transformer achieve similar sensitivity [9]. The receiver sensitivity is also improved by suppression of wideband interference through an external RF filter.

In contrast to the active transceiver systems, the backscatter communication is based on the modulated reflection of a transmitter antenna. In conventional RFID technology [10], the backscatter signal reflected of an RFID tag is captured by a high-sensitivity active receiver with carrier-cancellation at RFID reader. A new paradigm shift in the backscatter communication presents a tag-to-tag communication [11], [12], in which the passive receiver demodulates the backscatter signal, an ASK signal with low modulation index [13]. The modulation index is related to the distance between the tags and the communication range is therefore determined by the ability of detector to resolve such input signals [13]. The sensitivity of the detector is thus defined by the lowest backscatter power that it can resolve. A range of ASK demodulators that can detect low modulation signals has been reported in literature, however with the reported power consumption on the order of μW [14]–[17].

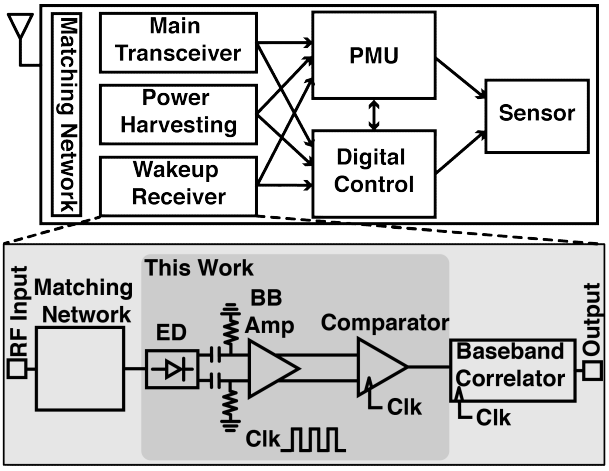


Fig. 1. System block diagram of a backscattering RF tag (top) and system-level architecture of wake-up receiver (bottom). RF tag additionally integrates a main transceiver, energy harvester along with a power management unit (PMU), a digital control unit and potentially a sensor. The highlighted block shows the scope of this paper.

Additional challenge in the design of passive receiver in backscattering tag presents simultaneous RF energy harvesting along with data detection and demodulation. This calls for a dedicated WuRx in the backscattering tag that resolves the backscattering signal as weak as possible with extremely low power consumption, while having limiting effect on the operation of the energy harvesting circuit.

The proposed architecture of backscattering RF tag that integrates wake-up receiver is shown in Fig. I. We present a design of WuRx that achieves -67.98 dBm sensitivity with only 2 nW by:

- arranging the passive ED in a pseudo-balun topology to perform single-ended to differential conversion and improve the conversion gain by 2× compared to a conventional single-ended passive ED.

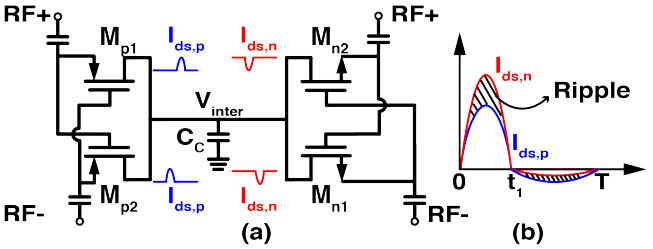


Fig. 2. (a) A fully differential passive ED at the inter stage. (b) Illustration of the currents through nmos and pmos transistor in a single branch.

- increase the effective input resistance as well as a body-biasing technique to reduce the input capacitance,
- a multistage passive ED architecture, which, unlike active EDs, does not have 1/f noise [7].

The paper is organized in a following manner. Section II presents the model of the differential envelope detector, that results in estimates of the output voltage and voltage ripple. Section III details the circuit implementation of WuRx, with the simulation results presented in Section IV. Section V outlines the future work.

II. Modeling of the Differential Wake-up Receiver for Low Input RF Power

The sensitivity of the WuRx is determined by the ripple voltage at the output of envelope detector [13]. In this section, we estimate the output voltage and voltage ripple of the passive fully-differential multi-stage rectifier, where each stage is implemented in cross-coupled bridge configuration [18]. At each inter stage, four transistors are connected with smoothing capacitors C_c as shown in Figure 2(a).

A. Output Voltage of Passive Multi-stage Envelope Detector

To calculate the steady state output voltage of the passive ED, a constant input RF power level is assumed. The RF inputs, RF^+ and RF^-, are ac-coupled to the source and gate of each transistor in ED. We assume that all transistors operate in subthreshold region at low input RF power. The symmetric substhreshold drain-to-source current is give by:

$$I_{ds} = I_{so}(e^{\frac{V_{gs}}{U_t}} - e^{\frac{V_{gd}}{U_t}}) \tag{1}$$

where U_t is thermal voltage and current I_{so}

$$I_{so} = 2n\frac{\beta}{L}U_t^2 e^{-\frac{V_{th}}{U_T}} \tag{2}$$

depends on process. n is the slope factor, β is transconductance factor, L is the length of transistor and V_{th} is the threshold voltage. If RF^+ is positive, M_{p1} conducts and current flows from the input source to the output while M_{n1} turns on to absorbs the current from M_{p1}, as illustrated in Figure 2(b). M_{p2} and M_{n2} are reversely biased at the same time. In the next half cycle, RF^+ swaps with RF^-, M_{p1} and M_{n1} are off while M_{p2} and M_{n2} turn on. The charge conversion principle

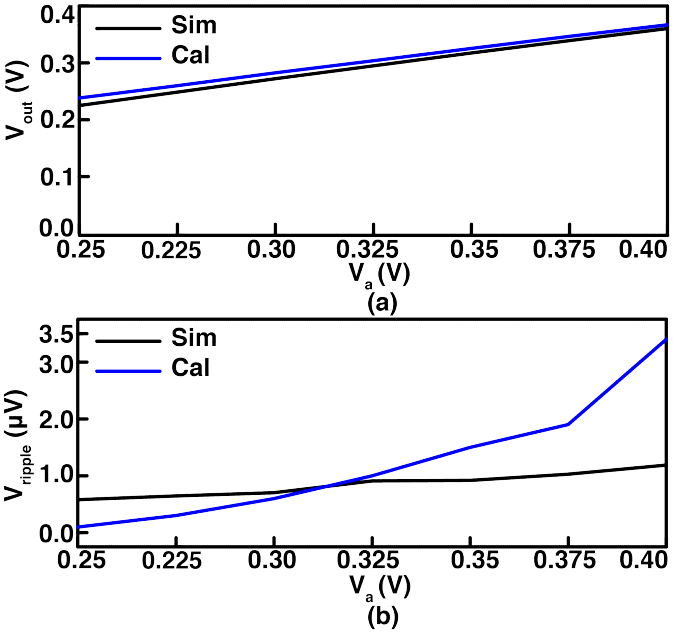


Fig. 3. Calculated and simulate values of (a) the output voltage and (b) voltage ripple at the inter stage of ED.

for the current flow in each pair of transistors to the inter stage capacitor is used to derive the output voltage

$$Q_{p1} + Q_{n1} + Q_{leak} = 0 \tag{3}$$

where Q_{p1} and Q_{n1} represent the charge flow into and out of the M_{p1} and M_{n1}. The third term Q_{leak} represents the charge flow due to the leakage current in the circuit and is negligible. The accumulated charge Q_{p1} and Q_{n1} are expressed as

$$\begin{aligned} Q_{p1} &= -\int_0^{T/2} I_{sop}W_p(e^{\frac{2V_a cos\omega t}{U_t}} - e^{\frac{V_{out}+V_a cos\omega t}{U_t}})dt \\ Q_{n1} &= \int_0^{T/2} I_{son}W_n(e^{\frac{2V_a cos\omega t}{U_t}} - e^{\frac{V_{out}+V_{off}+V_a cos\omega t}{U_t}})dt \end{aligned} \tag{4}$$

The V_{off} accounts for the mismatch between the PMOS and NMOS transistors in the cascaded stages. The RF signals RF^+ and RF^- are in a form of $V_a cos(\omega t)$. M_{p1} and M_{n1} turn off from $T/2$ to T and the accumulated charge can be neglected during this period.

Substituting (4) into (3), the output voltage at each unit stage can be derived as

$$V_{out} = U_T \ln\left(\frac{I_{son}W_n - I_{sop}W_p}{I_{son}W_n e^{-\frac{V_{off}}{U_T}} - I_{sop}W_p} * \frac{I_0(\frac{2V_a}{U_T})}{I_0(\frac{V_a}{U_T})}\right), \tag{5}$$

where I_0 denotes the zero-order modified Bessel function of the first. From (5) it seems that the output voltage only depends on the ratio of the transistor widths W_p/W_n. However, the input impedance R_{in} of passive ED decreases for the wider transistors, even if the width ratio is kept constant. This degrades the passive voltage gain $A = \sqrt{R_{in}/R_{ant}}$ from matching network and reduces V_a. At the same time, wider

transistors improve charge capacity and reduce voltage ripple at the inter stage nodes.

The calculated output voltage after a single stage ED is shown in Figure 3(a), along with the simulated value, verifying the proposed model.

B. Estimation of Output Voltage Ripple

Figure 2(b) illustrates how the difference between PMOS and NMOS drain-to-source current contributes to voltage ripple at inter node between stages. However, $I_{ds,n} - I_{ds,p}$ is a non-integrable equation, except when integrating from 0 to π. To strike a reasonable balance between simplicity and accuracy, two assumptions are made to derive a closed-form expression. Firstly, we assume that the drain-to-source current is equal to the peak current value at $\omega t = 2\pi$. Then, we assume that the integrating range is given as one third of time point at which the source is at the same voltage level as the drain.

$$V_{ripple} = \int_{-t_1}^{t_1} \frac{(I(2\pi)_{ds,n} - I(2\pi)_{ds,p})}{C_c} dt$$
$$t_1 = \frac{1}{3} arccos(\frac{V_{out}}{V_a})/\pi \quad (6)$$

The calculated ripple voltage along with the simulated ripple voltage at the output of the first stage is shown in Figure 3(b). The calculated value deviates from the simulated voltage when the input voltage increases as the transistors move into strong inversion, while in the low voltage range the deviation is caused by the body-diode leakage current.

III. Circuit Implementation

The wake-up receiver integrates the envelope detector and baseband amplifier, along with the comparator and correlator. The details of the circuit implementation of these blocks follow.

A. Envelope Detector

The envelope detector utilizes a multi-stage rectifier configuration as illustrated in Figure 4. Unit stages are cascaded in series along the DC path and in parallel connected to the input RF ports through ac-coupled capacitor. As the number of stages, N, increases, input impedance R_{in} of ED drops and limits the achievable passive voltage gain, given as $V_{RF} = \sqrt{2P_{in}R_{in}} \propto \sqrt{N}$. In Figure 5(a), ED output voltage ripple is shown versus the number of stages, N. The output voltage for even number of stages is $V_{ED,pn} = 2N(V_{out})$. The sensitivity of the receiver is defined by the signal-to-noise ratio(SNR), $\Delta V_{out}/\Delta V_{Ripple}$. To optimize the SNR, the number of stages is chosen as $N = 6$.

The bulk of transistor in each stage is biased from backward stages to reduce the bulk-to-source junction diode leakage. The threshold voltage is increased and effectively maximizes the passive ED input impedance. This further increases the passive voltage gain from the matching network. One additional stage with smaller transistor sizes is added at each side to provide the backward bias voltage. Additionally, auxiliary stages enhance

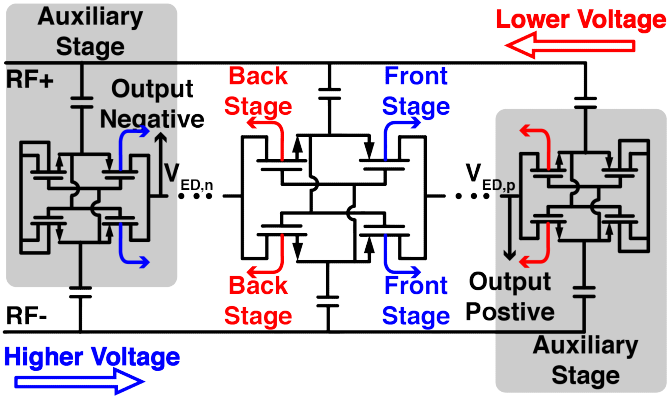


Fig. 4. Proposed six stages envelope detector with two auxiliary stages.

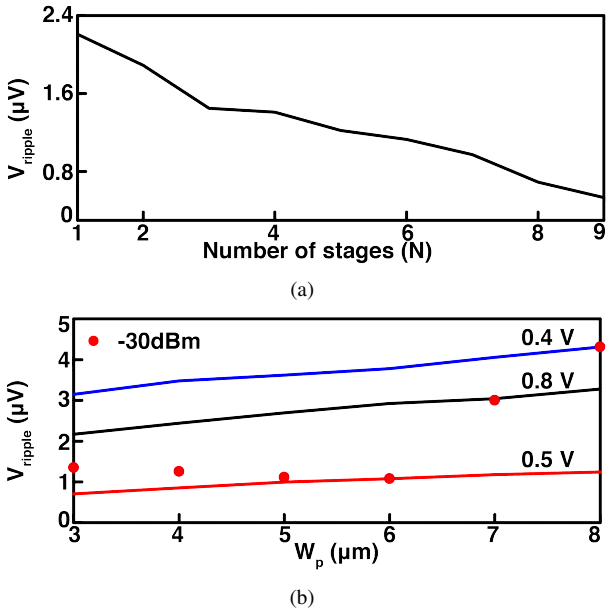


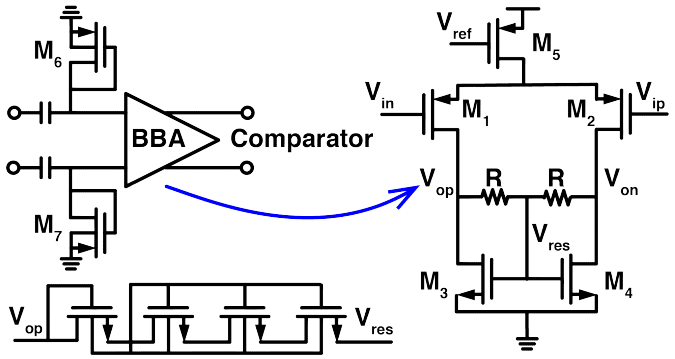
Fig. 5. Simulated V_{ripple} of passive ED for: (a) N stages with -30 dB input power level, (b) and different transistors size with $W_p/W_n = 2$ at constant input voltage and -30 dBm input power.

symmetry as unbalanced PMOS and NMOS channel resistances are connected with baseband amplifier input impedance, and reduce the ED offset voltage between two opposite ED outputs.

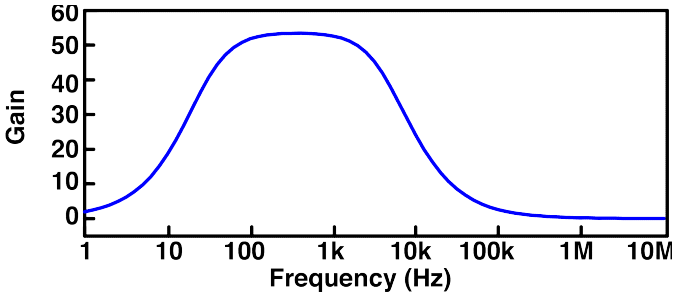
Conventionally, the large load capacitor C_L is used to reduce the output ripple voltage. From (5), the output voltage is almost constant if the width ratio W_n/W_p is fixed. On the other hand, for a fixed width ratio, increased sizing of the transistors results in the reduced voltage ripple. The Fig.5(b) shows the voltage ripple versus different transistor widths, where the solid lines and dots correspond to constant input voltage and a -30 dBm power level, respectively. $W_p/W_n = 4\mu/2\mu$ is used in the later simulation to balance small ripple and large R_{in}.

B. Baseband Amplifier and Comparator

Due to the low modulation index, the weak baseband signal cannot be distinguished by the comparator. A self-biased,



(a)



(b)

Fig. 6. (a) Schematic of the baseband amplifier preceded by the high-pass filter and implementation of the resistor R. (b) Frequency response of the high-pass filter followed by the baseband amplifier.

17 dB baseband amplifier is implemented in continuous time as shown in Fig. 6(a), in order to relax the high resolution requirement for the comparator.

The high-pass filter precedes the baseband amplifier. The diode-connected PMOS transistors operate as pseudo-resistors to achieve an equivalent resistance greater than 10^{10} Ω and provide 10 Hz high-pass cutoff while rejecting large dc offsets. The gain of the baseband amplifier shows better performance with a higher bias current. The input referred noise is reduced at the same time, as the g_{m1} is larger. Wider input transistors M_1 and M_2 have less $1/f$ noise, however it reduces the drain source voltage headroom. The NMOS pseudo-resistors provide bias for the bottom transistors. Fig. 6(b) shows the gain of the baseband amplifier and the pass band characteristic. The input referred noise

$$V_{in,noise}^2 = 8kT\left(\frac{2}{3g_{m1}} + \frac{2g_{m3}}{3g_{m1}^2}\right) + \frac{2K_{m4}}{C_{ox}W_{m3}L_{m3}f}\frac{g_{m3}^2}{g_{m1}^2} + \frac{2K_{m1}}{C_{ox}W_{m1}L_{m1}f} + \frac{4kT}{Rg_{m1}^2} + \frac{2K_{m6}}{C_{ox}W_{m6}L_{m6}f} \quad (7)$$

is 0.2 μV. This verifies that the noise in the ASK wake-up receiver is dominated by the passive ED, which is optimized to improve the sensitivity, as previously described. The core amplifier consumes 2.5 nA to balance the gain and bandwidth.

The two stage dynamic comparator slices the output of the baseband amplifier. The comparator is implemented as a dynamic pre-amplifier followed by a dynamic latch [17]. The kickback charge from comparator is absorbed by symmetrical

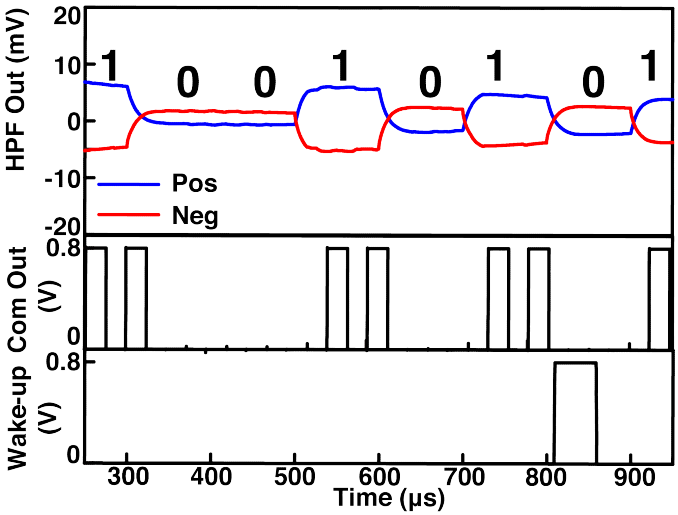


Fig. 7. Transient waveform at 10 kpbs wake-up data pattern of (a) high pass filter output voltage, (b) comprator output and (c) correlator output.

design and ac-coupled capacitor. A RC relaxation oscillator generates the time clock for the comparator and other digital circuitry [19]. The baseband signal is oversampled by 2x, to overcome phase uncertainty and correlated with a pre-defined code-book integrated in the correlator.

IV. Simulation Results

To demonstrate the performance of proposed wake-up receiver, we simulated the circuit with carrier signal at 915 MHz and data rate of 10 kbps. The simulated transient waveforms are shown in Fig. 7 at 1.57 μW input power with 1% modulation index (MI), where the sensitivity is defined as $P_{in} * MI^2$ = -67.98 dBm [20]. Fig. 7 depicts the output of the high pass filter, dynamic comparator and generated wake-up signal, respectively. The carrier signal is modulated with '100101' baseband signal and the circuit wakes up after the correct comparison. The longer correlator wake-up word will improve the sensitivity further, however increasing missing rate at the same time [21].

V. Conclusion

In this paper, a 0.8 V 915 MHz ASK modulated wake-up receiver that achieves -67.98 dBm sensitivity consuming only 2 nW in 0.18 μm CMOS technology is presented. The model of passive differential ED operating in the subthreshold region is developed. The noise contributed by ED is shown to determine the sensitivity in a direct envelope detection receiver architecture, which driven the circuit optimization. A proposed wake-up circuit will be integrated in backscattering RF tag system-on-chip implementation.

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