Performance Assessment of Quantum Processor Based on p-Type Semiconductor Quantum Dot Array

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Abstract— A multiscale simulation method is developed to model and assess silicon- and germanium-hole-based quantum dot (QD) arrays for quantum processors. The multiscale process takes a bottom-up approach, which integrates device-level simulations into quantum circuit simulations for semiconductor QD array processors. This process allows essential device physics to be incorporated in the assessment of quantum circuit performance for a Si- or Ge-QD-based quantum processor. The results show that the Ge hole array provides a promising semiconductor platform to enhance entanglement between neighboring QDs for two-qubit quantum gates. Furthermore, a two-qubit quantum gate based on holes in Ge can achieve fast gate speed, and smaller device variability compared to its Si counterpart. Design and multiscale simulation of the Ge QD array processor shows its potential to achieve high fidelity in preparing the ansatz state of quantum chemistry simulations based on variational quantum eigensolver. The bottom-up, multiscale method developed here can allow the physical design and assessment of semiconductor-QD-based quantum processors from the physical properties of quantum gate devices and their underlying material properties.

Keywords— Semiconductor quantum computing, multiscale simulation, quantum dot array

Poster relevance – Related to QCE22 topics of Quantum Computing, Quantum Hardware Engineering

I. Introduction

Significant progress has been made in the hardware realization of quantum computing based on semiconductors. Two-qubit quantum gates and small-scale quantum processors with high computing speed and high fidelity have been demonstrated on semiconductors [1][2][3]. For example, two-qubit quantum gates based on hole spins in Germanium (Ge) with a fast two-qubit gate operation with a gate time of ~20 ns, and high fidelity of 99.3% have been demonstrated [3]. In group IV semiconductors such as silicon (Si) and Ge, nuclear spin dephasing can be removed through isotope engineering, which is ideal for building a "quiet" semiconductor material system to host qubits. Furthermore, by leveraging the semiconductor industry, semiconductor-based quantum hardware can provide a scalable, low-cost quantum computing platform with extremely high integration density.

Motivated by these recent experiments and the potential of semiconductor QDs for quantum computing in the noisy intermediate-scale quantum (NISQ) era, it is imperative to develop computer-aided simulation and design methods for the design of quantum processors based on semiconductor QD array. While top-down approaches have been generally used for quantum computing algorithms and circuits, co-design of quantum software and hardware has been reported recently [4]. A bottom-up approach that encapsulates essential material and device physics to quantum circuit modeling can facilitate the co-design of semiconductor quantum processors. In this study, a multiscale, bottom-up simulation framework is developed to model a quantum processor based on a semiconductor quantum dot array and to explore its designs and performance [5].

II. Multiscale Simulation Approach

A multiscale simulation approach from numerical device simulations to small-scale quantum circuit simulations is developed to describe the operation of a hole qubit array. We make the assumptions that the single-qubit gates are ideal, and focus on assessing the performance limited by two-qubit quantum gates, which is typically the bottleneck compared to one-qubit gates. The complete workflow of multiscale simulation of hole-based quantum computing, which is shown in Fig. 1., consists of a bottom-up flow from the quantum gate device level to the quantum circuit and algorithm level simulations. The crucial parameters of the device and simulation is shown in Table I.

To obtain the Hamiltonian or device simulation, we numerically discretize a 4-band LK $k \cdot p$ Hamiltonian, H_{LK}, in the vertical confinement direction. The $k \cdot p$ Hamiltonian captures the heavy hole and light hole bands, which are most important for low-energy excitations in a p-type semiconductor

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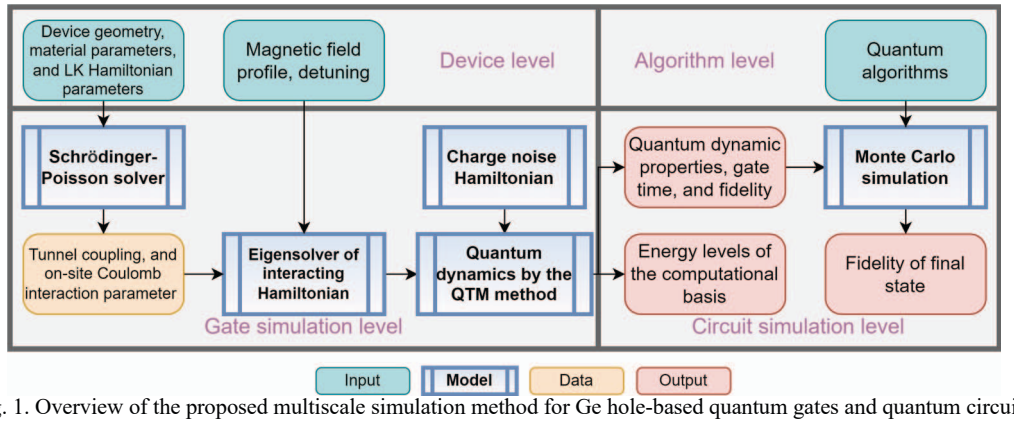


Fig. 1. Overview of the proposed multiscale simulation method for Ge hole-based quantum gates and quantum circuits.

Table. I. Nominal values of the material and device parameters for simulation. (* marks the hitting parameter.)

Device geometry			**Relative dielectric constant**			**Magnetic field (Zeeman splitting)**		**Charge noise***
Plunger gate (PG)	Barrier gate (BG) length	Ge thickness	Ge	$Si_{0.2}Ge_{0.8}$	Al_2O_3	E_Z	ΔE_z	$\langle \delta t_c \rangle$
20×20 nm^2	$(L_s - 4)$ nm	20 nm	16	15.2	9.8	1.0 meV	0.1 meV	0.24 μeV

nanostructure. The details of the Hamiltonian parameters are listed in Ref.[5].

To simulate the quantum gate device shown in Fig. 2(b), numerical device simulations are first performed by solving a 3-D Poisson equation with the Schrödinger equation by using the finite element method (FEM). The single-particle wave equation and eigen-energies obtained from the FEM Schrödinger-Poisson device simulation can be subsequently used to parameterize the tunnel coupling and on-site Coulomb repulsion terms in the quantum gate Hamiltonian as described below.

To understand the quantum gate operation on the computational basis, the Hamiltonian can be projected to the computational basis of $\{|\uparrow\uparrow\rangle, |\uparrow\downarrow\rangle, |\downarrow\uparrow\rangle, |\downarrow\downarrow\rangle\}$ by using the Schrieffer-Wolff transformation. The effective Hamiltonian can be expressed as,

$$H_{eff} \approx \mu_B\left(g_1 B_1 s_{1,z} + g_2 B_2 s_{2,z}\right) + J\left(\boldsymbol{s_1}\cdot\boldsymbol{s_2} - \frac{1}{4}\right), \quad (1)$$

where $s_{1,2}$ are the spin-1/2 operator on QD1 (QD2), the subscript z denotes its z component, and the exchange interaction can be expressed as,

$$J \approx 2t_c^2(U_1 + U_2)/((U_1 - \epsilon)(U_2 + \epsilon)). \quad (2)$$

In the symmetrically biased case, i.e., $\epsilon = 0$, modulation of exchange is achieved through modulation of the tunnel coupling by the barrier gate voltage. It is important to model the dependence of the tunnel coupling on the barrier gate voltage accurately. The lowest energy levels of the DQD structures are binding and anti-binding "molecular" orbits. The value of the tunnel coupling t_c between the DQDs can be simulated numerically from the difference between the energies of the lowest anti-binding and binding states, E_{AB} and E_B, $t_c = |E_{AB} - E_B|/2$ [5].

At the symmetrically biased point, the tunnel noise is dominant over the detuning noise. The tunnel noise Hamiltonian in the basis of $\{|\uparrow\downarrow\rangle, |\downarrow\uparrow\rangle, S_{20}, S_{02}\}$ can be expressed as,

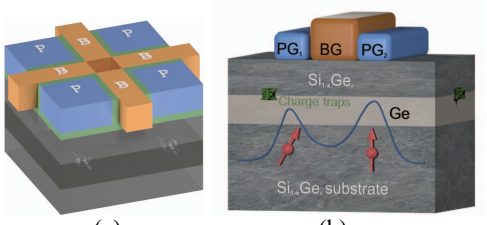
$$H_n = \begin{bmatrix} 0 & 0 & 1 & 1 \\ 0 & 0 & -1 & -1 \\ 1 & -1 & 0 & 0 \\ 1 & -1 & 0 & 0 \end{bmatrix} \delta t_c, \quad (3)$$

where δt_c is the stochastic fluctuation of the tunnel coupling due to charge noise. δt_c is assumed to follow a Gaussian distribution with a mean value of 0 and the standard deviation of A_n, which characterizes the noise amplitude. In the time domain, the noise is assumed to obey the stochastic time dynamics of random telegraph noise [6], with a characteristic time of τ_n. In the isotopically purified semiconductor, dephasing due to nuclear spins can be neglected. We, therefore, focus on charge noise in this work.

To simulate the time evolution and quantum dynamics of the quantum gate and circuit, we use a quantum trajectory method (QTM). In this method, multiple quantum evolution paths in the presence of noise are tracked, and their statistical average behaviors are used to calculate the density matrix and quantum fidelity.

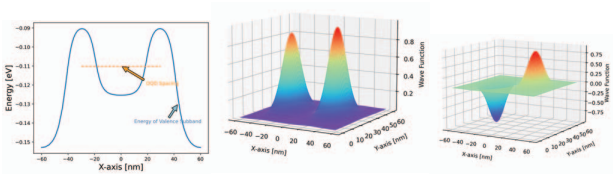
III. Results

To test a basic 2-qubit quantum gate, the devices as shown in Fig. 2(b) is simulated. Figure 3(a) shows the valence band of this 2-qubit system, and the simulated ground state (dashed



(a) (b)

Fig. 2. (a) Schematic layout of a 2×2 QD array for a quantum processor. PG_i is the ith plunger gate, and BG_i is the ith barrier gate. (b) The schematic device structure between 2 neighboring QDs cut at the dashed line in (a).



(a) (b) (c)

Fig. 3. (a) The valence subband profile along x for the two-qubit hole quantum gate as shown in Fig. 2(b), where $L_s = 40$ nm and $|V_{BG}| = 40$ mV. The $Si_{0.2}Ge_{0.8}$ top layer thickness is 10 nm. The simulated wave function of (b) binding state and (c) anti-binding state.

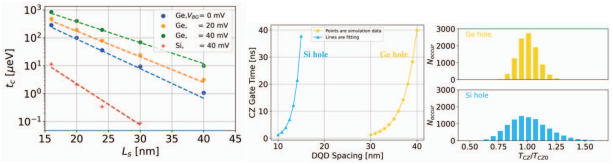
line). The corresponding wave function of the binding state and the next anti-binding state is shown in Fig. 3(b) and 3(c), respectively.

The two-qubit quantum gate performance is assessed next. The tunnel coupling between DQDs in two-qubit gates is calculated as a function of the DQD spacing and barrier gate as shown in Fig. 4(a), [5]. Compared to Si holes, the Ge holes achieve a larger quantum tunnel coupling at various applied barrier gate voltages, due to a smaller in-plane effective mass and enhanced entanglement. Figure 4(b) shows the quantum gate time T_{CZ} as a function of the device size. To achieve a fast, sub-10 ns CZ gate time, a DQD spacing of $L_s < 37$ nm is needed for Ge holes. However, only $L_s < 13$ nm is needed for Si, which is nearly 3 times more stringent. Fig. 4(c) shows the normalized CZ gate time of Ge shows less device-to-device variability compared to that of Si due to the smaller effective mass of Ge [5].

Quantum dynamic characteristics are explored by simulation of the rabi oscillation in the 2-qubit CPHASE gate by using the QTM, which is shown in Fig. 5(a). An envelope function of spin up probability $p_{up} = \exp(-(t/\tau)^2)$ fitted to the simulated oscillation with the extracted phenomenological charge noise magnitude as $\langle \delta t_c \rangle \approx 0.24$ μeV and $\tau = 180\ ns$ by comparing to the experimental data from [3]. Then a QD array processor is examined by preparing a variational quantum eigensolver (VQE) ansatz state in simulation a BeH_2 molecule, which is shown schematically in Fig. 5(b) and can be realized in a processor as Fig. 5(c). The results indicate the potential of Ge-hole-based QD array processors in preparing the ansatz quantum states with high quantum fidelity in the variational quantum algorithm simulations, as shown in Fig. 5(d).

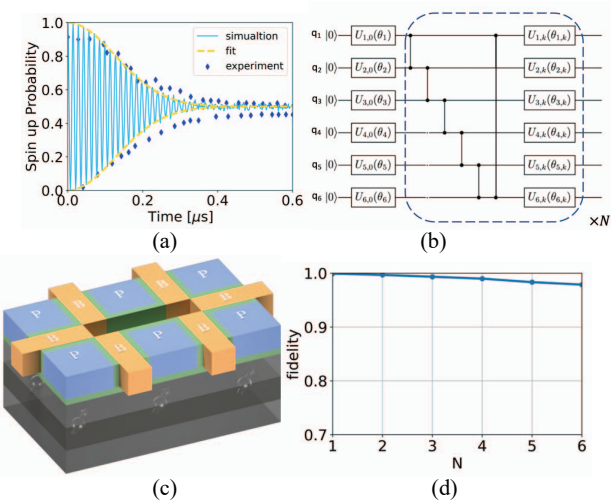
IV. Conclusions

A multiscale simulation method is developed to model and assess the group-IV-semiconductor-hole-based QD array for the quantum processor. The multiscale process takes a bottom-up approach, which allows essential device physics to be incorporated in the assessment of quantum circuit performance for a semiconductor-based quantum processor. The simulation results indicate that two-qubit quantum gates based on holes in Ge can achieve fast gate speed, and smaller device variability compared to their Si counterpart. Furthermore, multiscale quantum circuit simulations of the Ge QD array processor show its potential to achieve high fidelity in preparing the ansatz state in variational quantum algorithm simulations.



(a) (b) (c)

Fig. 4. (a) Tunnel coupling vs. the DQD spacing at different barrier gate voltage magnitudes of $|V_{BG}| = 0, 20, 40$ mV. Comparison between Si hole devices and Ge hole devices with (b) CZ gate time vs. DQD spacing, and (c) distribution of normalized CZ gate time.



(a) (b) (c) (d)

Fig. 5. (a) The simulated exchange oscillation (solid line) compared to the experimental data of the exchange oscillation envelope extracted from Ref. [3] (symbols). (b) Quantum circuit for preparing a VQE ansatz state in simulation a BeH_2 molecule. The subcircuit in the cashed box can be repeated in cascade for $N \geq 1$ times. (c) Design of a six-qubit quantum processor of a 2D QD array for efficiently implementing the quantum circuit in (a). (d) The fidelity of preparing the ansatz state vs. the number of repeating stages N as denoted in (a).

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