

PAPERTRONICS: FULLY PAPER-INTEGRATED RESISTOR, CAPACITOR, AND TRANSISTOR CIRCUITS

Mya Landers¹, Anwar Elhadad¹, and Seokheun Choi^{1,2*}

¹Bioelectronics & Microsystems Laboratory, Department of Electrical & Computer Engineering, State University of New York at Binghamton (SUNY Binghamton), Binghamton, New York, USA

²Center for Research in Advanced Sensing Technologies & Environmental Sustainability, SUNY Binghamton, Binghamton, New York, USA

ABSTRACT

This work presents fabrication techniques for achieving individual electronic components both on the surface and within the fibers of a paper substrate, attaining full integration of paper and functional electronics materials. A process of hydrophobic wax patterning coupled with conductive and semiconductive poly(3,4-ethylenedioxythiophene): poly(styrene sulfonic acid) (PEDOT: PSS)-based ink injection and screen-printing has allowed for the implementation of all-paper-based, tunable resistors, capacitors, and transistors. The characteristics of the paper resistors can be adjusted as desired through finetuning of the PEDOT: PSS-based ink recipe, and the components can be combined in various arrangements to attain paper-based printed circuit boards (PCBs) for a wide range of practical applications. As a first step towards multiple component integration, a simple example circuit design is demonstrated that incorporates the three different components. Furthermore, through the strategic organization of the resistors, transistors, and capacitors and stacking of paper layers, more complex and diverse paper PCBs can be attained while minimizing the perceived surface area of the circuitry, allowing for a compact, pliable, and highly customizable means of fabricating paper-based electronic systems.

KEYWORDS

Papertronics, biodegradable, paper transistors, paper resistors, paper capacitors, paper PCBs

INTRODUCTION

The realization of paper-based electronic technologies has long been an ambition for many research groups, as paper-electronic integration offers to improve upon the disposability, affordability, and sustainability of conventional electronic systems [1-5]. Most of the attempted methods for achieving high-level integration, or bottom-up design, have involved utilizing paper as a substrate material only, while the constituents of individual electronic components have remained distinctly non-paper [6, 7]. Due to the rough, fibrous structure of paper, it often fundamentally interferes with material dispersion and electrical flow as recurrent imperfections within the material interrupt operation [8]. This can limit the precision of paper-made electronic interfaces and reduce the resultant device performance. Therefore, to mitigate this issue, the paper substrate often is first coated in a nonporous priming agent and then sequentially layered with the functional materials to attain the desired electronic component architecture on the “paper” surface [6-8]. Alternatively, paper has also been used in the manufacture of PCBs as well, serving simply as a substrate upon which conductive wires, or traces, are printed followed by adhesion of standard off-shelf surface mountable components [2, 9]. However, neither of these integration methods fully retain the flexibility and ease of disposability implied by the use of paper materials, as the attached electronic materials interfere with device bendability and biodegradability. To tackle this issue, paper must take on a more functional role within paper electronic platforms.

Despite this need, a fully integrated paper electronic system has yet to be demonstrated that can take advantage of the paper’s 3D structure by utilizing it as a functional material within circuit components as well as a substrate.

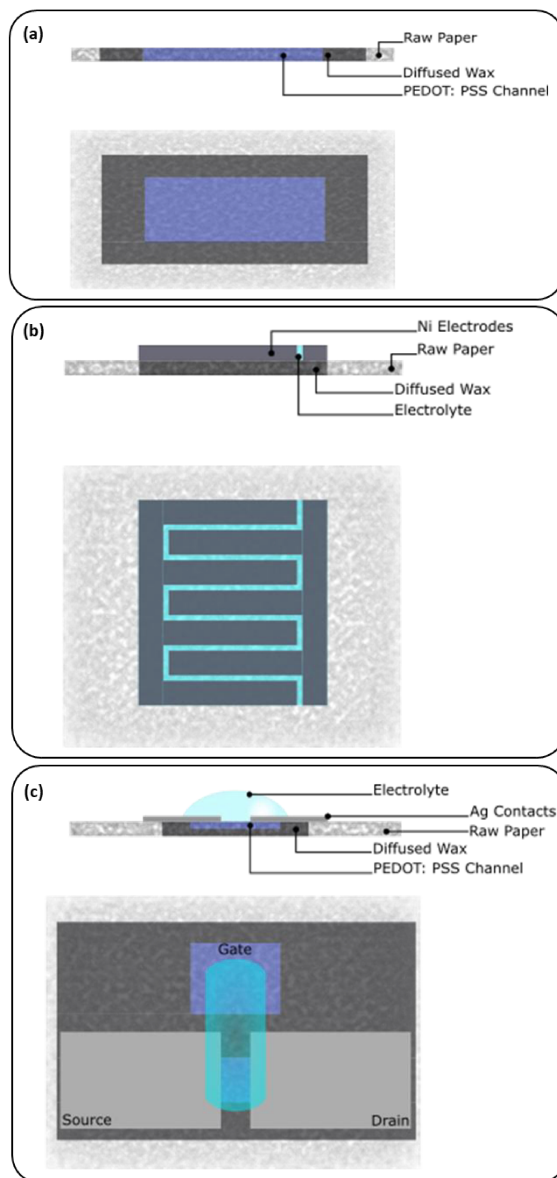


Figure 1: (a) Schematic illustrations of the self-charging power system integrating the MFC and the supercapacitor (back and front view), (b) the MFC inoculated with *B. subtilis* spores and its operating principle with sweat, and (c) the system applied to human.

Herein, our group provided novel approaches to fabrication of paper-based electronic components and PCBs. We successfully designed, assembled, and evaluated three of the most commonly used electronic components on paper: resistors, capacitors, and transistors (Figure 1). These components were achieved through simple, affordable, and rapid fabrication techniques, enabling easy customization and efficient development of paper circuitry for disposable applications.

EXPERIMENTAL PROCEDURE

Materials

Poly(3,4-ethylenedioxythiophene):polystyrene sulfonate (PEDOT:PSS) (Clevios PH1000) was purchased from Heraeus. Dimethyl sulfoxide (DMSO), hydrolyzed polyvinyl alcohol (PVA), and sodium sulfate (Na_2SO_4) were obtained from Sigma-Aldrich. The Whatman Grade 1 filter paper substrate was purchased from VWR. Silver/Silver-Chloride and graphite ink were acquired from Ercon Inc. A nickel conductive spray was purchased from MG Chemicals.

Resistor fabrication

Paper resistors were fabricated by first patterning filter paper with a hydrophobic, wax-printed (Xerox Phaser, ColorQube 8570) boundary with a width of 1 mm and variable length (0.5 cm, 1 cm, 1.5 cm, 3 cm, and 3.5 cm). The wax was diffused throughout the paper fibers via baking at 140°C for 30 s. The paper was then injected with a resistive PEDOT:PSS/DMSO ink. Since DMSO addition enhances the conductivity of PEDOT:PSS, the amount of DMSO in the ink mixture can be manipulated to achieve the desired resistivity [10-12]. Four different ink mixtures were prepared with different ratios of DMSO: 1 wt%, 5 wt%, 10 wt%, and 20 wt%.

Capacitor fabrication

The interdigitated electrolytic capacitor was realized on paper through similar wax-patterning described for the paper resistor. After baking the wax-patterned paper, a mask was laser-cut from copy paper and temporarily pasted onto the filter paper substrate for electrode patterning. The capacitor electrodes were evenly applied via spray coating of a conductive nickel spray. Capacitor electrodes were interdigitated, each with 3 legs of length 10 mm, width 2 mm, and gap 0.75 mm.

A gel electrolyte was prepared with PVA and Na_2SO_4 . A 75 g/L PVA solution was made by stirring hydrolyzed PVA into distilled water at 85°. As this mixture cooled to room temperature, a 106 g/L Na_2SO_4 solution was separately prepared and mixed thoroughly by sonication for 10 min. The Na_2SO_4 solution was slowly added to the PVA solution at a ratio of 1:2 and stirred until clear. The gel electrolyte was cast over the active region of the interdigitated capacitor electrodes and allowed to set overnight.

Transistor fabrication

A planar, electrolytic p-channel FET was fabricated using a PEDOT:PSS/DMSO semiconductive ink to functionalize a paper channel. Wax was printed onto filter paper to define the transistor channel and gate electrode region. The paper was baked at 140°C for 30 s. The functional inks were prepared by sonicating a mixture of PEDOT:PSS and DMSO for 30 min. A 5% DMSO was introduced to the paper channel and a 10% DMSO ink was applied to the gate. After drying, application of the source and drain electrodes were achieved via screen-printing of the silver/silver-chloride ink. A channel length of 4 mm and a width of 2 mm were chosen for the FET dimensions, resulting in a W/L dimension of 1/2. The PVA/ Na_2SO_4 gel electrolyte for the FET was prepared as described for the capacitor electrolyte, and it was

applied over the FET's active region and allowed to solidify before use.

Paper PCB fabrication

The three components (resistors, capacitors, and transistors) were designed to be fabricated into a single sheet of paper to facilitate easier and more rapid manufacturing. Since the electronic components share many of the same materials and fabrication processes, these steps can be carried out simultaneously, allowing for an entire paper PCB to be achieved in almost the same amount of time it takes to create just a single component. The only additional step was the screen-printing of conductive graphene ink trace to interconnect the components as desired as per the circuit design. These connections and placements of components on the PCB were adjusted using AutoCAD software, which can be used to design any other variation or custom paper PCB. The order of fabrication for a PCB is as follows: components' wax boundaries are patterned according to the AutoCAD file and heat-diffused in an oven at 140°C, PEDOT:PSS/DMSO inks are applied to the appropriate component regions and allowed to dry, drain and source electrodes are applied to the FET via screen printing and allowed to dry, conductive traces are patterned, and prepared gel electrolyte is cast onto the capacitor and FET.

Measurement procedure

Resistor values were determined via a Lomvum T28B digital multimeter. Capacitor behavior and transistor behavior were monitored and characterized using an Agilent HP Keysight MSOX3054A oscilloscope and an Agilent E3630A DC power supply.

RESULTS AND DISCUSSION

Resistor Characterization

The resistance values of our fabricated paper resistor were measured with the modifications of three distinct variables: the percentage of DMSO used in the ink recipe, the volume of resistive ink applied, and the length of the paper resistor. The trends and effects of these variable manipulations can be obtained from the plots presented (Figure 2). The resistance range of the plots is kept constant for clearer observation of the attainable resistance values for each percent DMSO increment. Data consistency is also represented in the form of error bars with each point placed at the average of 5 resistor samples.

The collected data shows strong correlations between the three variables and paper resistance. As the percentage of DMSO is increased from 1% to 20%, the heightened conductivity of the ink results in much lower resistances in the resulting paper resistors. Resistors fabricated with 1% DMSO inks attained a maximum of about 285 k Ω , whereas 20% DMSO resistors only reached a resistance of about 3.4 k Ω . Therefore, resistive ink recipes with higher concentrations of DMSO can be used to achieve more finetuned low resistance paper resistors and vice versa. Similarly, the length of the paper resistors and volume of ink utilized can be adjusted to further tailor the resistor characteristics since shorter and more saturated paper resistors exhibit lower resistance. In this way, the DMSO concentration, length, and ink volume used for resistor fabrication can be concurrently altered to achieve practically any desired resistance. With the test cases presented here, including DMSO concentrations between 1% and 20%, lengths between 0.5 cm and 3.5 cm, and ink volumes between 2 μL and 20 μL , the range of resistances achieved was from 26 Ω to 280 k Ω . If necessary for the desired circuit, higher resistances could additionally be realized by further decreasing DMSO concentration and ink volume or increasing length. Furthermore, zig-zag resistor designs can be

implemented to reduce their perceived length while still maintaining larger resistance values, allowing for more compact paper PCB designs.

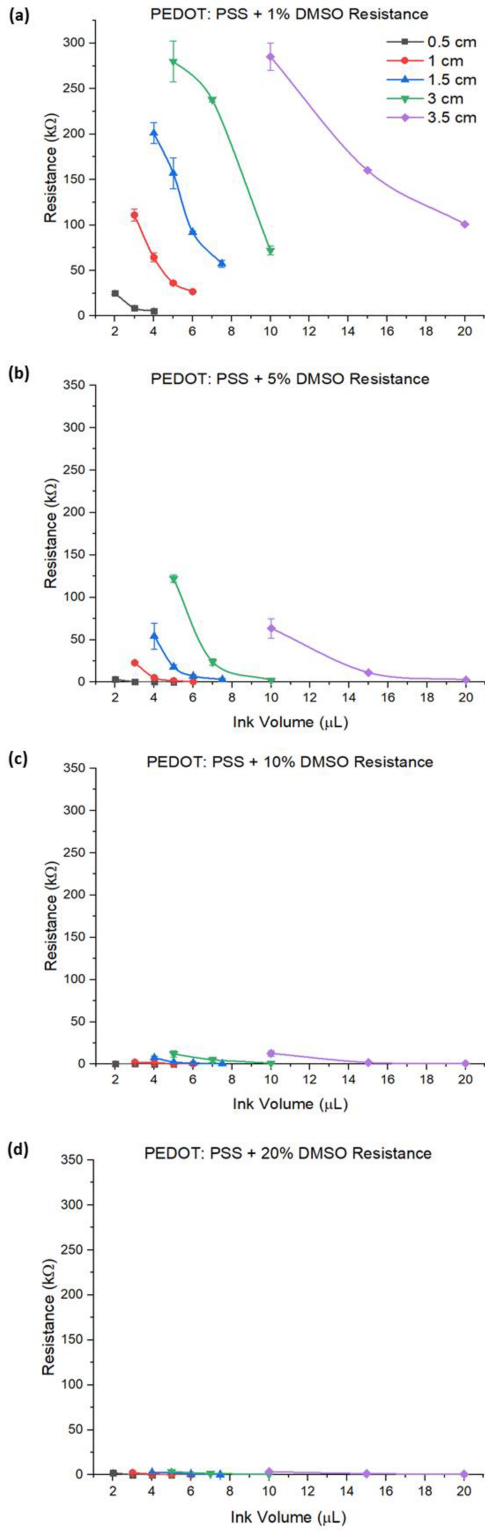


Figure 2: Measured resistance values of fabricated paper resistors at different lengths and applied ink volumes for DMSO percentage at (a) 1%, (b) 5%, (c) 10%, and (d) 20%.

Capacitance characterization

The charging and discharging profiles of the paper-integrated capacitor were measured both with and without the addition of the PVA- Na_2SO_4 gel electrolyte (Figure 3). For the non-electrolytic case, the applied resistance was 200 kΩ with a resulting time constant of 14.2 μs, while the electrolytic case utilized a 100 Ω and exhibited a time constant of 27.14 ns. According to this data, the electrolytic capacitor achieved almost 100 times higher capacitance than it did without the electrolyte, and so the electrolytic capacitor was chosen to be used in subsequent designs.

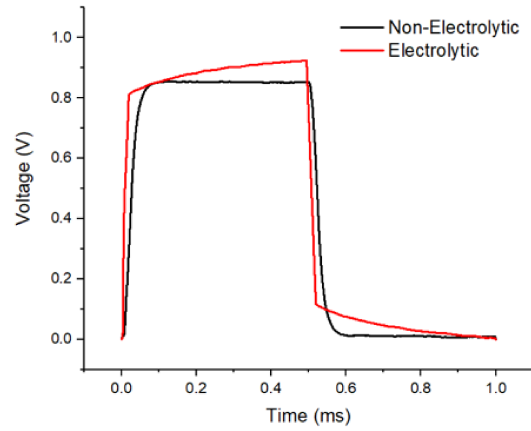


Figure 3: Paper capacitor charge/discharge cycle with and without PVA- Na_2SO_4 electrolyte.

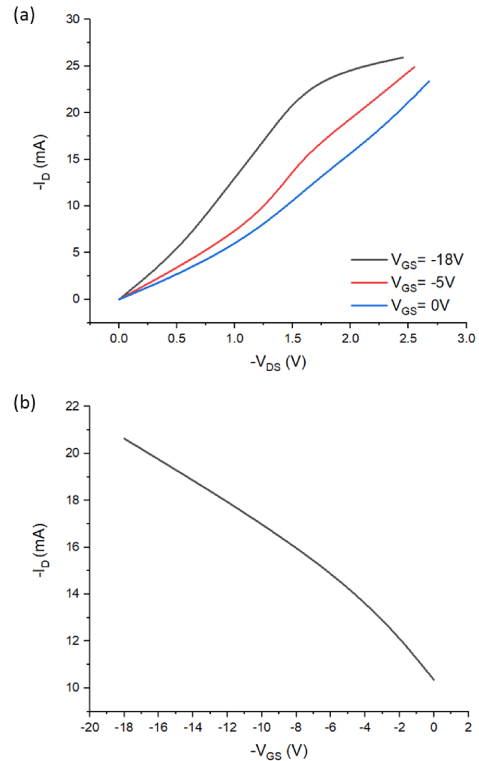


Figure 4: Measured (a) output characteristics and (b) transfer characteristics ($V_{DS} = -1.5V$) of paper-fabricated FET.

Transistor characterization

The fabricated electrolytic FET was evaluated via its output and transfer characteristic plots (Figure 4). The output characteristic

plot reveals the relationship between the voltage at the drain electrode and the drain current at varying gate biases, whereas the transfer characteristic plot demonstrates the drain current as the gate voltage is modified. The trends exhibited in both plots show that the FET successfully achieves the behavior of a depletion-type p-channel FET [13].

Paper PCBs

Each type of component was used in the design of a paper PCB. The circuit model containing four fully functional paper resistors, a capacitor, and a transistor was fabricated into a single sheet of filter paper, exemplifying the ease in which one could manufacture and customize paper circuitry that requires resistors, capacitors, and transistors. The entire circuit was obtained on a thin sheet of paper and within a small area, occupying a volume of only approximately 0.5 cm^3 .

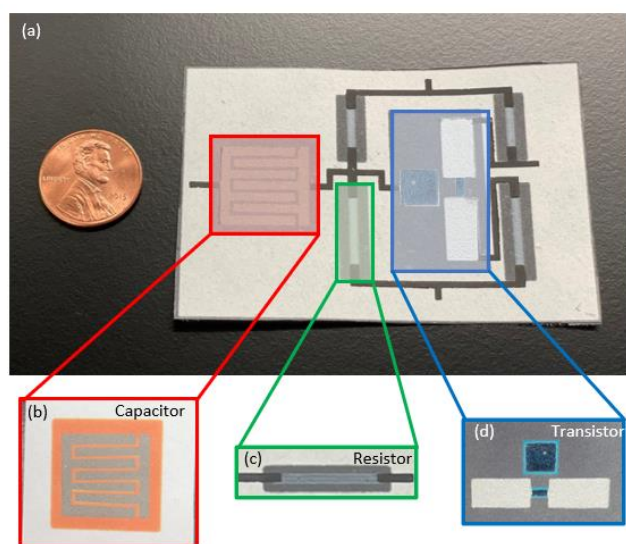


Figure 5: Photographs of (a) example paper printed circuit board (P-PCB) using all paper components, (b) individual paper capacitor, (c) individual paper resistor, and (d) individual paper transistor.

CONCLUSION

In this work, we have successfully demonstrated the capability of achieving functional electronic circuits on paper without significant disruption of the paper's biodegradability and affordability. Employing the presented techniques, users can devise any variation of the resistor, capacitor, and transistor circuits and simultaneously develop the components within a single, compact paper PCB. This capability implies facile integration of electronic circuitry within disposable sensor systems and other short-time use electronic device applications.

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CONTACT

*Prof. S. Choi, tel: +1-607-777-5913; sechoi@binghamton.edu