A 16-Channel High-Voltage ASIC with Programmable Delay Lines for Image-Guided Ultrasound Neuromodulation

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***Abstract*—Conventional ultrasound neuromodulation (USN) systems utilize bulky electronics to drive a single-element ultrasonic (US) transducer. To achieve large-scale USN within a given tissue volume, a US transducer array should electronically be driven in a beamforming fashion to steer focused US beams towards different neural targets. This paper presents a 16-channel high-voltage ASIC (with 4-channel US imaging frontend) for driving a 16-element piezoelectric transducer array suitable for image-guided USN applications. The ASIC integrates programmable delay lines for 16 channels, controlled by an external interface with only three wires, to provide beam focusing and steering capability. The ASIC also integrates 8-channel neural recording frontend and an inductive power management circuity. The ASIC was designed and fabricated in a 0.25 µm HV BCD CMOS process with an area of 8.7×6.6 mm^2. In measurements, the performance of the high-voltage drivers with programmable delay lines in generating 50 V peak-peak pulses at 2 MHz with the total delay range of 32.05 µs and fine tuning has been demonstrated.**

Keywords— Ultrasound neuromodulation, high-voltage driver, programmable delay, beamforming, neural interface)

I. Introduction

Transcranial focused ultrasound neuromodulation (USN) is an emerging technique for both exciting and inhibiting neural activity in animals and even humans with improved millimeter-scale spatial resolution, compared to its noninvasive counterparts [1]-[3]. Conventional USN systems often utilize commercially available off-the-shelf electronics, which are extremely bulky, to drive a single-element piezoelectric transducer, focusing an ultrasound (US) beam at a specific neural target [4]-[6]. However, these systems can only be utilized on anesthetized or highly constrained animals due to their bulkiness. They also suffer from limited spatial coverage as their US transducers must be mechanically moved to change the stimulation target.

There have recently been some efforts to partially mitigate some of these issues. For example, miniature single-element US transducers, connected to the driving electronics through a cable, have been mounted on rodents' heads in [7]-[9] to enable longer-term studies on behaving animals. But these systems still suffer from a fixed transmitted US beam, providing a fixed stimulation site. To achieve large-scale USN, a US transducer array (similar to Fig. 1) should electronically be driven in a beamforming fashion to steer focused US beams towards different neural targets. Recently, several US transducer arrays with different specifications have been reported in the literature for USN applications [10]-[13].

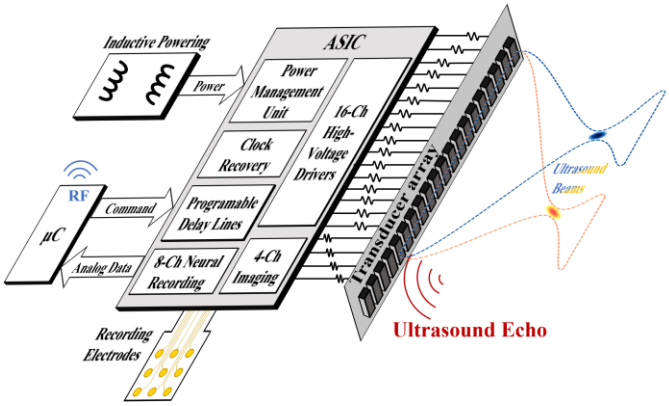

Fig. 1. Simplified schematic diagram of the proposed system for USN using a 16-channel ASIC with programmable delay lines (PDLs) for driving a 16-element linear US array (neural-recording and imaging AFEs as well as the power-management circuitry will be discussed in our future work).

Several CMOS ASICs have also been presented recently for driving US transducers arrays in USN applications. In [14], a two-dimensional (2D) transmit beamformer CMOS ASIC has been presented in a 5 V process with integrated piezoelectric transducers at 8.4 MHz. But this ASIC operates at low 5 V supply, thereby generating only up to ~ 100 kPa of US pressure outputs. A high-voltage (HV) 2D transmit beamformer CMOS ASIC at 60 V has been presented in [15] with an integrated 2 MHz capacitive micromachined US transducer (CMUT) array, achieving a higher US pressure output of ~ 575 kPa at a 5 mm depth. These ASICs provide beam focusing/steering capability with a maximum delay range of one cycle ($T = 1/f$, where f is the sonication frequency) using an on-chip delay-locked loop.

For guiding the US beam of a phased array in USN, the same US phased array can potentially be used for imaging the tissue [12]. Although a delay range within one T is sufficient for USN due to its use of many pulses, utilizing the same US phased array for transmit beamforming in imaging, which uses one pulse or a few number of pulses, requires a delay range larger than T. It is known that for beam focusing and steering at a depth F with the

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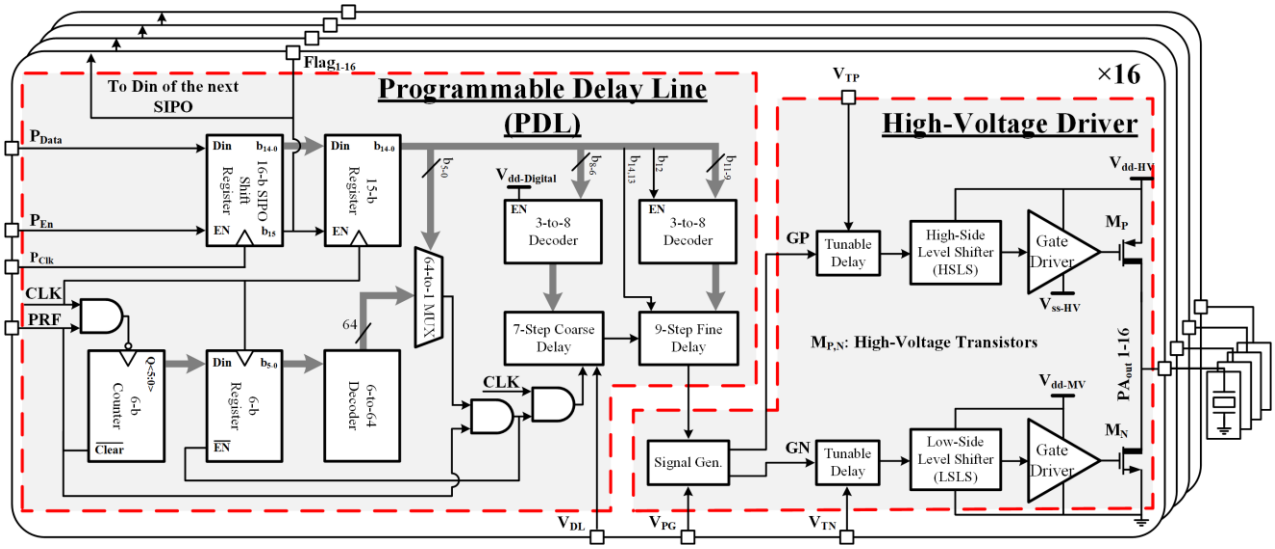

Fig. 2. Block diagram of the 16-channel US stimulator (and imaging pulser) of the ASIC including 16 PDLs and HV drivers with level shifters.

azimuthal angle θ_s, the excitation time delay (Δt_n) for the n^{th} element in a linear array should be:

$$\Delta t_n = (F/c)(1 - \sqrt{[1 + (nd/F)^2 - 2ndsin(\theta_s)/F]}) \qquad (1)$$

where c is the US velocity in the targeted medium and d is the interelement spacing [16].

This has motivated us to design a 16-channel HV CMOS ASIC (as shown in Fig. 1) with optimal programmable delays, generated by programmable delay lines (PDLs), for each channel based on (1) that can be used for both US stimulation and tissue imaging in image-guided USN applications. All 16 PDLs can be programmed using an external interface with only three wires, reducing the complexity of the system and number of ASIC pads. This paper is focused on the PDLs and HV drivers. The ASIC also integrates 8-channel neural recording and 4-channel US imaging analog frontends (AFEs), and an inductive power-management circuity, envisioning a closed-loop neural interface with image-guided US beam delivery and wireless powering (to be presented in future).

The paper is organized as follows. Section II describes the ASIC architecture with a focus on the PDL and HV driver circuits. Section III summarizes the simulation and measurement results of the HV drivers and PDLs, followed by the concluding remarks in Section IV.

II. ASIC Architecture

Fig. 1 shows the simplified block diagram of the proposed ASIC comprising of 16-channel HV drivers, 16 PDLs, clock recovery, 8-channel neural recording and 4-channel US imaging AFEs, and inductive power management. The ASIC has been designed in a 0.25 µm HV BCD CMOS process that supports HV transistors up to 60 V. A reference clock ($CLK = 1/T$) at the sonication frequency is generated from either the inductive power carrier or an external signal for HV drivers. The power management includes a full-wave passive rectifier and multiple low-dropout regulators (LDOs) to generate $V_{dd\text{-}MV}$ = 5 V, $V_{dd\text{-}Imaging}$ = 4 V, $V_{dd\text{-}Analog}$ = 2.4 V, and $V_{dd\text{-}Digital}$ = 2.4 V. Also, an on-chip LDO generates $V_{ss\text{-}HV}$ = 45 V from an external supply $V_{dd\text{-}HV}$ = 50 V.

The ASIC can communicate with an external interface (e.g., a microcontroller) through three wires to provide the optimal delay for each channel (using 16 bits per channel) for focusing and steering the beam at a particular F and θ_s based on (1). The CLK signal is delayed by the PDLs, each of which can provide a delay range up to ~ 63×T with fine tuning, and is applied to 16 HV drivers that drive 16 US elements with pulses as large as 50 V (peak-peak). The same drivers can also be used for imaging the tissue with transmit beamforming along with 4 imaging AFEs, which are designed with transimpedance amplifiers to amplify the received US echoes from 4 additional US elements. Finally, the chip also integrates an 8-channel neural recording AFE (low-noise amplifiers with capacitive feedback) to provide electrophysiological recording function in addition to USN. In the following, the ASIC circuits are described with an emphasis on the PDL and HV driver.

A. Programmable Delay Line (PDL)

Fig. 2 shows the block diagram of the 16-channel US stimulator (and imaging pulser) including 16 PDLs and HV drivers with level shifters. The PDLs, operating with low voltage ($V_{dd\text{-}Digital}$ = 2.4 V), generate 16 signals with optimal delays, which are fed into the level shifters. The delay cells in each PDL are programmed with 16 bits (total 16×16 = 256 bits for 16 PDLs) using an external interface. As shown in Fig. 2, three signals are needed to program all 16 PDLs: P_{Data}, P_{Clk}, P_{En}. The P_{Data} signal carries 256 serial bits, which are read by the ASIC at the rising edge of the P_{Clk} signal. The 16th bit for each channel (i.e., b_{15} out of $b_{15\text{-}0}$) is always "1". The P_{En} signal is used to enable the ASIC programming, which can also be used to program several ASICs to extend beyond 16 channels.

As shown in Fig. 2, each channel includes a 16-bit serial-in-parallel-out (SIPO) shift register, the clock and enable pins of which are all connected to external P_{Clk} and P_{En}, respectively. The input data pin (Din) of first channel SIPO is connected to

external P_{Data}, while *Din* of SIPOs in the next channels is connected to the most significant bit output (b_{15}) of SIPO in the preceding channel. When all 256 bits of P_{Data} are in, b_{15} outputs of all 16 SIPOs go high, enabling a 15-bit register in each channel to hold the 15-bit ($b_{14\text{-}0}$) delay profile per channel. The b_{15} outputs of all SIPOs are given to an AND gate to raise a *Flag*, indicating successful programming.

The 15 delay bits in each channel control three delay cells: 1) Six bits ($b_{5\text{-}0}$) provide delay steps of *1/T* generated by a 6-bit counter (e.g., 0 to 63×0.5=31.5 µs with 500 ns steps at f = 2 MHz); 2) Three bits ($b_{8\text{-}6}$) provide 7 steps of coarse delay, which is tunable with an external voltage, for a total delay of 175-500 ns; 3) Six bits ($b_{14\text{-}9}$) provide 9 steps of fine delays (for fine tuning) with a total delay of ~ 50 ns. The fine and coarse delay lines are designed with selectable delay cells that include current-starved inverters loaded by small capacitors. These delays are controlled externally, and therefore, they can also be used to compensate for any PVT variations.

The recovered clock signal (*CLK* at f = 1/T frequency) is used to clock the counter for generating large delay steps of *1/T*. As shown in Fig. 2, the *CLK* signal is enabled by an external signal at a much lower frequency (called *PRF*) through AND gates to determine the desired stimulation pattern (or pulse repetition frequency). Decoders and multiplexers in each channel properly apply the delay bits to the delay cells. In brief, the *CLK* signal is first delayed by the counter with large delay steps, and then extra delays are provided by first the coarse delay cells followed by the fine delay cells to achieve the required delay in each channel.

B. *High-Voltage Driver*

Fig. 2 shows the schematic diagram of the HV driver and level shifters in each channel to drive a 16-element linear US array with pulses as large as 50 V. To drive each US transducer efficiently, a class DE driver with non-overlapping switching signals is designed with both zero-voltage switching (ZDS) and zero-derivative switching. The HV driver is comprised of HV PMOS and NMOS transistors, M_P (W/L = 2 mm / 0.4 µm) and M_N (W/L = 1.44 mm / 0.7 µm), respectively.

To provide optimal switching signals for driving M_P and M_N, the delayed *CLK* signal for each channel is first converted into two switching signals, *GP* and *GN*, with optimal (and adjustable through external V_{PG} signal in Fig. 2) duty cycle. To further adjust the timing of *GP* and *GN* signals, two tunable delay cells (through analog signals V_{TN} and V_{TP} in Fig. 2) with a maximum delay range of 50 ns are used. The *GP* and *GN* signals with [0, 2.4 V] levels are then fed into high-side level shifter (HSLS) and low-side level shifter (LSLS) to create signals with [$V_{ss\text{-}HV}$, $V_{dd\text{-}HV}$] and [0, $V_{dd\text{-}MV}$] levels to drive M_P and M_N transistors with gate drivers, respectively.

III. Simulation and Measurement Results

Fig. 3 shows the die micrograph of the fabricated ASIC in the 0.25 µm HV BCD CMOS process, occupying 57.4 mm^2 active area with pads. Fig. 4 shows the transient simulation results of the key signals in the HV driver, including the output of one PDL, *GP*, *GN*, HSLS and LSLS outputs, and the HV driver output (PA_{out}) as shown in Fig. 2. The chip was simulated at f = 2 MHz (*CLK* in Fig. 2) while loading the HV driver with

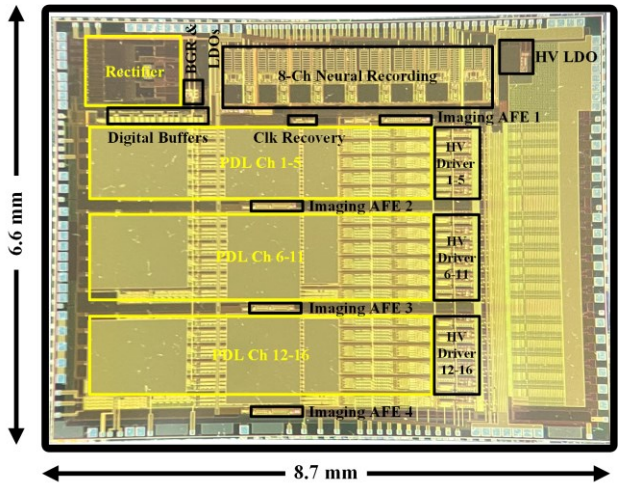

Fig. 3. The chip micrograph occupying 57.4 mm^2 active area including pads.

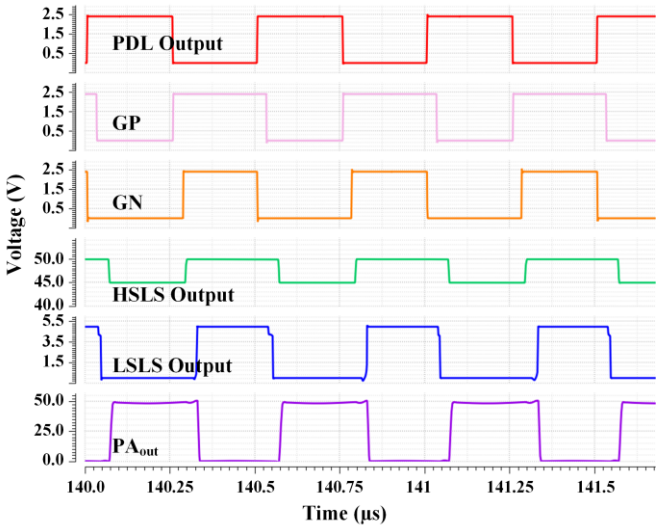

Fig. 4. Simulated transient waveforms (PDL output, *GP*, *GN*, HSLS and LSLS outputs, PA_{out} in Fig. 2) of the HV driver, loaded by a modeled piezoelectric transducer at 2 MHz.

the Butterworth-Van Dyke model of a small piezoelectric transducer with the resonant frequency of 2 MHz [9]. Fig. 4 shows that *GP* and *GN* are generated from the PDL output indicates that both M_P and M_N turn on, does not occur. The HSLS and LSLS circuits shifted *GP* and *GN* to [45 V, 50 V] and [0, 5 V] levels, respectively. These signals were applied to M_P and M_N, generating 50 V (peak-peak) pulses (PA_{out}) at 2 MHz across the modeled transducer.

To demonstrate the functionality of the PDLs and HV drivers in measurement, the ASIC was interfaced with a microcontroller (nRF24LE1, Nordic Semiconductor, Norway) through three wires (P_{Data}, P_{Clk}, P_{En} in Fig. 2) to program all 16 PDLs of the ASIC with different delays ranging from 0 to 32.05 µs (*Clk* = 2 MHz). The ASIC *Flag* signal, indicating successful programming, was also monitored. Fig. 5 shows the measured waveforms of P_{En}, P_{Clk}, and P_{Data}, which were generated by the nRF24LE1, as well as the *Flag* output from the ASIC when 256 bits (corresponding to different delays as an example) were programmed into 16 PDLs at the rate of f_{PClk} = 4 MHz. The P_{En}

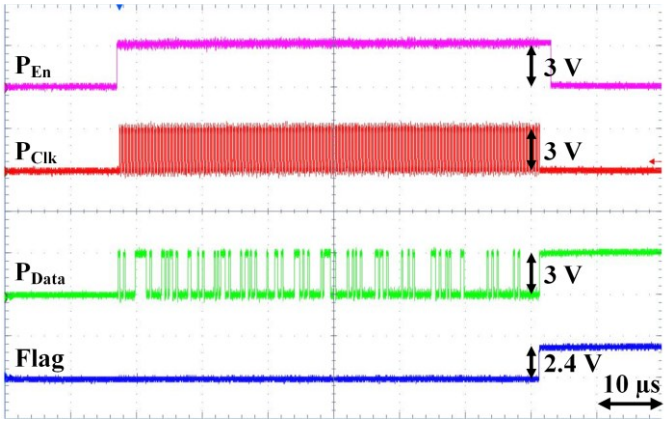

Fig. 5. Measured signals (P_{En}, P_{Clk}, P_{Data} from nRF24LE1, *Flag* output from ASIC) demonstrating successful programming of PDLs at f_{PClk} = 4 MHz.

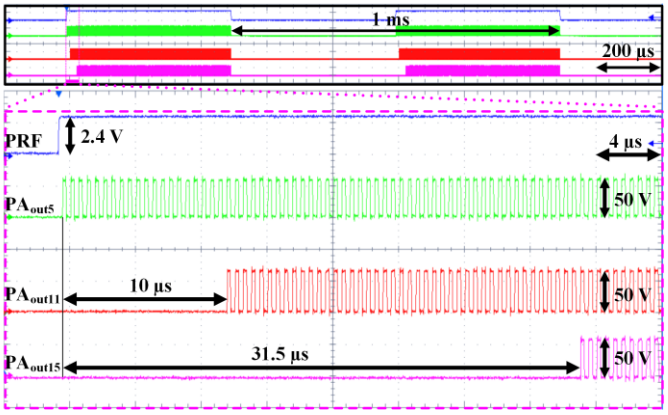

Fig. 6. Measured waveforms of three HV driver outputs $PA_{out5,11,15}$ (50 V) at 2 MHz when programmed with delays of 0, 10, and 31.5 µs (*PRF* = 1 kHz).

signal was first held high to select the ASIC and begin the data transmission. Then 256 arbitrary bits were generated on P_{Data} and were read by the ASIC at the rising edge of the P_{Clk} signal. As shown in Fig. 5, right after sending the 256th bit, the *Flag* signal went high by the ASIC, indicating all 16 PDLs were successfully programmed. Finally, P_{En} was held low to avoid any reprogramming of the ASIC due to any input changes.

Fig. 6 shows the measured waveforms for three different HV drivers ($PA_{out5,11,15}$ as an example), generating 50 V peak-peak pulses at 2 MHz with different delays of 0, 10, and 31.5 µs, which were programmed using the 3-wire interface. In this measurement PRF was set to 1 kHz, which is a typical value for USN applications. The Fig. 6 inset also shows the zoomed waveforms of the measured signals. When the external PRF signal became high, the drivers output 50 V pulses with different predefined delays (as long as PRF was held high). These measurement results show the functionality of the HV drivers and the programming circuits.

To characterize the PDL precisely, the total 5120 delay values for all available codes were measured at 2 MHz (*CLK* frequency in Fig. 2) by programming the ASIC. By operating at 2 MHz, the 6-bit counter provided a delay range of 0 to 31.5 µs with 500 ns steps. The coarse delay provided a range of 0 to 500 ns in 7 steps. The fine delay was used for fine tuning of ~ 50 ns. Therefore, a total delay range of 0 to 32.05 µs was programmed to the ASIC and was accurately measured.

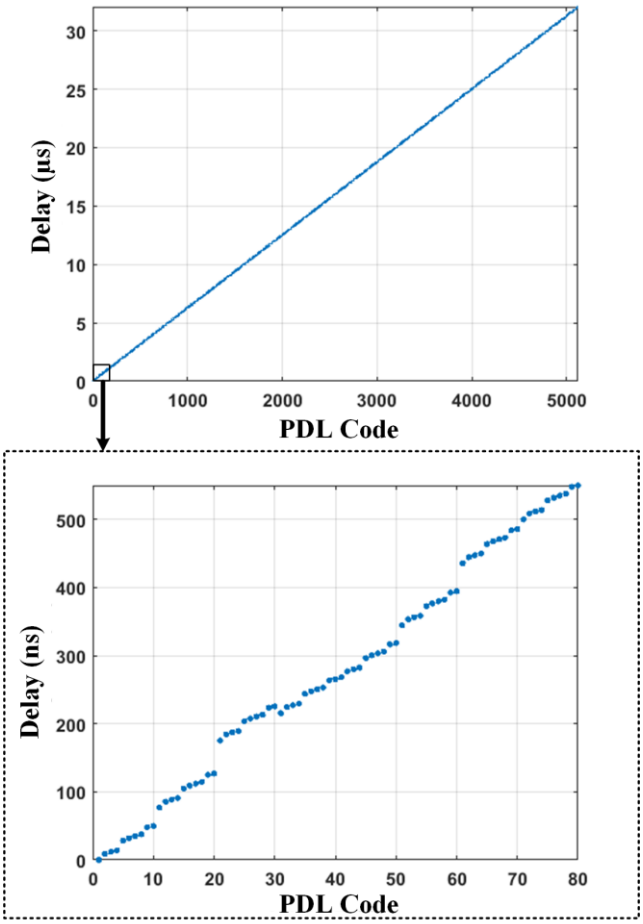

Fig. 7. Measured delay values for all available codes at 2 MHz (*CLK* frequency) by programming the ASIC with 5120 variations.

Fig. 7 shows the measured results of the PDL for all available codes. As expected, the whole range of 0 to 32.05 µs was provided by the PDL. The Fig. 7 inset shows zoomed of the ASIC in providing different delay values with high resolution. In brief, Fig. 7 shows that the ASIC can provide a large delay range with tens of ns resolution for optimal beam focusing and steering using optimal delays based on (1).

IV. Conclusion

An ASIC with 16 channels of high-voltage drivers and programmable delays was presented for driving a 16-element linear ultrasonic array to generate focused and steered ultrasonic beams suitable for image-guided ultrasound neuromodulation applications. The delay lines of all 16 channels in the ASIC were programmed with an external interface using only three wires. Measurement results demonstrated the functionality of the ASIC in generating 50 V pulses with different delays at each channel using a microcontroller for programming. In measurements with 2 MHz operation, a maximum delay of 32.05 µs was achieved with fine delay steps using a combination of coarse and fine tuning. In our future work, the ASIC will be integrated with our ultrasound arrays to demonstrate beam focusing and steering [17]. The ASIC also includes imaging and neural recording circuits for image-guided closed-loop neural interfacing.

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