Tunable Source of Quantum-Correlated Photons with Integrated Pump Rejection in a Silicon CMOS Platform

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Abstract: A wavelength-tunable, silicon photon-pair source based on spontaneous four-wave mixing, integrated with a pump rejection filter in a single, flip-chip packaged CMOS chip, is demonstrated with a coincidence-to-accidentals ratio of 9.1 with no off-chip pump filtering. © 2021 The Author(s)

Integrated silicon photonics is a leading candidate platform for quantum photonic technology due to its scalable, high fidelity CMOS manufacturing and its ability to operate at standard telecommunication wavelengths [1, 2]. Sources of indistinguishable correlated photon pairs are a basic building block required for such platforms to support quantum networking and information processing [1]. When biphotons are generated via spontaneous four-wave mixing (SFWM), a major challenge is to isolate the single-photon outputs from the strong classical pump field [3]. Previously, we demonstrated the first photon pair source in a CMOS platform [4], as well as the first source integrating a SFWM cavity and pump rejection filter on a single chip [5] with no additional external pump filtering. The fully passive device featured a cascaded array of wavelength spaced microring SFWM sources that, in presence of fabrication variations, would ensure one source ring is aligned to the high-order, microring based pump-rejection filter. However, this passive design precludes multiple copies of such integrated sources from being tuned to the same wavelength. In this work, we present a microring-based source and integrated pump rejection filters based on thermally tunable rings. This eliminates the array of sources, halving the device footprint, and will enable quantum interference between multiple such sources implemented and controlled on a CMOS photonics platform. The design also includes a new grating coupler design at 1550 nm, based on our bilevel unidirectional design [6], with simulated ~1 dB fiber-to-chip coupling loss. The source circuit [Fig. 1(a)] consists of a tunable microring resonator SFWM pair generator cavity and a tunable 8-pole bandpass filter formed by four cascaded 2^{nd} -order filters, occupying $460 \times 220 \,\mu\text{m}$ overall die area, including

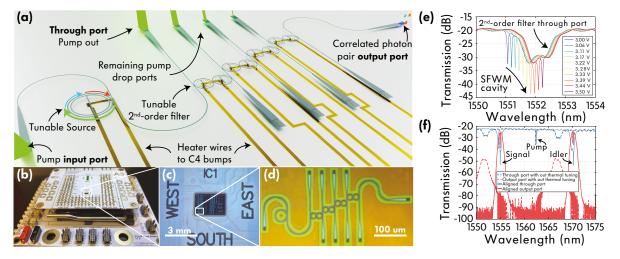


Fig. 1: (a) 3D rendering of photon pair source; (b) CMOS packaging scheme with chip carrier and host board; (c) SOI-CMOS die flip-chip attached to PCB with Si substrate removed via XeF_2 etch; (d) correlated photon pair source micrograph; (e) SFWM cavity tuning to match pump rejection filter; (f) photon pair source transmission spectra before and after tuning.

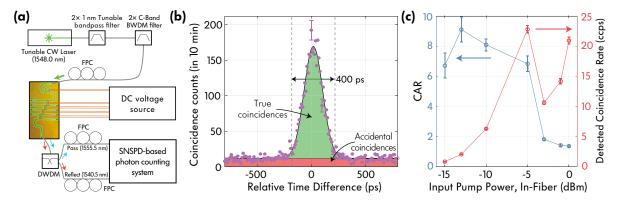


Fig. 2: (a) Schematic of experimental setup for measuring CAR and coincidence count rates using superconducting nanowire single photon detectors (SNSPDs) for time correlated single photon counting (TCSPC); (b) Coincidence histogram with 10 ps bin widths integrated for 10 minutes at an in-fiber input power of -10 dBm; (c) CAR and detected coincidence pair count rate as a function of pump power in the input fiber. The represented uncertainties are estimated from Poisson statistics, but additional sources of systematic error such as alignment stability are not quantified.

input/output and debug grating couplers [Fig. 1 (c,d)]. The 2nd-order filters are designed to achieve 42.3 dB maximum out of band rejection, half way between the signal and idler photon passbands (42 dB measured), which projects to 168 dB total pump rejection. Our direct pump rejection measurement for the entire filter gave 86 dB, limited by the photodetector noise floor. Scattered pump light that bypasses this filter is blocked by metal density fill around the silicon waveguides, whose primary purpose is comply with foundry design rules for pattern density fluctuations. The filters' passband width is 0.5 nm (60 GHz) – far wider than the source cavity linewidth of 6 GHz in order to minimize insertion loss. The source (filters) have thermal resonance tuning efficiencies of 0.15 nm/mW (0.24 nm/mW).

Fig. 2(a) shows the experimental setup for characterizing the photon pair generation rate and coincidences-to-accidentals ratio (CAR). The source and filters are thermally tuned for 1540.5 nm signal, 1548.0 nm pump, and 1555.5 nm idler wavelengths. Off-chip filters on the input side attenuate the pump laser's ASE noise in the signal and idler bands by over 100 dB. A dense wavelength division multiplexer (DWDM) placed after the output grating coupler (GC) is used as a signal splitter, and transmits the idler wavelength while reflecting the signal wavelength and and pump exiting the chip into separate output ports that are connected to SNSPDs (75 % quantum efficiency) and a time tagger. The DWDM routes incoming light to one of these two output ports, so there is no additional pump rejection filtering off-chip. Fig. 2 (b) shows an example histogram and Gaussian fit used to extract the CAR and coincidence rate and Fig. 2 (c) shows the trends with respect to pump power. We chose a $\pm 2\sigma$ coincidence window of 400 ps to define the CAR and pair generation rate, yielding a maximum CAR of 9.1 ± 0.8 at -13 dBm power in the input fiber and maximum coincidence rate of 21 ± 0.6 counts per second at 0 dBm power in the input fiber.

The CAR and coincidence rate are limited by 20 dB of insertion loss between the input and output fibers (10 dB per grating coupler), caused primarily by a mismatch between the 10 µm mode field diameter (MFD) of the input/output fibers and the 5 µm spot size of the grating couplers. We anticipate significant improvement in the device performance with fibers matched to the grating coupler apertures, since pair rate increases with the square of the linear transmission (i.e. double the improvement in dB). With the fully tunable source and filters, this work represents a new step towards creating a source of entangled photons that incorporates active photonic devices and feedback control circuits onto the same CMOS chip, utilizing a standard 45 nm process that can support hundreds of electronically-controlled photonic devices operating alongside millions of transistors, already previously used for classical applications [7].

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