A Fully Hardware-based Memristive Multilayer Perceptron

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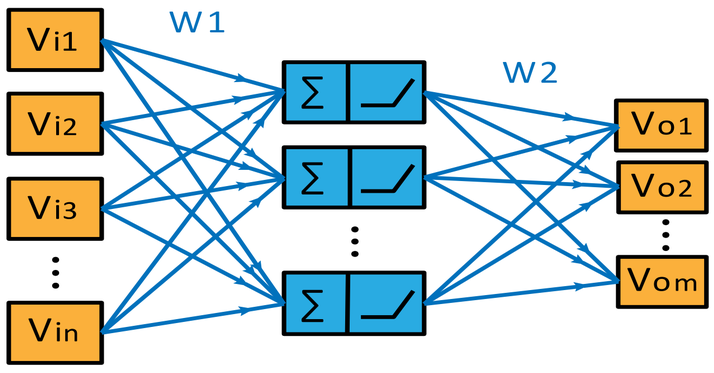
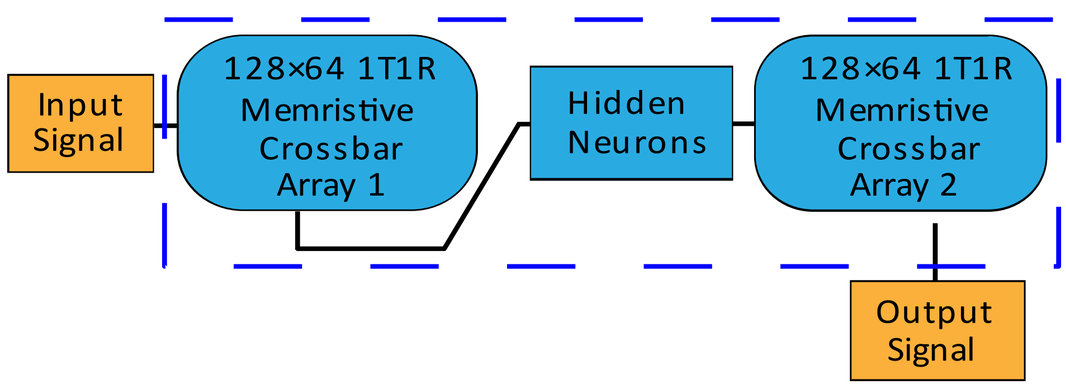
Summary

- Improving power consumption and computation throughput is essential in neural networks
- Fully hardware perceptron is a promising approach in this regard because of in-memory analog computing
- Memristors with their multi-level conductance represent the synapses of the neural network
- To achieve a fully hardware perceptron, activation functions (neurons) are required to be demonstrated
- In this work, we designed a compact multi-channel Rectified Linear Unit (ReLU) as the activation function
- We developed a two-layer perceptron and achieved a 93.63% recognition accuracy with the MNIST dataset

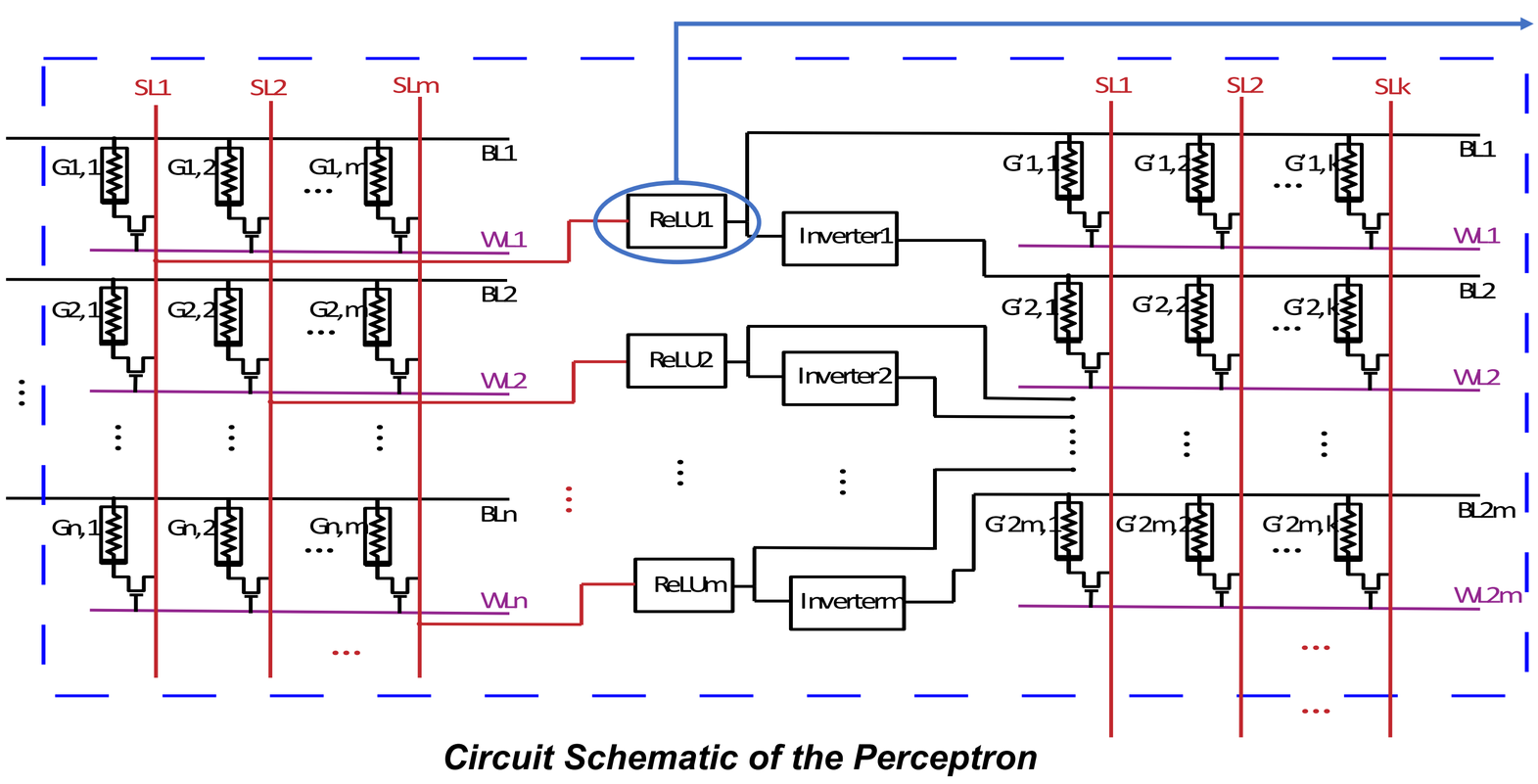
Two-layer Memristive Perceptron Design



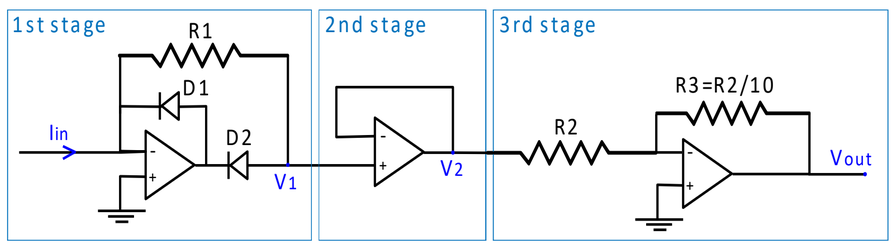
Schematic of a Two-layer Perceptron



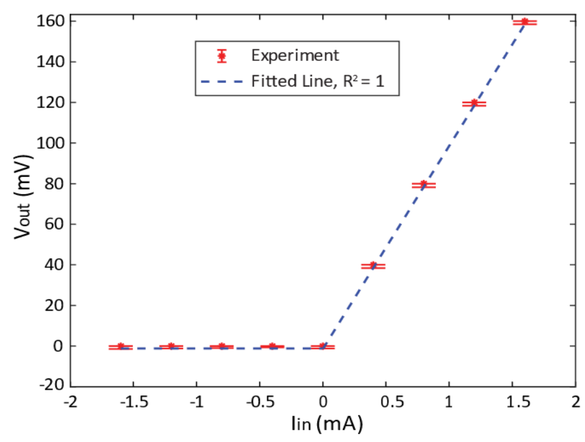
Block Diagram of the Implemented Perceptron



Circuit Schematic of the Perceptron

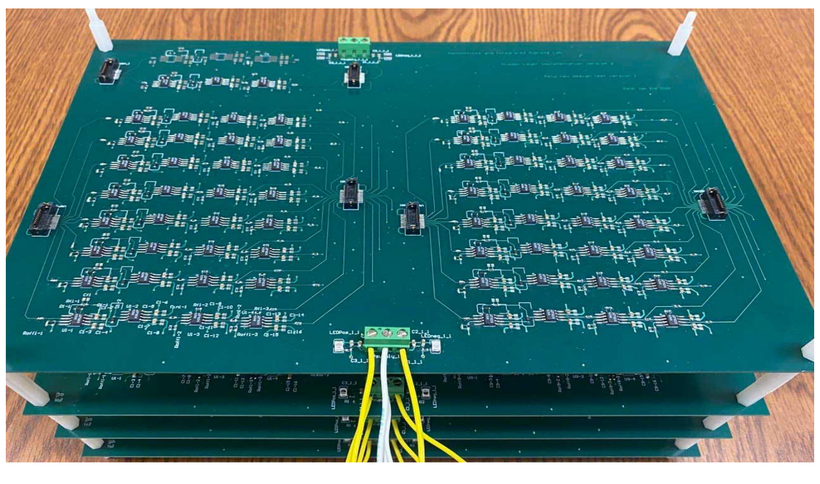


Circuit Schematic of the ReLU

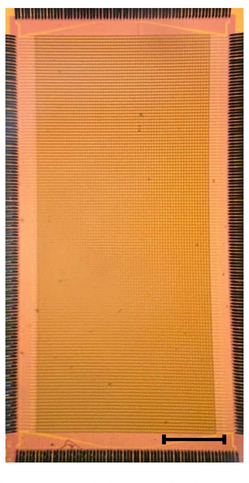


DC Characteristic of the ReLU

1T1R Array Used for the First Layer (scale bar: 1mm)



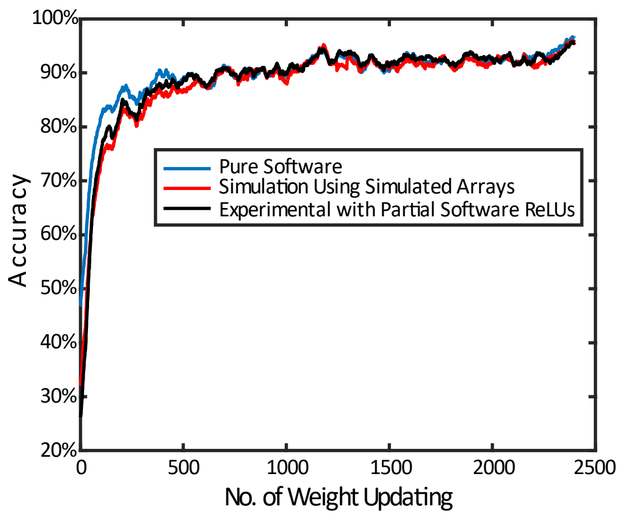
Stack of Multi-channel ReLU PCBs



1T1R Array Used for the Second Layer (scale bar: 1mm)

MNIST Digits Classification

- two-layer fully connected neural network is trained using the MNIST dataset
- 128 input neurons, 64 hidden neurons, and 10 output neurons
- Comparable accuracy with its partially software counterpart with much-improved power and execution time



Accuracy Trend During the Training

Implementation	Classification Accuracy(%)
Full Hardware	93.63
Partial Software	93.27
Pure Software	93.68

Inference Accuracy for Different Implementations

	All-hardware Neuron	Digital Neuron
Components	TIA + buffer + inverting amp.	TIA + buffer + S&H + ADC + DAC + Digital-based units + Digital computational unit (MCU or PC)
Power (mW)	2.16	70.84 + x
Area (mm^2)	0.042	0.237 + x

All-hardware vs. Digital Neuron Resources and Power Estimation using 65nm technology

Publication

[1] F. Kiani, J. Yin, Z. Wang, J. J. Yang, and Q. Xia, “A fully hardware-based memristive multilayer neural network," Science advances, vol. 7, no. 48, p.eabj4801, Nov 2021.

[2] F. Kiani, J. Yin, Z. Wang, J. J. Yang, and Q. Xia, “All Hardware-based Two-layer Perceptron Implemented in Memristor Crossbar Arrays," International Symposium on Circuits and Systems (ISCAS), May 2021.